Power and Area Efficient Error Tolerant Adder Using Pass Transistor XOR Logic in VLSI Circuits

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Abstract— **In adders the truncation and round off errors cannot be ignored. A new type of adder that is error tolerant adder (ETA) is proposed to tolerate those errors and to attain low power consumption. To rectify the errors in adders error tolerant adder (ETA) is proposed here. It increases the performance & reduces the delay by low power consumption. ETA mainly focuses on low power VLSI applications. ETA compensates the errors by adding the inputs parallel. In this paper to prove the efficiency of ETA normal CMOS XOR logic is replaced by, PASS TRANSISTOR logic.**

***Index Terms*—About four key words or phrases in alphabetical order, separated by commas.**

I. INTRODUCTION

In conventional digital VLSI design, it is assumed that a circuit/system should function perfectly to provide accurate results. The analog computation produces "good enough" results rather than accurate results. For many digital systems, the data already contained errors e.g. in a communication system errors may occur everywhere. The analog signal is coming from the outside world must first be sampled before being converted to digital data. The digital data are then processed and transmitted in a noisy channel before convert back to an analog signal at the back end of the system. During this process errors may be occurring. Due to the advance in transistor size scaling, factors such as noise and process variations which are previously not important are becoming important in today's digital IC design. Occurrence of errors is unavoidable in modern scaled VLSI technology and to overcome all.

To deal with error tolerant problems, some truncated adders have been reported, but are not able to perform well in its speed, power, area, or accuracy. The error tolerant adder designs produce almost correct results at the given required accuracy, and obtain power reductions and performance improvements in return. Approximate design exploits a trade off of accuracy in computation versus performance and power.

Relaxing the requirement of accuracy for design may dramatically reduce cost of manufacturing cost of verification, power consumption and delay. Leveraging the application having error tolerance, we can design adder which provide approximate result very fast compared to conventional design. With small loss in accuracy, provide huge improvement in power, delay and area. The Error Tolerant Adder (ETA) provides high the speed by cutting down the carry propagation.

II. NECESSITY OF ERROR TOLERANT ADDER

Most of the adder structures discussed in this paper is applicable to general purpose designs, with a few objections. Increasingly huge data sets and the need for instant response, the adder should be large and fast. The traditional ripple carry adder (RCA) is therefore no longer suitable for large adders because of its low speed performance.

Many different types of adders, such as the carry skip adder (CSK), the carry skip adder reduce the carry propagation time by skipping over groups of consecutive adder stages. The carry skip adder is usually comparable in speed to the carry look ahead adders, but it requires less chip area and consumes low power compared to carry look ahead adder.

Then next the Carry Select Adder (CSL), the carry select adder consists of two ripple carry adders are used to calculate the addition twice, one addition is computed assuming carry input ''1'' and other as ''0''. The correct output is then selected upon the arrival of carry in and carry look ahead adder (CLA), have been developed. The carry look ahead adder has lower delay but requires much more complex circuitry in achieving its performance However, there are always trade-offs between speed and power. The error tolerant design can be a potential solution to this problem. By sacrificing some accuracy, the ETA can attain great improvement in both the power consumption and speed performance.

III. PROPOSED APPROACH

In a conventional digital adder circuit, the delay is mainly due to the carry propagation chain all along the critical path, from the least significant bit (LSB) to the most significant bit (MSB). A major proportion of the power consumption of an adder is due to the unwanted signal components that are caused by the carry propagation. Therefore, if the carry propagation can be eliminate a great improvement in speed performance and power consumption can be achieved. In this paper, we propose a novel addition arithmetic that can achieve great saving in speed and power consumption. This new addition arithmetic can be illustrated by an example shown in Fig. 1. First we divide the input operands into two parts. They are accurate part and inaccurate part. An accurate part that includes several higher order bits. The each

part length is not necessary be equal. The addition process starts from the centre (joining point of the two parts) towards the two opposite directions simultaneously. In the example of Fig.1. The two 16 bit operands, A= ‘‘1011001001011001’’ (45657) and B= ‘‘1101110110010100’’ (56724), are divided equally into 8 bits each for the accurate and inaccurate parts.

In accurate part normal addition method applied from right to left (LSB to MSB). This is to preserve its correctness since the higher order bits play a more important role than the lower order bits. No carry signal will be generated at any bit position to eliminate the carry propagation path. To minimize the overall error, a special strategy is adapted and can be described as follow: 1) check every bit position from left to right (MSB to LSB); 2)if both input bits are ‘‘0’’ or different, normal one bit addition is performed and the operation proceeds to next bit position; 3)if both input bits are ‘‘1’’ the checking process stoped and from this bit, all sum bits to the right are set to ‘‘1’’. The addition mechanism described can be easily understood from the example given with a final result of ‘‘1100011111011111’’ (102367).

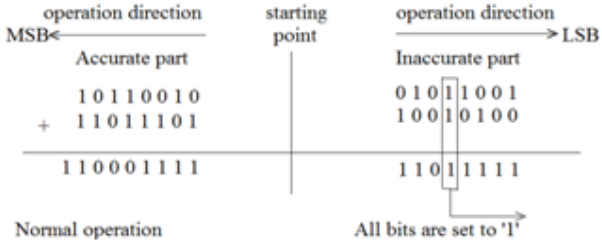


Figure 1 proposed adder

The above addition should actually yield ‘‘1100011111101101’’ (102381) if normal arithmetic has been applied. The total error generated can be computed as OE= 102381-102367 =14. The accuracy if the adder with respect to these two input operands is ACC= (1-14/102381)*100%=99.98%. By eliminating the carry propagation path in the inaccurate part and performing the addition in two separate parts simultaneously, the overall delay time is greatly reduced, so is the power consumption.

IV. Hardware Implementation

The block diagram of the ETA that adopts our proposed addition arithmetic is provided in Fig. 2. This structure consists of two parts: an accurate part and an inaccurate part. The accurate is constructed using a conventional adder such as the RCA, CSK, CSL, or CLA. The carry in of this adder is connected to ground. The inaccurate part contains two blocks: a carry free addition block and a control block. The control block is used to generate the control signal, to determine the working mode of the carry free addition block.

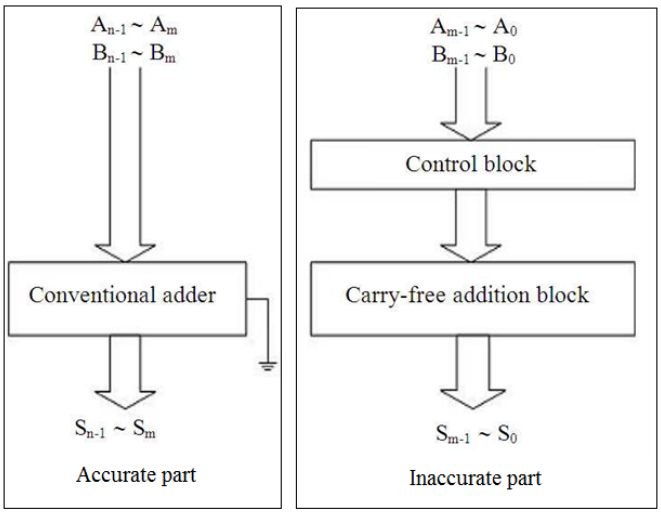


Figure 2: Hardware Implementation

V. Design of ETA

A. Concept of divide Adder into Accurate and Approximate

Firstly we divide proposed ETA in to two parts in a particular manner. The dividing approach is based on a guess and verify stratagem, depending on the requirements, such as accuracy, speed, and power.

First, we define the delay of the proposed adder as Td=max (Eh, El) where Eh is the delay in the accurate part and El is the delay in the inaccurate part. With the proper dividing strategy, we can make Eh approximately equal to El and hence achieve an optimal time delay.

B. Design of Accurate Part

In the proposed 32-bit ETA, the accurate part consists of 12 bits. The Ripple Carry Adder, has been chosen for the accurate part of the circuit since it is the most power saving conventional adder, The Ripple Carry Adder, being the simplest one, uses the least hardware circuitry when compared to all other traditional adder circuits in use is shown in Fig 3.

The delay of the Ripple Carry Adder increases linearly with the number of bits with a worst case delay of O(n). This worst case delay makes it slow when large bit sizes are used.

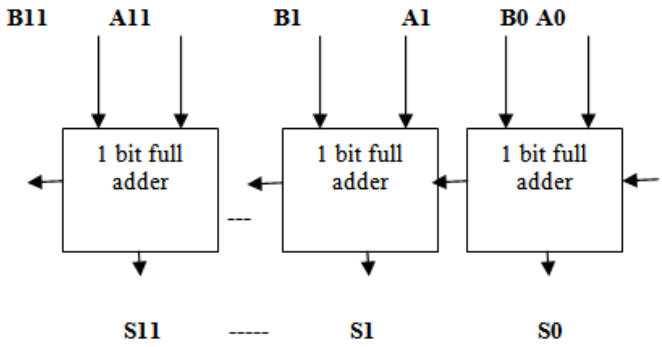


Fig.3: 12 bit ripple carry adder

C. Design of the Inaccurate Part

The inaccurate part consist of 20 bits and it is the most essential section in the proposed ETA as it determines the accuracy, speed performance, and power consumption of the adder. The inaccurate part consists of two blocks: the carry free addition block and control block.

The function of the control block is to detect the first bit position when both input bits are ‘‘1,’’ and to set the control signal on this position as well as those on its right to high. It is made up of 20 control signal generating cells (CSGCs) and each cell generates a control signal for the modified XOR gate at the corresponding bit position in the carry free addition block.

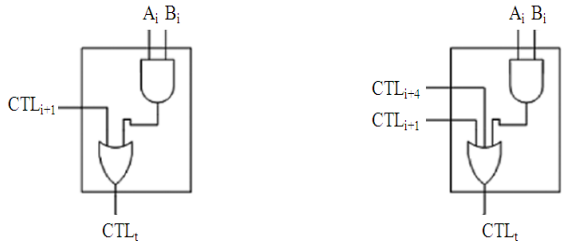


Fig.4: Control Signal Generating Cells of type I & II

Two types of CSGC, labelled as type I and II, are designed, and the schematic implementations of these two types of CSGC are provided.

The new combination of CSGC will reduce the propagation delay here the dark shaded cells are the critical path of the control block. For example, if 12th CSGC group finds the both input bits ‘1’ then the control signal is made high from this CSGC cell to the rightmost cell, here the delay is reduced hardly by CSGC II. Where the CSGC II in each block helps the control signal from the neighbour block to bypass through separate connections to other CSGC II, so that fast signal processing will happen.

D. Carry free Addition block

The carry free addition block consists of modified XOR gate, which produce resultant sum by getting the control signal from the control block. Here, 12 modified XOR gates are used shown in figure 5. In this modified XOR gate, three transistors M1 & M2 and M3 are added to the conventional XOR gate. The operation mode of the modified XOR gate is decided by the control signal from control block. If CTL=0, then M1 & M2 are turned on, while M3 is turned off, while M3 is turned on, sum node is connected to VDD and hence the sum=1.

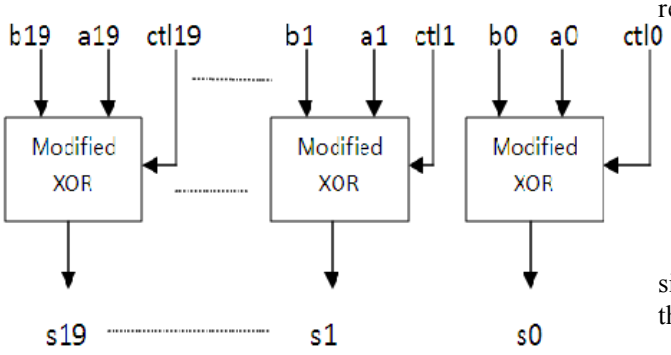


Fig 5: Architecture of Carry Free Addition Block

VI. Proposed Logic Methods

A. Pseudo NMOS logic

Compared to CMOS, this family has higher packing density, since for n inputs only n+1 transistors are required. The main disadvantages with Pseudo-NMOS gates is the large static power dissipation that occurs whenever a pull down path is activated. Has much smaller pull up network than static gate. Pull down time is longer because pull up is fighting. For logic 0 output, pull up and pull down form a voltage divider. Must choose n, p transistor sizes to create effective resistances of the required ratio. Effective resistance of pull down network must be computed in worst case series n-types means larger transistors

B. Complementary Pass Transistor logic (CPL)

Complementary pass transistor logic or “Differential pass transistor logic” refers to a logic family which is designed for certain advantages. It is common to use this logic family for multiplexers and latches.

CPL uses series transistors to select between possible inverted outputs values of the logic, the output of the non inverted inputs are needed to drive the gates of the pass transistor. The CMOS transmission gates consist of nNMOS and pMOS transistor connected in parallel.

C. Pass Transistor logic (PTL)

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistor are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional cmos logic switches transistors so the output connects to one of power supply rails, so logic voltage levels in a sequential chain do not decrease. Since there is less isolation between input signals and outputs, designers must take care to assess the effects of unintentional paths within the circuit. For proper operation, design rules restrict the arrangement of circuits, so that sneak paths, charge sharing, and slow switching can be avoided. Simulation of circuits may be required to ensure adequate performance.

VII. Experimental Result and Comparison

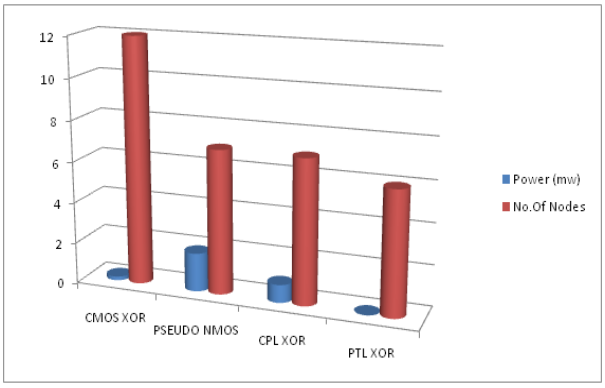
To determine the advantages of the proposed method, simulate the complementary pass transistor logic along with three types of logics.

TABLE I

POWER AND AREA RESULT S

TYPE	POWER(MW)	NO.OF NODES (TRANSISTOR COUNT)
CMOS XOR	0.185	12
PSEUDO NMOS XOR	1.673	7
COMPLEMENTARY PASS TRANSISTOR XOR	0.08752	7
PASS TRANSISTOR XOR	0.002673	6

Comparison Result of XOR logics



VIII. CONCLUSION

In this project, the concept of error tolerance is introduced in VLSI design. A novel type of adder, (error-tolerant adder), which trades certain amount of accuracy for significant power saving and performance improvement, is proposed. By eliminating the carry propagation path in the inaccurate part and performing the addition in two separate parts simultaneously, the overall delay time is greatly reduced. In existing system CMOS XOR logic gate is used. By using these systems the power and area are reduced in a range of 0.185 mw and 12 transistors are used. In proposed system, the comparison can be done for pseudo NMOS XOR logic, complementary pass transistor XOR logic, and pass transistor XOR logic by using micro wind simulator tool. As the analysis of comparison result shows that pass transistor XOR logic is better than others. It decreases the power and area in a range of 0.002673 mw and 6 transistors are used.

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