DESIGN AND PERFORMANCE ANALYSIS OF FAULT SECURE NETWORK-ON-CHIP USING FPGA

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Abstract — **Network on-chip is a novel designing communication protocol. It creates a communication between the on-chip cores. It has been proposed as one of the interconnect solutions for future systems-on-chip (SoCs). This paper presents an offline/online concurrent scan based built-in-self-test (scan-BIST) method for a Network-on Chip (NoC). The proposed architecture contains a special scan cell and an Embedded Test Core (ETC) as its test source. The ETC performs a static flow control and a centric average power consumption control during the proposed test mechanism. This shows the design and implementation of a novel pipeline circuit-switched switch to support guaranteed throughput. The circuit-switched switch, based on a backtracking probing path setup, operates with a source-synchronous wave-pipeline approach. The switch can support a dead- and live-lock free dynamic path-setup scheme and can achieve high bandwidth, high area and energy efficiency. The proposed BIST methodology enables a fast go/no-go BIST, with minor extra area in the NoC itself. Chip design is becoming increasingly communication-bound rather than computation-bound. In this paper the test scheduling problem is also addressed for such NoC-based SoCs. We assume a hybrid BIST approach, where test sets of individual cores are composed of pseudorandom and deterministic test sequences and, contrary to many other scheduling approaches, not treated as black boxes. This work also presents two more technique called N-detect test relaxation and hybrid algorithm to improve the performance of the system.**

Index Terms—**Network-on-chip (NoC), Fault tolerance, BIST, LFSR.**

I. INTRODUCTION

In the area of Embedded Systems, there is a desire to create 'Systems-On-Chips'(SOC's), the implementation and integration of multiple computer components or entire electronic systems (microcontroller, memory blocks, timers, voltage regulators, etc.) on a single chip. However, a new and increasingly popular research field which addresses some of the concerns of effective communication between on-chip components, Network-on-Chip (NoC) design, endeavors to bring network communication methodologies to on chip communications, in hopes of improving performance over current bus-based systems. Basically, design space exploration for Systems-on-Chip (SoCs) has mainly dealt with the computational aspects of the problem in the system at hand. However, as both the number of components on a single chip and their performance continue to increase, the design of the communication architecture plays a vital role in defining the area, performance and energy consumption of the overall system. In addition, global interconnects cause severe on-chip synchronization errors, unpredictable delays and high power consumption [1].Hence Networks-on-Chip have been proposed as an alternative communication platform capable of providing interconnections and communication among On-chip cores, handling performance, energy consumption and reusability issues for large integrated systems [2]. NoC is a promising alternative to classical bus-based and point-to-point communication architectures.

Network-on-chip is also used to design an on-chip switch/router to dynamically support (hard) guaranteed throughput [3] under the constraints of power, timing, and area. NoC provide guaranteed services such as uncorrupted, lossless, ordered data delivery and bounded latency is essential for the efficient construction of robust SoCs. NoC uses pipelined time-division-multiplexed circuit switching, to implement its guaranteed services [4]. But the TDM approach faces difficulty in the management of huge time-slot tables at guaranteed service routers for contention-free communication [4] and restriction of the routing function for deadlock-free data transfer in the virtual circuits with a priority approach may lead to throughput degradation in Packet-switched NoCs [5].So circuit-switching approach is chosen to provide guaranteed throughput due to its attractive QoS [6][7] property. After this setup, end-to-end data can be pipelined in order at the full rate of the dedicated links with low delay, no data jitter, and in a lossless manner.

Normally Built-in-self-test (BIST) is used to determine the fault tolerance in NoC. Built-In-self-Test (offline/online) of circuit with scan (scan-BIST) achieves high fault coverage with low overhead [8][9]. Additionally it does not require modifying the function logic and does not degrade system performance. During built-in self-test

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(BIST), the set of patterns generated by a pseudo-random patterns generator may not provide sufficiently high fault coverage and many patterns were undetected faults, so some pattern increases test time [10]. Hence, we reseed and modify the pseudo-random bit to improve test length and achieve fault coverage of 100%. The fact that a random test set contains useless (non fault dropping) patterns, so we use parallel technology, including both reseeding and bit modifying (also called pattern mapping) to remove useless patterns (i.e. reduce the test time), leading to very short test length.

In this paper, the first on-line BIST and BIST based diagnostic approach [11] are used for the programmable interconnect resources in FPGAs. This interconnect BIST is used in the roving STARs approach. This technique provides a complete BIST of the programmable interconnect followed by high-resolution diagnostics to support reconfiguration around the fault for fault-tolerant applications..Roving STARs approach takes two columns of CLBs to form a vertical STAR (V-STAR) and two rows of CLBs to form a horizontal STAR (H-STAR) as the global interconnect is usually spread into both the vertical and horizontal direction [11].Usually horizontal STAR and vertical STAR takes different time for scanning in FPGA.In this project the scanning time for both H-STAR and V-STAR are reduced to increase the testing speed. We also used a new technique called physically aware N-detect test relaxation to reduce the test pattern generation. This technique uses only 64 test patterns to detect faults but, whereas reseeding technique requires 256 test patterns. So it reduces the test time as well as it improves the performance.

The remainder of this paper is organized as follows. Section II addresses the related work of this project. Section III outlines the System Model for the proposed work. Section IV addresses the algorithm used in proposed architecture and its design. Section V deals with the Simulation result of the work. Finally, the conclusion is given in Section VI.

II. RELATED WORK

Network-On-Chip (NoC) design paradigm has been proposed as the future of ASIC design [12]. Fault tolerance in NoC can be obtained by communication architecture. In NoC communications the two major sources of errors are crosstalk faults and soft errors [2][13]. In the past, it was assumed that connections cannot be affected by soft errors because there was no sequential circuit involved. However, when NoCs are used, buffers and sequential circuits are present in the routers, consequently, soft errors can occur between the communication source and destination provoking errors. Fault tolerant techniques that once have been applied in integrated circuits in general can be used to protect routers against bit-flips. The results show that the effect of those faults in the SoC communication can be disastrous, leading to loss of packets and system crash or unavailability. Then it proposes and evaluates a set of fault tolerant techniques applied at routers able to mitigate soft errors and crosstalk faults at the hardware level. Such techniques were based on error correcting codes and hardware redundancy.

Another method of fault tolerance in NoC can be achieved by adaptive remapping [14]. The new algorithm can be used to dynamically react and recover from PE failures in order to maintain system functionality. The quality of results is similar to that achieved using simulated annealing but in significantly shorter runtime.

III. SYSTEM MODEL

In this section, the actual concept of system model is based on NoC architecture [15] and the design of fault tolerant NoC router.

A. Network-on-Chip architecture

Network-on-Chip or Network-on-a-Chip (NoC or NOC) is an approach to design the communication subsystem between IP cores in a System-on-a-Chip (SoC).NoCs can span synchronous and asynchronous clock domain logic. NoC applies networking theory and methods to on-chip communication and brings notable improvements over conventional bus and crossbar interconnection.

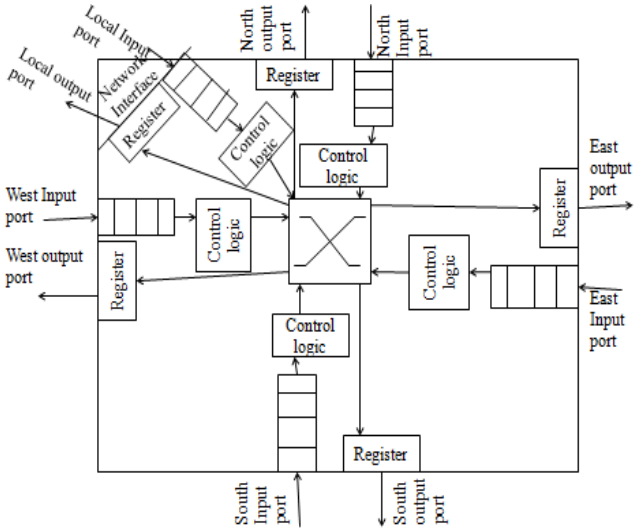

Figure1. Typical NoC router architecture.

In a typical NoC, each router has five input ports and five output ports corresponding to the north, east, south, and west directions as well as the local processing element (PE). Each port will connect to another port on the neighboring router via a set of physical interconnect wires (channels). The router's function is to route flits entering from each input port to an appropriate output port and then toward the final destinations. To realize this function, a router is equipped with an input buffer for each input port, a 5 × 5 crossbar switches to redirect traffic to the desired output port and necessary control logic to ensure correctness of routing results as shown in Figure1.

Usually, for each data packet, the corresponding head flit specifies its intended destination. After examining the head flit, the router control logic will determine which output direction to route all the subsequent (body and tail) flits associated with this data packet according to the routing algorithm applied.

B.Fault Tolerant NoC router architecture

Fault tolerant NoC router architecture is based on Backtracking wave pipeline Switch architecture [3].Fault tolerant NoC router is implemented with five bidirectional ports which are suitable to be employed in both Torus and Mesh topologies. There is no clock in this design and all of the data transmissions are put into action by the help of handshaking signals. A four-phased handshake protocol has been employed in this router [16]. Figure 2 shows Fault tolerant NoC router.

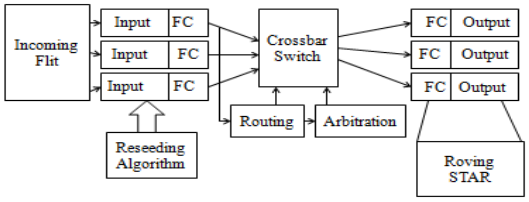

Figure 2.Fault Tolerant NoC router

The router consists of three main modules which are input buffer, crossbar switch, and routing unit. Input buffer is responsible to store temporarily incoming flits from adjacent routers whether it has free space. The capacity of input buffer in all five ports is five flits (one buffer is dedicated per port). Each input buffer contains a counter to determine the number of received flits in current packet. This counter is accessed by a subcomponent called header extractor which distinguishes header flit among others in a packet. Header processor is another sub-component of routing unit which is responsible to process the incoming packet's header.

Routing unit is the main component in this design. Routing process is implemented in this component once a new packet has been received. Each input channel can reserve one of output ports after routing process has been accomplished. An arbitration unit is utilized to dedicate the output port with round robin algorithm if there is more than one request for a special output channel. In other words, by the help of arbitration sub component output ports are distributed fairly through input ports. As soon as routing table set the switch links, the input port is connected to appropriate output port. The last component which is crossbar switch is in charge of connecting all input ports to each of output ones. The control signals of routing unit select one of output port for an incoming header flit.

A. *Reseeding Algorithm*

Reseeding algorithm is used to improve fault coverage in BIST pseudo-random testing [17]. Most of the work done on reseeding is based on storing the seeds in an external tester. Besides its high cost, testing using automatic test equipment (ATE) makes it hard to test the circuit in the system. Hence built-in reseeding [10] technique is used. This technique requires no storage for the seeds. The seeds are deterministic and encoded in hardware, so 100% fault coverage can be achieved. This technique causes no performance overhead and does not change the original circuit under test. Built-in reseeding is based on expanding every seed to as many ATPG patterns as possible. This is different from many existing reseeding techniques that expand every seed into a single ATPG pattern. An advantage of built in self test is its low cost compared to external testing using automatic test equipment(ATE)[17].In BIST,on-chip circuitry is included to provide test vectors and to analyse output response. Many digital circuits contain random- pattern-resistant (r.p.r) faults that limit the coverage of pseudo-random testing [17]. The r.p.r faults are faults with low detectability (Few patterns detect them). Several techniques have been suggested for enhancing the fault coverage achieved with BIST. These techniques use an additional bit counter and modifying circuit in which deterministic test cubes are embedded in the pseudo-random sequence of bits [8]. The modifying circuit is added at the serial output of the Linear Feedback Shift Register (LFSR) [10] to modify the pseudo- random bit sequence so that the useful patterns will be obtained.

Reseeding refers to loading the LFSR with a seed that expands into a pre computed test pattern. The operation of the reseeding circuit is as follows: the LFSR starts running in autonomous mode for sometime according to the reseeding algorithm. Once it is time for reseeding, a seed is loaded into the LFSR, which then goes back to the autonomous mode and so on and so forth until the desired coverage is achieved. The new seed is in the LFSR. By activating the select line of a multiplexer, the logic value in the corresponding LFSR stage is inverted.

In reseeding technique deterministic patterns are applied after a random testing to reduce number of the pattern. The deterministic pattern are loaded into the LFSR and then expended into the desire patterns in the scan chain. In this technique, random patterns that don't detect r.p.r faults are mapped to ATPG generated cubes through combinational logic. The mapping is performed in two phases, the pseudo-random patterns are identified in the first step, and the ATPG cubes are loaded in the second step. In this, we loaded new seed by putting the LFSR in the state that precedes the seed value, so that at the next clock pulse, the new seed is in the LFSR, and the technique is based on deterministic seeds which expand into ATPG patterns so 100% fault coverage can be achieved. The algorithm is based on the following strategies: (1) generate ATPG patterns for faults that were not detected with pseudo-random patterns and calculate seeds for these patterns, (2) when a seed is loaded into the LFSR, let the LFSR run in autonomous mode for sometime because there is a chance that some of the ATPG patterns will drop more faults so that some of the ATPG patterns are not needed, (3) as long as pseudo-random patterns don't detect faults, the LFSR should be loaded with a

new pattern. This technique is based on deterministic seeds which expand into ATPG patterns so high fault coverage can be achieved and reduced the test length.

B. Roving STAR Approach

Usually testing takes place within the roving STARs while the system continues operation in the remaining portions of the FPGA. Initially Lucent ORCA 2C series FPGA is used for the design and implementation of the BIST and diagnosis; but now this technique is emphasized and can be applied to any FPGA that features incremental RTR, such as the Xilinx Virtex series FPGA.

In the normal operations of FPGAs, as different functions will be configured to FPGAs and the configured logic will be lost when FPGAs are power off, an external module outside of FPGA is used to implement the reconfiguration process. Such kind of controller is typically an embedded microprocessor or microcontroller. It has some memory or uses extra memory, e.g., ROM, EEPROM, to store the configurations for not only the application functions, but in Roving STARs extended to the test and diagnosis functions. So this processor is also referred as Test and Reconfiguration Controller (TREC) [18]. TREC not only controls the normal operation of FPGAs, but also can access to BISTERs for testing and diagnosing. If faults are detected, TREC starts the diagnosis process e.g., if a fault exists and located, when the same part is going to be test next time, the TREC can skip it or test it functionally as partially usable block (PUB), in case of functional testing. When the normal configurations come across faulty CLBs or interconnect, TREC determines to bypass the defective resources or replace them with fault-free ones.

1. Roving STARs Structure

Based on the structure of STAR, Roving STAR[19] takes two columns of CLBs to form a vertical STAR (V-STAR) and two rows of CLBs to form a horizontal STAR (H-STAR), as well as the interconnect connected with these CLBs. The even number of column or row is for the symmetric consideration. So when testing the CLBs in the STAR, the interconnect is tested as well. Fig 3(a). gives an initial position of STARs. The reason to use two STARs – V-STAR and H-STAR – is that, as the global interconnect is usually spread into both the vertical and horizontal direction, both the V-STAR and H-STAR must be used at the same time to test and diagnosis. They also provide essential features for diagnosis, we will see in adaptive diagnosis techniques, and for testing procedure at the presence of previously located faults.

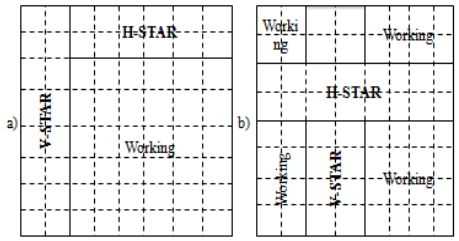

Figure.3.Roving STARs: (a) Initial Position and (b) During Roving

A roving step involves relocating a slice of the system logic adjacent to the STAR in the current STAR position and recreating the STAR logic in the area vacated by the system logic. This is illustrated in Figure.3 (b), after one roving step across of the V-STAR and one roving step down of the H-STAR; meanwhile the previous STAR areas are used for system logic.

After finishing the first sweeping, roving changes to the opposite direction, i.e., left→right, up→down, right→left, down→up. Following this step, one full horizontal sweep of V-STAR and one full vertical seep of H-STAR are needed to test the entire FPGA. For an *N*N* FPGA, a full sweep of one STAR requires *N/2* positions; thus, the total number of roving positions is *N*. The roving process is based on run-time reconfiguration and it is controlled by TREC.Besides with the above mentioned algorithm, this paper also addresses hybrid algorithm which is a combination of new energy efficient fault tolerant algorithm [20] and new resilient fault tolerant algorithm [21] to provide better fault coverage and performance than reseeding and roving star .

IV. N-DETECT TEST RELAXATION

N-detect test relaxation technique is mainly used to reduce the test time because; it takes very less test patterns to detect faults. Thereby it increases performance and power reduction. The effectiveness of physically-aware N-detect (PAN-detect) [22] test in detecting defects affecting modern designs has been demonstrated using both defect simulation and in-production ASICs. The applicability of a PAN-detect test set can be further improved by employing test relaxation. Test relaxation is a process of converting a fully-specified test set to a partially-specified (relaxed) one with as many unspecified test-input values as possible. The benefit of performing test relaxation comes from the flexibility of reassigning the unspecified test input values for (1) test compression, (2) reducing power incurred during scan test, (3) embedding tests to detect targeted faults more often, and (4) enriching tests to target other fault models. Yen-Tzu Lin, Emeka Ezekwe and Shawn Blanton have developed a physically-aware test relaxation (PATR) software, where

information collected in test generation or fault simulation is exploited for systematically identifying test-inputs that can be left unspecified (i.e., changed to a don't care value). The quality of the relaxed test set is ensured by maintaining the PAN-detect coverage of the original test sets.

V. SIMULATION RESULT

Because Simulation result of the proposed fault tolerance for NoC is presented in the form of timing diagram in fig.4 and fig.5.

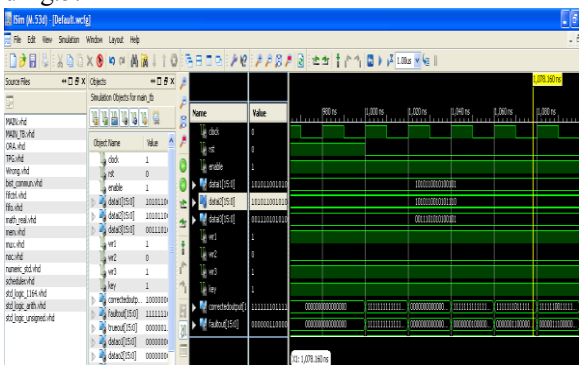

Figure 4:Main output

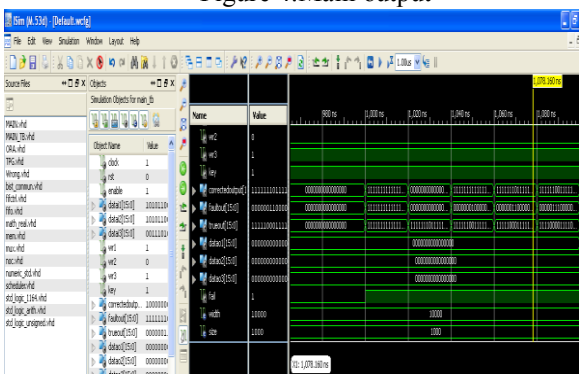

Figure 5: Main output

It is obtained using Xilinx version 12.1.In Fig.4 and Fig.5 Main output has been obtained with the input of clk, reset, enable, data_input. Main block is a combination of two sub blocks NoC and BIST. NoC contains three sub modules such as Register (DEMUX), FIFO and Scheduler.BIST contains three sub blocks such as Test pattern generator which is used to produce trueoutput.The second block called Circuit under test is mainly used to produce fault output from trueouput. The last and final block of BIST is Output response analyzer (ORA) which is used to generate corrected output from fault output. The input data_in is 16 bit and Test pattern generator will produce test pattern when reset becomes zero. Thus proposed algorithm produces corrected output from faulty input.

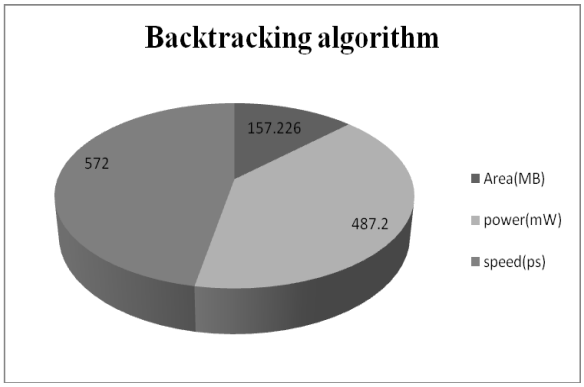

Figure 6: Area ,power and speed analysis of Existing system

In this work, device utilization plays a major role because it will determine area and power consumption of the project. Figure 6 shows the Area, power and speed analysis of existing backtracking algorithm in pie chart.

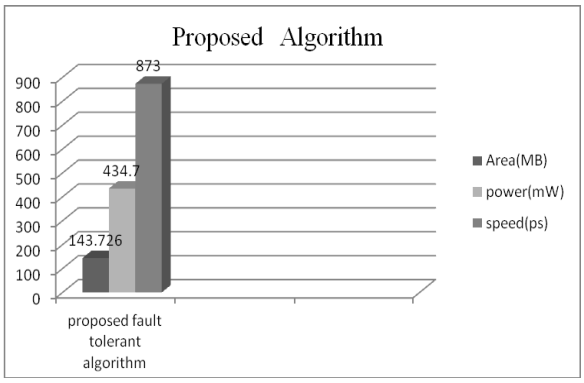

Figure 7:Area,power and speed analysis

Please Figure 7 presents proposed algorithm analysis under three main constraints such area,power and speed.Experimental result of this work shows the proposed algorithm gives better result when compared with the backtracking algorithm.Hence proposed algorithm provide high performance than the Existing system based on the above mentioned three constraints.

VI. CONCLUSION

This paper has presented Fault tolerance and cost-effective design of NoC to support guaranteed throughput, power consumption and reduces area. The proposed design of NoC is completely implemented in Virtex-6 FPGA.The Virtex-6 family consumes 15% less power and has improved performance over other Xilinx family. The first section of this work deals with two techniques such as reseeding and roving STAR to determine the faults in NoC. These techniques provide good fault coverage but it takes more time for testing the entire system. So the project presents a new technique and hybrid algorithm to reduce the test time. Hence the performance and the fault coverage are improved tremendously.

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