A NOVEL APPROACH FOR DESIGNING A D-FLIP FLOP USING MTCMOS TECHNIQUE FOR REDUCING POWER CONSUMPTION

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Abstract

Power consumption is a major bottleneck of system performance. A large portion of the on chip power is consumed by the clock system. It is made of the any integrated circuit, clock distribution network and flop-flops. A new system will considerably reduce the number of transistor it will lead to the reduction in clocking power and also improve the overall power consumption. Various design techniques used for a low power clocking system. Among those techniques Clocked Pair Shared Flip Flop(CPSFF) consume least power than Conditional Data Mapping Flip-Flop(CDMFF), Conditional Discharge Flip Flop(CDFF) and Conventional double Edge Triggered Flip-Flop (DEFF). A proposed novel Clocked Pair Shared Flip-Flop(CPSFF) using Multi-Threshold voltage CMOS(MTCMOS) technique which reduces the power consumption approximately by 20% to 90% than the original CPSFF. Simulation using Tanner Tool version 13.00 with 250 nanometer technology. The power consumption is calculated by T Spice. The proposed work clock pair shared flip flop using MTCMOS technique is more efficient than all other designs.

Key words- MTCMOS technique, integrated circuit, CPSFF, CDMFF ,CDFF, DEFF, power delay.

I. INTRODUCTION

To optimize the power consumption, many low-power design techniques have been introduced, such as clock gating, power gating, creating multi-supply-voltage designs, dynamic voltage frequency scaling, and minimizing clock network. Among these techniques, minimizing clock network is very important in reducing power consumption of a SoC. Power has become a big issue in modern VLSI design.

Flip-Flop is an electronic circuit that is used to store a logical state of any data input signals with the response to a clock pulse. Flip-flops are widely used to receive and maintain data in selected sequences during recurring clock intervals for a limited time period sufficient for other circuits within a system. A huge portion of the on-chip power is consumed by clock systems, which consists of timing elements such as flipflops, latches and clock distribution network. These clock systems have redundant transition and the transition probability of the clock is 100% while an ordinary logic has one-third on average so clock systems are one of the most power consuming components in a VLSI system .These components consume 30% to 60% of the total power dissipation in 2.1a system Consequently, reduction in the power consumed by flip-flops will show a deep impact on the total power consumed. Several techniques as well as various flip-flops have been proposed recently to reduce redundancy in clock system. There are many flip-flops given in the literature.

II. RELATED WORKS

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A. Double edge triggered flip flop(DEFF)

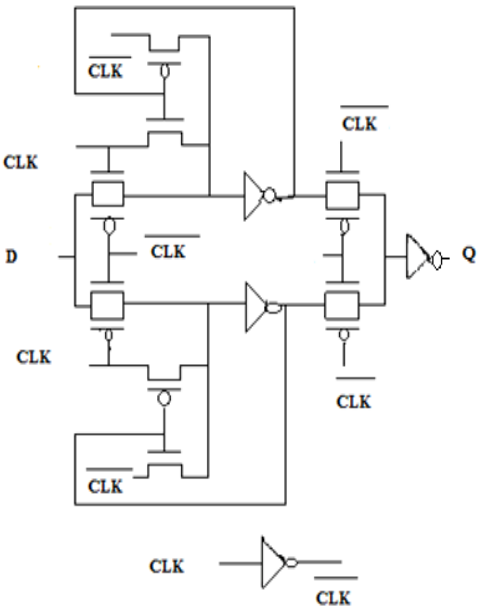

Figure 1.1 Double edge triggered flip flop

Figure 1.1 shows that double edge triggered flip flop. Data sampling is done on both the rising and the falling edge of the clock signals by Double Edge triggered Flip Flop (DEFF)[1]. It has the same number of transistors as that of the conventional Single Edge triggered Flip-Flop (SEFF) . Reduction of the frequency to half in case of DEFF results in abatement of the power dissipation to approximately half of the value of SEFF.

B. Conditional discharge flip-flop(CDFF)

Figure 1.2 shows that the conditional discharge flip flop. CDFF operates in two stages. The first stage is mainly for the LOW to HIGH transition, and the second stage for HIGH to LOW transition.

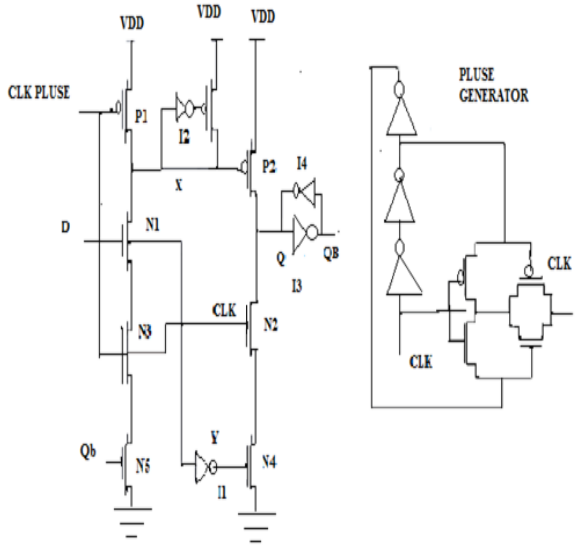

Figure 1.2 Conditional discharge flip-flop

CDFF uses a pulse generator which eventually generates the pulses for implementing the circuit in double edge triggered technology. The discharge path of the first stage helps in preventing evaluation in the coming clock cycles as long as input remain stable level '1'

C. Conditional Data Mapping Flip Flop(CDMFF)

Figure 1.3 shows that the conditional data mapping flip flop. CDMFF uses only 7 clocked transistors .when compare with CDFF which uses 13clocked transistors [2] resulting in reduction of the power consumption. The conditional data mapping (CDM) methodology exploits the property of the flip-flop, by providing the flip-flop with a stage to map its inputs to (0, 0) if a redundant event is predicted, such that the outputs will be unchanged when clock signal is triggered. The CDMFF has the floating node problem. The input for conditional data mapping flip flop is D and clock, and the output is Q.

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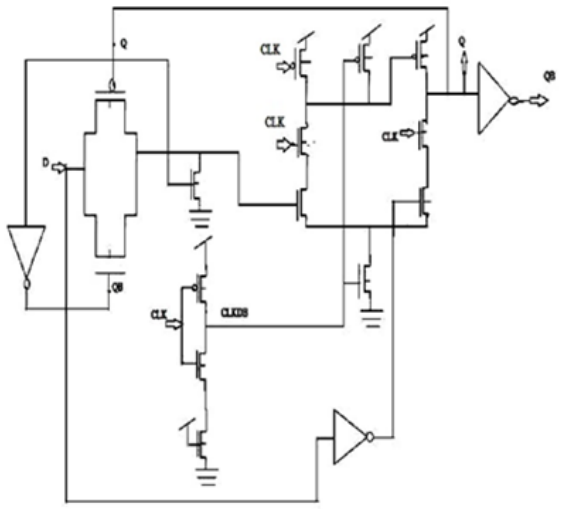

Figure 1.3 Conditional Data Mapping Flip-Flop

D. Clocked Pair Shared Flip Flop(CPSFF)

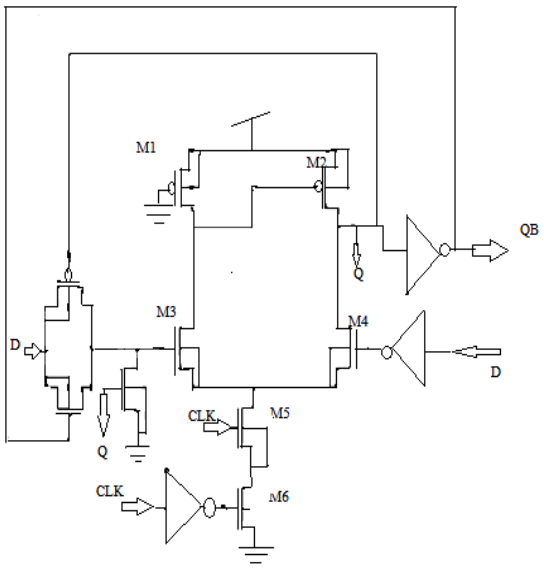

Figure 1.4 Clocked Pair Shared Flip-Flop

Figure 1.4 shows that the clocked pair shared flip flop. The CPSFF overcomes the problem of floating node in CDMFF by reducing the number of clocked transistors. CPSFF uses 4 clocked transistors while comparing with CDMFF which uses 7 clocked transistors shown in Figure (1.3). Hence reducing the clock load. In CPSFF the clocked pair is shared by the first and second stage. The always on pMOS in CPSFF allows the internal node to be always connected to Vdd thus prevents the floating problem. Thus in terms of power consumption of clock circuit CPSFF is high efficient than CDMFF.

III.PROPOSED SYSTEM

The main focus of this work is on minimizing the power consumption in any internal circuit. So that multi threshold CMOS (MTCMOS) technique is used with the clocked pair shared flip flop for reducing the power consumption.

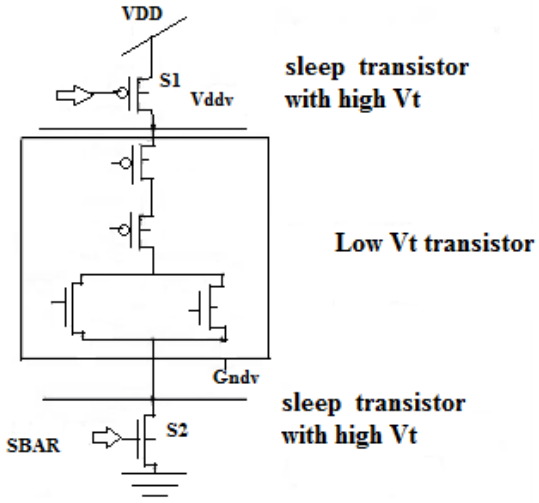

Figure 1.5 Power gating technique using MTCMOS.

The figure 1,5 shows that the power gating technique using MTCMOS. The diagram consists of two sleep transistors S1 and S2 with higher V. The logic circuit between the S1 and S2 is not directly connected to real supply lines V_{dd} and $G_{nd.}$ but in turn it is connected to virtual power supply lines Vdd v and Gnd v and has low V. Both the sleep transistors are given complementary inputs S and SBAR. The circuit operates in two modes active mode and standby mode. In active mode, S=0 and SBAR=1 such that S1 and S2 are ON and virtual supply lines Vdd and Gnd work as real supply lines therefore the logic circuit operates normally and at t higher speed.

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In sleep mode, S=1 and SBAR=0 such that S1 And S2 are OFF and this will cause virtual power supply lines to float and large leakage current present in circuit is suppressed by sleep transistors S1 and S2 resulting in lower leakage current and thus reducing power consumption.

The figure 1.6 shows that the schematic diagram of CPSFF using MTCMOS technique[3]. The flip flop works, when both clk and clkdb are at logic '1'. Pseudo nMOS and conditional mapping technique both are combined using the above scheme. The nMOS M3 is controlled by a feedback signal. For input D=1and S=1,Q will be high, switching ON the transistor M8, and turning OFF M3 thus parrying redundant switching activity and flow of short- circuit current at the node X.

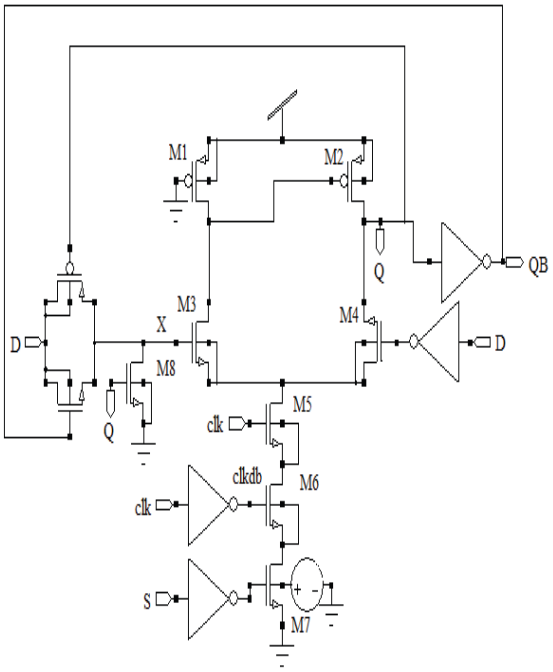

Figure1.6 Schematic of Proposed CPSFF using MTCMOS.

When D transits to 1 the output Q is pulled up by pMOS M2 whereas M4 is used to pull down Q when D=0 and Y=1 at the arrival of clock pulse. When the input D transits from 0-1 the short-circuit occurs for once even though M1 is always ON, thus disconnecting the discharge path and turning off M3 after two gates delay by feedback signal. There will be no short-circuiting even if the input D stays high as M3 disconnects the discharge path. The output of the flip flop depends upon the state previously acquired by Q and QB along with the clock and the data signal inputs provided.

IV. RESULT ANALYSIS

The below table is shows the power analysis for various flip flop. The inputs are 1.5v, 3.3v and 5v.which is calculated in watts. The power analysis is calculated in different temperature. While comparing the various flip flop like, DEFF, CDFF, CMFF,CPSFF,MTCPSFF. The MTCPSFF consume least power then the other flip flop. Table 1 Comparison of power analysis for D-flip-flops.

The MTCPSFF waveform is shown below, D is the input and Q is the output, clock is also the input.

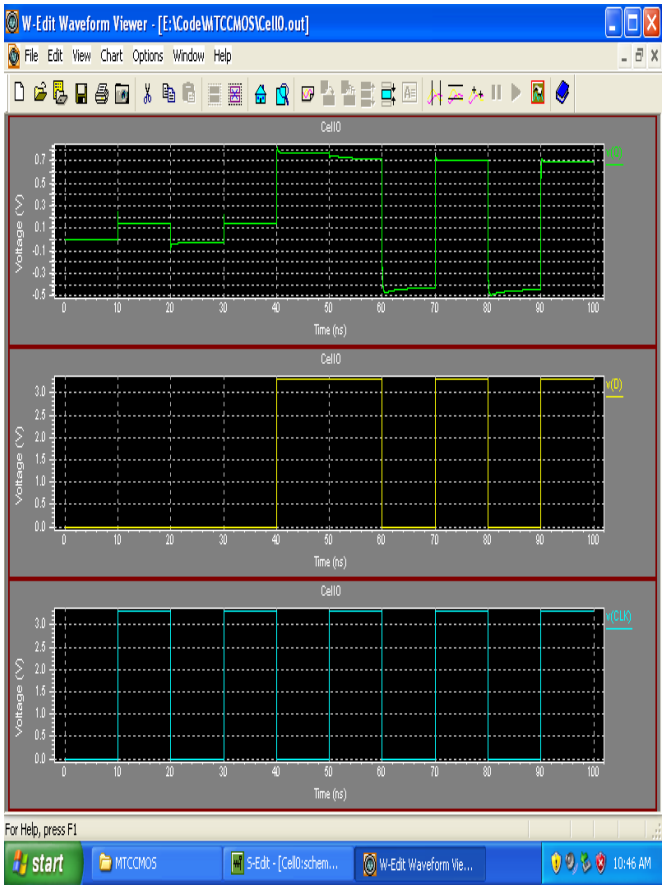

Figure 5.5 Output waveform of MTCPSFF

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Table 1.1 Power analysis

Design name	Temperature = 25 C			27 C		
	Power consumption (in watts)					
	1.5v	3.3v	5v	1.5v	3.3v	5v
CDFF	$3.309x10^{-004}$	$3.293 x10^{-003}$	$8.684 x10^{-004}$	$3.281 x10^{-004}$	$3.279 x10^{-003}$	$8.658 x10^{-003}$
DEFF	$2.439 x10^{-004}$	$2.950 x10^{-003}$	$9.097 x10^{-003}$	$2.418 x10^{-003}$	$2.935 x10^{-003}$	$9.054 x10^{-003}$
CDMFF	$2.551 x10^{-005}$	$9.741 x10^{-004}$	$5.058 x10^{-003}$	$2.558 x10^{-005}$	$9.788 x10^{-004}$	$5.028 x10^{-003}$
CPSFF	$3.069 x10^{-006}$	$3.071 x10^{-006}$	$9.472 x10^{-004}$	$2.308 x10^{-004}$	$2.290 x10^{-004}$	$9.423 x10^{-004}$
MTCMOS	$1.842 x10^{-008}$	$2.227 x10^{-008}$	$8.728 x10^{-008}$	$1.832 x10^{-008}$	$2.226 x10^{-008}$	$9.00 x10^{-008}$

V.CONCLUSION

The existing clocked pair shared flip flop using MTCMOS reduces local clock transistor number and power consumption as well. The proposed MT-CPSFF has given better result than the previously existing DEFF, CDFF, CDMFF and CPSFF in terms of power and good output response by approximately 20% to 90%. Furthermore, several low power techniques, including Forced stack technique, can be explored to incorporate into the new flip-flop to build system.

VII. FUTURE ENHANCEMENT

The work will be extended by using Forced stack technique for reducing power consumption in D flip-flop and can be implemented in any one of the applications. Further the work can be extended in reducing the number of transistors in MTCMOS Clock Pair Shared Flip-flop.

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