Design and Analysis of Low-Power Subtractor Circuits using P-XOR Logic Gates with Sleep Approach

Ms. Varsha Rani Tamrakar, Mr. Alok Kumar

Abstract— **In this paper we have presented the design of a low-power full subtractor circuit using P-XOR/ G-XNOR pass transistors logic gates. The main aim of designing the low power full subtractor circuit is the increasing circuit's complexity and demand of portable devices. Full subtractor circuit is one of the main components of most of the arithmetic and logic circuits. Full subtractor circuit is implemented using one or more XOR/ XNOR gates which consume the large part of the energy. The main objective of the work is to reduce the power of the circuit either by reducing the number of XOR/ XNOR gate or by using P-XOR/ G-XNOR logic gates which consumes less power in comparison with the conventional XOR/ XNOR gates.**

Key-words: Arithmetic and Logic circuits, Conventional XOR/ XNOR gates, Full subtractor, Low power, Powerless (P)-XOR/ Groundless (G)-XNOR gates.

I. INTRODUCTION

In the past, the main concern for the designers of the VLSI circuits was the area, performance and reliability of the design. But during the recent years, as the demand for the portable devices have gained importance, the main concern for the designers is the power, comparable to the area and speed considerations. The low power VLSI designs are of much interest in the recent years, concerning the demand for long battery life in portable devices and high heat removal in non-portable devices.

The problem for low power VLSI design can be broadly classified into two major categories: Analysis and Optimization. Analysis is concerned to be the accurate estimation of the power or energy dissipation during the different designing phase of the circuit. Analysis techniques differ in their accuracy and efficiency. The accuracy of analysis depends on information available to design a particular design. Optimization is the process of generating the best design, given an optimization goal, without violating design specifications.

The interests in low power chips and systems are driven by both business and technical needs. The industry for low power consumer electronic products is booming with a rapidly expanding market. At the same time, current generations of semiconductor processing technologies present more rigorous requirements to the power distribution of digital chips due to increased device density, speed and complexity.

The conventional full subtractor circuit requires 38 transistors and conventional half subtractor circuit requires 16 transistors for its designing as shown in the figure. The main aim of this paper is to reduce the area and the power dissipation of these circuits using different methods.

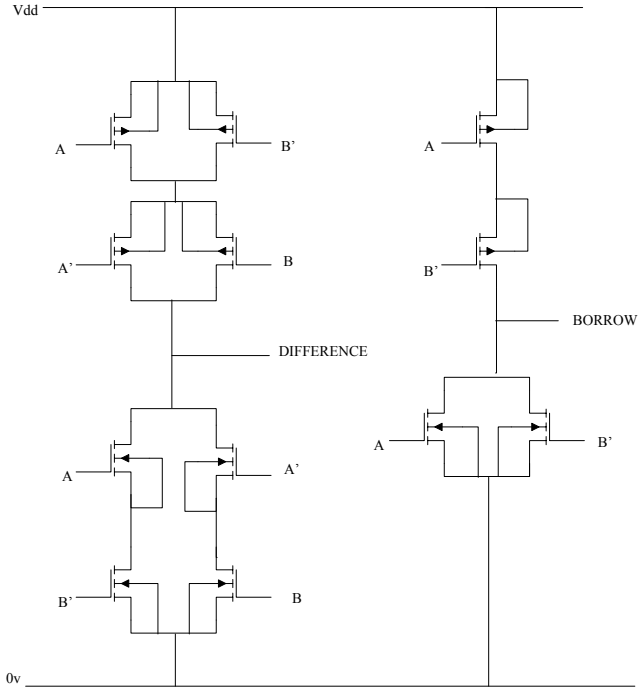

Figure 1: Conventional Half Subtractor

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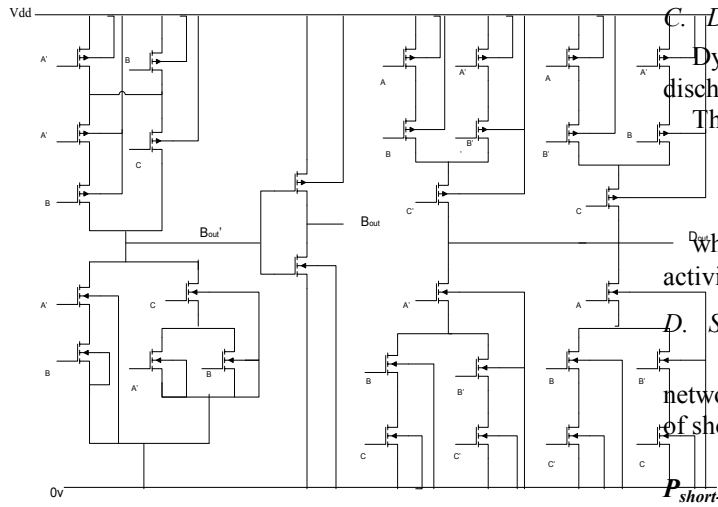

Figure 2: Conventional Full Subtractor

I. EASE OF USE

The development of digital integrated circuits is challenged by higher power consumption. The combination of higher clock speeds, greater functional integration, and smaller process geometries has contributed to considerable growth in power density. Scaling helps to increase speed and frequency of operation and hence higher performance.

Leakage power has become a serious concern in nanometer CMOS technologies. Nowadays, leakage power has become a progressively more important issue in processor hardware and software design.

A. Power Dissipation

Power is defined as the rate at which the energy is transferred or exchanged in the circuit. Power dissipation in the circuit is defined as the rate at which the energy is taken from source and is converted to heat.

Advances in CMOS fabrication technology double the number of transistor per chip every two years and double the operating frequency every three years. Consequently, the power dissipation per unit area grows, increasing the chip temperature. This excessive temperature reduces the reliability and lifetime of the circuit. Hence, large cooling device and expensive packaging are required to dissipate the extra heat.

B. Sources of Power Dissipation

For the most recent CMOS feature sizes, leakage power dissipation has become an overriding concern for VLSI circuit designers. International technology roadmap for semiconductors (ITRS) reports that leakage power dissipation may come to dominate total power consumption. There are three sources of power dissipation in CMOS digital circuits: dynamic power, short circuit power and leakage power. Formerly, the dynamic power was dominant and the other two parts were negligible. But leakage power is becoming more and more significant as the CMOS technology goes into the deep submicron scale. Now, all three are important and leakage power is beginning to dominate.

C. Dynamic Power

Dynamic power is the powers required to charge and discharge the load capacitances when transistors switch.

The formula for dynamic power is given by

$$P_{dynamic} = \propto C_L V_{DD}^2 f$$

where f is the clock frequency and is the node transition activity factor.

D. Short-Circuit Power Dissipation

When transistors switch, both nMOS and pMOS networks may be momentarily on at once. This leads to a blip of short circuit current. The short circuit power is given by:

$$P_{short\text{-}circuit} = I_{mean} V_{DD}$$

Where I_{mean} is average short-circuit current. For a symmetric inverter.

$$I_{mean} = \frac{\beta}{12}(V_{DD} - 2V_t)^3 \quad [1]$$

E. Leakage Power

Leakage power, also called static power, is due to the off-state current of a transistor when it is off. Suppose that there are N transistors in a circuit, and I_{offi} is the off-state current of the i_{th} transistor. Then, the total leakage power of the circuit can be expressed in the following formula:

$$Pleakage = V_{DD} \sum_{i=1}^{N} I_{offi}$$

II. NEED OF LOW-POWER FULL SUBTRACTOR

Basic building blocks of most of the arithmetic and logic circuits are formed by XOR-XNOR gates. Full subtractors are the basic block of many circuits. Therefore reducing power consumption in full subtractor is very important in low power circuits. One of the most power consuming modules in full subtractor is XOR/XNOR circuit. The proposed logic approaches use one XOR or XNOR gate to implement a full subtractor. A full subtractor is one of the essential components in digital circuit design; many improvements have been made to reduce the architecture of a full subtractor.

The main aim of this is to reduce the power dissipation and area by reducing the number of transistors. In this, a novel design for the realization of full subtractor circuit is being proposed with significant area and power savings. One approach based on XOR-XNOR design full subtractor circuit in a single unit. Objective of this work is to investigate the power, delay and operational speed of the low voltage full subtractor cells in different CMOS logic styles.

III. TECHNIQUES FOR DESING LOW-POWER FULL SUBTRACTOR

The conventional full subtractor circuit has large area, large delay and higher power dissipation due to large number of transistors, as the conventional XOR gates consists of large number of transistors.

The algebraic expressions for XOR are as follows:

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$$A \cdot \overline{B} + \overline{A} \cdot B$$

The CMOS implementation for the conventional XOR gate is a follows:

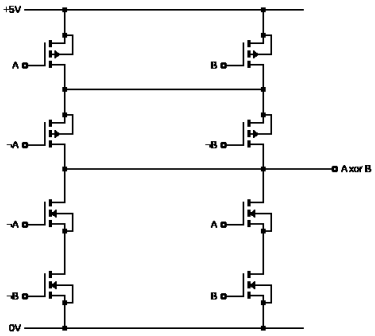

Figure 3: Conventional XOR Gate

The XNOR gate with inputs *A* and *B* implements the logical expression

$$A.B + \overline{A}.\overline{B}$$

The CMOS implementation for XNOR gate is:

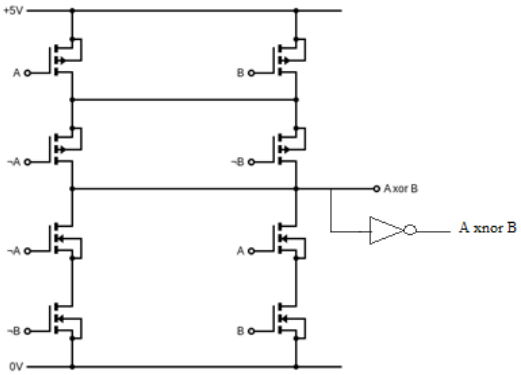

Figure 4: Conventional XNOR Gate

The P-XOR and G-XNOR consumes less power than other design because it has no power supply (VDD) or ground (VSS) connection. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications. The advantage of PTL is that only one PTL network (either NMOS or PMOS) is sufficient to perform the logic operation, which results in smaller number of transistors and smaller input loads, especially when NMOS network is used. Moreover, VDD-to-GND paths, which may lead to short-circuit energy dissipation, are eliminated.

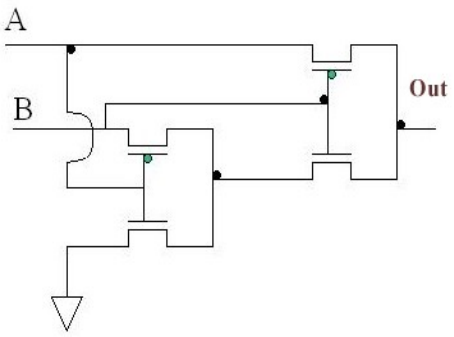

Figure 5: P-XOR Gate

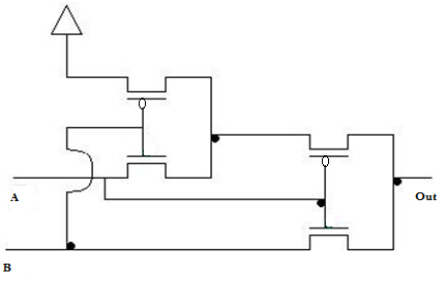

Figure 6: G-XNOR Gate

The P-XOR and G-XNOR consumes less power than other design because it has no power supply (*VDD*) or ground (*VSS*) connection. These circuits are unable to function properly at low supply voltage due to threshold loss at the output node and displayed poor delay characteristics.

IV. PREVIOUS WORKS DONE

The previous works done up to date is the designing of low-power full adder circuits with different techniques and are compared with different structures.

[2] proposed a technique to build a total of 41 new 10-transistors full adders using novel XOR and XNOR gates in combination with the existing ones. They have done over 10,000 HSPICE simulation runs of all the different adders in different input patterns, frequencies and load capacitances. Almost all those new adders consume less power in high frequencies, while three new adders consistently consume on average 10% less power and have higher speed compared with the previous 10-transistor full adder and the conventional 28-transistor CMOS adder. One drawback of the new adders is the threshold voltage loss of the pass transistors.

Based on the extensive simulations, it was concluded that the three new adders consumes on average 10% less power and have 90% higher speed compared to the previous 10-transistor adder.

[3] presented a performance analysis and evaluation of six different 1-bit full adder topologies in deep subthreshold operation. The cells are characterized with respect to delay, power consumption, driving capability, Power Delay product (PDP), Energy Delay Product (EDP) and maximum operating frequency. Both traditional CMOS, a specialized Low Power cell and minority-3 based Full Adders are simulated and characterized. PDPs of less than 200aJ are reported, for FA cells operating at frequencies around 2 MHz, for V_{DD} = 200 mV, dissipating less than 100 nW of average power.

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[4] proposed a novel approach based on XOR/XNOR design full adder circuits in a single unit was proposed. The objective of their work was to investigate the power, delay and power delay product of the low voltage full adder cells in different CMOS logic styles. Simulation results illustrate the superiority of the proposed adder circuit against the conventional CMOS, Hybrid, Bridge, XOR/XNOR adder circuits in terms of power, delay, PDP. The bridge style enjoys a high degree of regularity, higher density than conventional CMOS design style as well as lower power consumption by using some transistors named bridge transistors. Simulation result reveal that the proposed circuit exhibits lower PDP and is faster compared with the available 1-bit full adder circuits.

V. METHODOLOGY

The Methodology used in designing the project will be accomplished in two parts:

1. Designing and analysing of Half Subtractor Circuit.
2. Designing and analysing of Full Subtractor Circuit.

A. DESINGING OF THE HALF SUBTRACTOR CIRCUIT

The conventional Half Subtractor Circuit will be designed using the sleep approach and will be compared with the conventional Half Subtractor for the result.

Later, the circuit will be re-designed using the P-XOR Logic Gate and with the Sleep approach to get the better result than before.

The Conventional Half Subtractor which has to be analyzed is shown below:

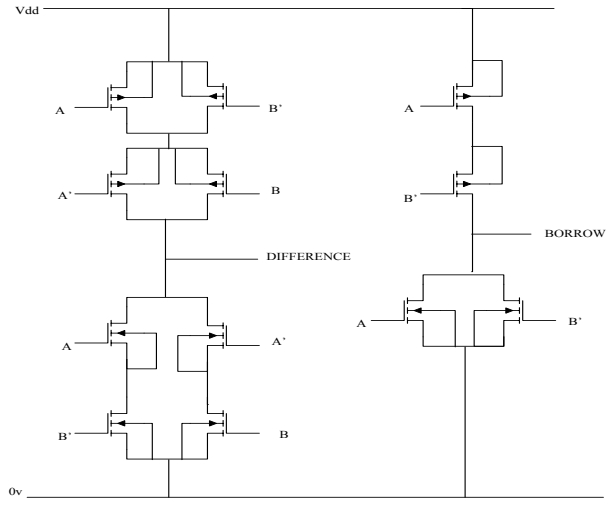

Figure 7: Conventional Half Subtractor

B. DESIGNING AND ANALYSING FULL SUBTRACTORCIRCUIT

The process for designing the Full Subtractor circuit is exactly the same as that of the Half Subtractor circuit. The only difference in the analysis of the Full Subtractor circuit is that, the Full subtractor will be designed using P-XOR/G-XNOR logic gates, sleep approach and also designed using the half subtractor circuit to analyze it for the better outcome and better performance of the conventional Full Subtractor circuit which is one of the main component of the Arithmetic and Logic Unit (ALU) of all the electronic devices.

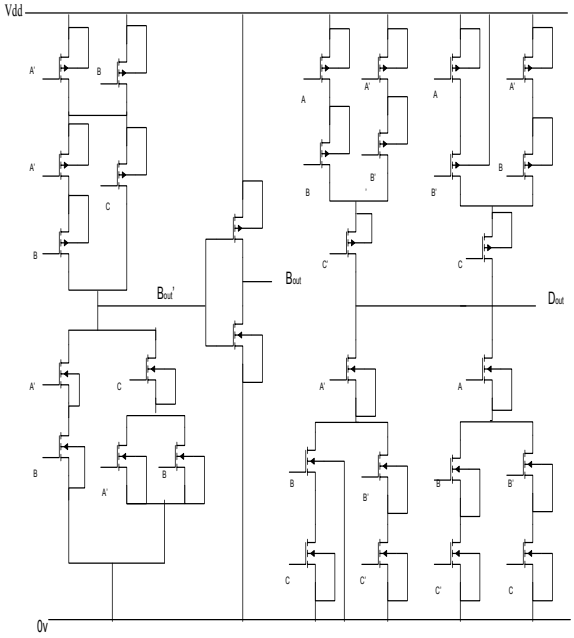

Figure 8: Conventional Full Subtractor

VI. RESULT AND DISSCUSSION

A. HALF SUBTRACTOR

The conventional Half Subtractor circuit is designed using the Sleep Approach, P-XOR Logic Gate and with the Sleep techniques, the following result is obtained.

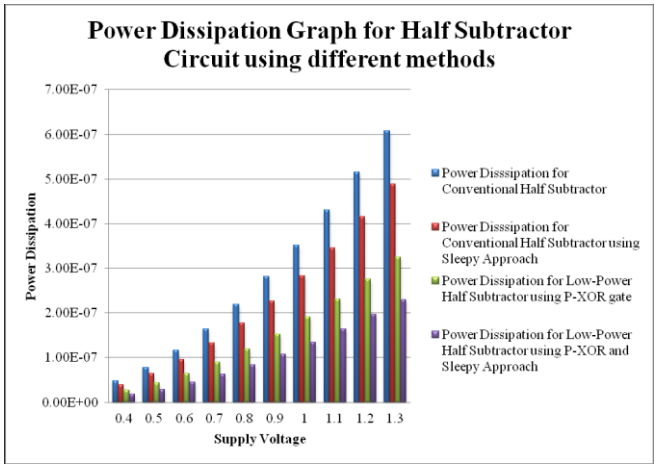

Figure 9: Result for Half Subtractor

B. FULL SUBTRACTOR

The Full Subtractor circuit is also one of the main components of most of the electronic devices whose performance has also to be improved. Using the same methods used in analyzing the Half Subtractor is also implemented in the Full Subtractor and the following result is obtained.

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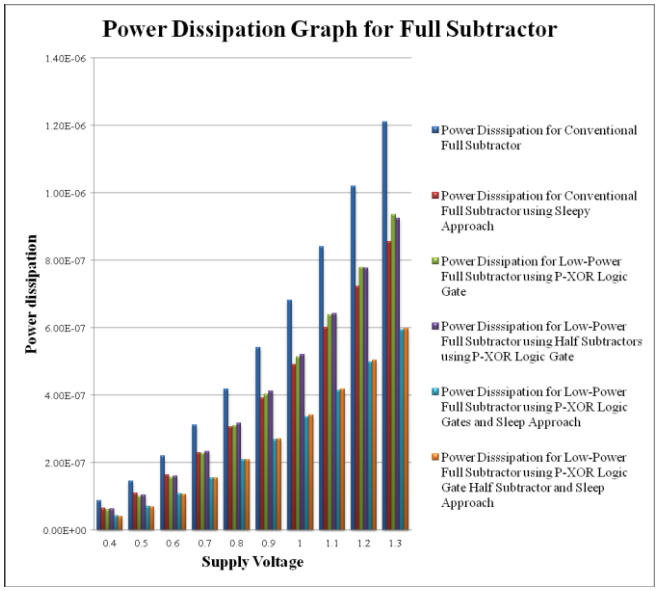

Figure 10: Result for Full Subtractor

VII. CONCLUSION

From the above results the following results have been drawn, which show that the Conventional Half Subtractor and the Conventional Full Subtractor Circuits can be implemented using the above techniques for the better performance of the circuits.

S. No.	***Methods Implemented***	***Conclusions with respect to Conventional Half Subtractor***			
		Elements (19)	***Nodes (12)***	***Number of Transistors used (16)***	***Percentage Reduction in Power Dissipation***
1	*Conventional using Sleep Approach*	21	14	18	18.92%
2	*Low-Power using P-XOR Logic Gates*	13	9	10	45.71%
3	*Low-Power using P-XOR Gates and Sleep Approach*	15	11	12	62.15%

Table 1: Concluding table for Half Subtractor

S. No.	***Methods Implemented***	***Conclusion with respect to Conventional Full Subtractor***			
		Elements (42)	***Nodes (27)***	***Number of Transistors used (38)***	***Percentage Reduction in Power Dissipation***
1	*Conventional using Sleep Approach*	44	29	40	27.09%
2	*Low-Power Full Subtractor using P-XOR Logic Gate*	26	16	22	25.86%
3	*Low-Power Full Subtractor using Half Subtractors using P-XOR Logic Gate*	30	18	26	25.08%
4	*Low-Power Full Subtractor using P-XOR Logic Gates and Sleep Approach*	32	20	28	50.85%
5	*Low-Power Full Subtractor using P-XOR Logic Gate Half Subtractor and Sleep Approach*	28	18	24	51.26%

Table 2: Conclusion for Full Subtractor

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