DECIMATION FILTER FOR MULTISTANDARD WIRELESS RECEIVER

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Abstract— **The demand for new telecommunication services requiring higher capacities, data rates and different operating modes have motivated the development of new generation multi-standard wireless receivers. A multi-standard design often involves extensive system level analysis and architectural partitioning, typically requiring extensive calculations. In this research, a decimation filter is designed for wireless communication multi-standards Consisting of GSM, WCDMA, and Wi-MAX is developed in MATLAB using GUIDE environment for visual analysis. The user can select a required wireless communication standard, and obtain the corresponding multi-stage decimation filter implementation using this design. Current radio frequency (RF) transceivers demand higher integration for low cost and low power operations, and adaptability to multiple communication standards. Specifically, software defined radio (SDR) is a wireless interface technology in which software-programmable hardware is used to provide flexible radio solutions in a single transceiver system.**

Keywords: Decimation filter, MATLAB, multi-standard wireless receiver.

I. Introduction

Current radio frequency (RF) transceivers demand higher integration for low cost and low power operations, and adaptability to multiple communication standards. Specifically in software defined radio is wireless interface technology in which software- programmable hardware is used to provide flexible radio solution in single transreceiver system. Multistandard operation is achieved by using a receiver architecture that performs channel selection on chip at baseband. This baseband channel filtering is performed in digital domain to adapt to the channel bandwidths, sampling rates, carrier to noise ratio, and blocking and interference profile of multiple communication standard. An expanding growth of wireless communications systems accomplish multitude of standard has been observed. More ever the competitive market imposes low cost and low power devices working with several standards. In order to assure the adaptability to different standards, digital signal processing is more advisable than analog processing. In the reception process, when analog to digital conversion are performed before channel selection, it cover severe specification due to strong adjacent channel blockers along with the desired signal because of high in band signal-to-noise ratio proposed by sigma delta converter , this kind of converter is currently included in transreceiver scheme. This oversampling based technique supposes the use of digital filter to prevent quantization noise aliasing during sampling decreasing .this decimation filter needs to perform both filtering of the out of band quantization noise and the adjacent channel blockers. It means that is required from the filter design to exhibits a high dynamic range, a programmable bandwidth to accommodate different standard, and precise tuning to select the desired channel within the standard.

This paper deals with the design of a decimation filter to be used in wideband radio frequency wireless .A decimation filter cascade structure is designed to meet the GSM,WCDMA, LANa, LANb, LANg and Wi-max standard specification

II RECEIVER ARCHITECTURE CONSIDERATION

This section deals with the receiver architecture

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which emphasizes high integration and multi-standard capability. A multistandard wireless system must meet the performance requirement for each standard and adjust to different channel bandwidth and carrier frequencies. Many receiver architecture architecture have been proposed: the conventional superheterdyne architecture . In this work direct conversion homodyne receiver architecture because it eliminate many off chip component. Fig 1 shows a direct conversion homodyne architecture which as an example of a receiver suitable for high integration and adaptability . it is also known as zero IF receiver. This architecture translates frequency to baseband directly to eliminate external component within the path. It can be program for a multistandard solution since the local oscillator is tuned to the same frequency as the incoming RF frequency to select different standard. On the other hand a dc offset created at the output of mixer. Here the incoming RF signal is multiplied by one sided LO signal band, and hence does not suffer from image signal interference. The down conversion with a one sided LO signal is achieved by a quadrature mixer in which the incoming signal is multiplied by two LO signals with 90 degrees out of phase. These in-phase and quadrature phase components are then low pass filtered and sent to ADCs. The digital signal from ADC is given to digital signal processing section for demodulation. Homodyne receivers are multi-standard capable because the channel filtering is done at baseband. However, the noise and DC offset are to be reduced to achieve adequate dynamic range. The sigma-delta ($\sum\Delta$) analog-to-digital converters (ADCs) are widely used in wireless systems because of their superior linearity, robustness to circuit imperfections, inherent resolution-bandwidth trade off and increased programmability in digital domain. A highly linear sigma-delta modulator for multi-standard operation that can achieve high resolution over a wide variety of bandwidth requirements remains challenging. A reconfigurable ADC is a promising solution to keep the power dissipation as low as possible.

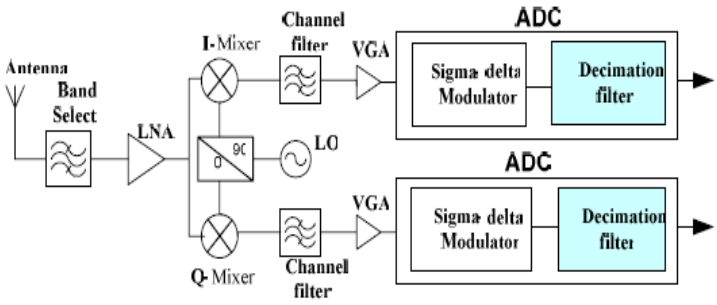

Fig. 1 Direct conversion homodyne receiver architecture

The theoretical dynamic range has been used in conjunction with the implementation attributes to choose the optimal topology for different RF standards. . The six popular standards considered in this paper are GSM, WCDMA, 802.11a, 802.11b, 802.11g and WiMAX. These standards have different bandwidth requirements. Since the bandwidth requirements of WLAN-a, b, g and Wi-MAX are more or less the same, the same topology can be adopted with different oversampling ratios (OSRs). This will reduce the DR calculation for the main three standards GSM, WCDMA and WLAN (Wireless Local Area Network) whose dynamic range requirements are chosen to be 94dB, 79dB and 69dB respectively.

III. FILTER STRUCTURE AND DESIGN

The performance of a decimation filter depends on the filter architecture and the order of each stage of multistage decimator. FIR filter are widely used in decimators as most of the modulation scheme require linear phase characteristics. The different filter architecture used in this work are as below.

A. filter architecture

1) Cascaded integrated comb (CIC) filter

Hogenauer deviced a flexible, multiplier free cascaded integrated comb (CIC) filter that can handle large sampling rate changes suitable for hardware implementation. The basic structure of hogenaur CIC filter is shown in figure 3. This consist of integrator and comb filter as two basic bulding blocks. So it is an infinite impulse response (IIR) filter followed by a finite impulse

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response (FIR) filter. In a CIC filter of order k , the integrator section consist of a cascade of k digital integrators operating at the high sampling rate fs. Each integrator is one-pole filter with unity feedback coefficient and the transfer function is

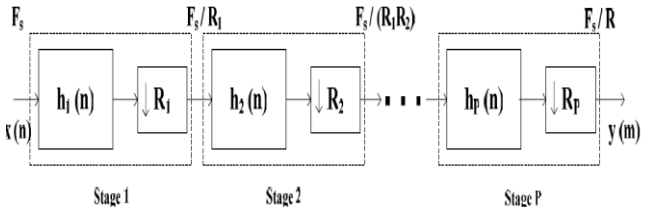
$$H_I(z) = \frac{1}{1 - z^{-1}}$$

The comb section consist of k comb stages with differential delay of M and operates at the low sampling rate fs/R, where R is the rate change or decimation factor. The transfer function of comb stage referenced to high sampling rate is

$$H_C(z) = 1 - z^{-RM}$$

The rate chnge swich between the two filter section subsamples the output of the integrator stage reducing the sample rate from fs to fs/R. in practice , the differential delay , m is usually held equal to 1 or 2. Using (3) and (4), the system transfer function of the CIC filter with respect to the high sampling rate fs is given by

$$H(z) = H_I^k(z) H_C^k(z) = \frac{\left(1 - z^{-RM}\right)^k}{\left(1 - z^{-1}\right)^k} = \left[\sum_{i=0}^{RM-1} z^{-i}\right]^k$$



2) Half band filter

Halfband filters are a special class of symmetric FIR filters used in second stage of multistage decimators. Half band filters are characterized by equal pass band and stop band ripples ($\delta_p = \delta_s$), and the transition band is symmetrical about $\pi/2$ such that $\omega_p + \omega_s = \pi$, where ω_p and ω_s correspond to the passband and stopband edges. The impulse response h(n) exhibits symmetry with almost 50% of coefficients 'zero' and with a magnitude of 0.5 at $F_s/4$. This implies reduced number of filter taps, lesser hardware and low power consumption.

3) FIR filter

The third type of filter used in multistage decimeter is FIR filter. The CIC filter response exhibits a droop in the passband which progressively attenuates the signals. The passband droop and stopband attenuation increases as the number of section of CIC filter increases. The FIR filter used in the last stage performs decimation and CIC droop compensation.

B].Decimation Filter Design Specification

The specifications for all six standards considered in this research and their corresponding decimation filter design parameters are given in Table I. The oversampling ratio (OSR) for each standard is selected so as to get the required dynamic range for the sigma-delta modulator of a particular order and number of quantizer bits. The receiver specifications and the blocking and interference profiles are defined first in order to set the parameters for the decimation filter. The decimation filter is generally designed to minimize the undesired signals in the desired band of operation. The output carrier to noise (C/N) ratio is calculated from the bit error rate (BER) of each standard and the modulation scheme used. Table II gives the interference profile and the C/N ratio for all the six standards. The passband frequency edge is taken as 80% of the bandwidth. The passband ripples are chosen to minimize signal distortions in the signal band. The stopband attenuations shown in Table I are selected according to the interference profile and C/N ratio given in Table II for each standard.

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TABLE I
MULTI-STANDARD SPECIFICATIONS AND DECIMATION FILTER DESIGN PARAMETERS

Standards	Frequency range (GHz)	Channel Spacing (MHz)	Symbol rate / Chip rate	OSR	Input sampling frequency, F_s (MHz)	Pass band edge (MHz)	Stop band edge (MHz)	Passband ripple (dB)	Stopband attenuation (dB)
GSM	DL:0.935-0.96 UL:0.89-0.915	0.2	270.833 Ksymbols/s	128	34.667	0.08	0.1	0.1	65
WCDMA	DL:2.11-2.17 UL:1.92-1.98	5	3.84 Mchips/s	16	61.44	2	2.5	0.5	55
WLANa	5.15-5.35	20	12 Msymbols/s	8	96	8	10	0.5	44
WLANb	2.4-2.4835	25	11 Mchips/s	12	132	10	12.5	0.5	42
WLANg	2.4-2.4835	25	12 Msymbols/s	12	144	10	12.5	0.5	44
WiMAX	10-66	20	16.704 Msymbols/s	8	133.632	8	10	0.5	39

TABLE II
INTERFERENCE PROFILE AND C/N RATIO

Standard	Offset from central frequency(MHz) : Interference magnitude(dBm)				C/N ratio (dB)
GSM	0.2 : -90	0.4 : -58	0.6 : -46	1 : -42	9.7
WCDMA	5 : -63	10 : -56	12.5:-44		7.2
WLANa	20 : -63	40 : -47			28
WLANb	25 : -35				7
WLANg	20 : -63	40 : -47			28
WiMAX	20 : -68	40 : -49			21

IV. Multistage decimation filter design

The toolbox is designed for six popular wireless communication standards, namely GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX. Initially, the desired standard is selected from the pop-up menu as in Fig. 8 and the filter design is obtained by pressing the push button named Multistandard Decimation Filter Design. The filter details such as the required channel spacing for a selected standard, passband edge, stopband edge, input sampling frequency, OSR, number of stages and type of filter used in each stage, decimation factors for each stage, and filter complexity are displayed on the GUI

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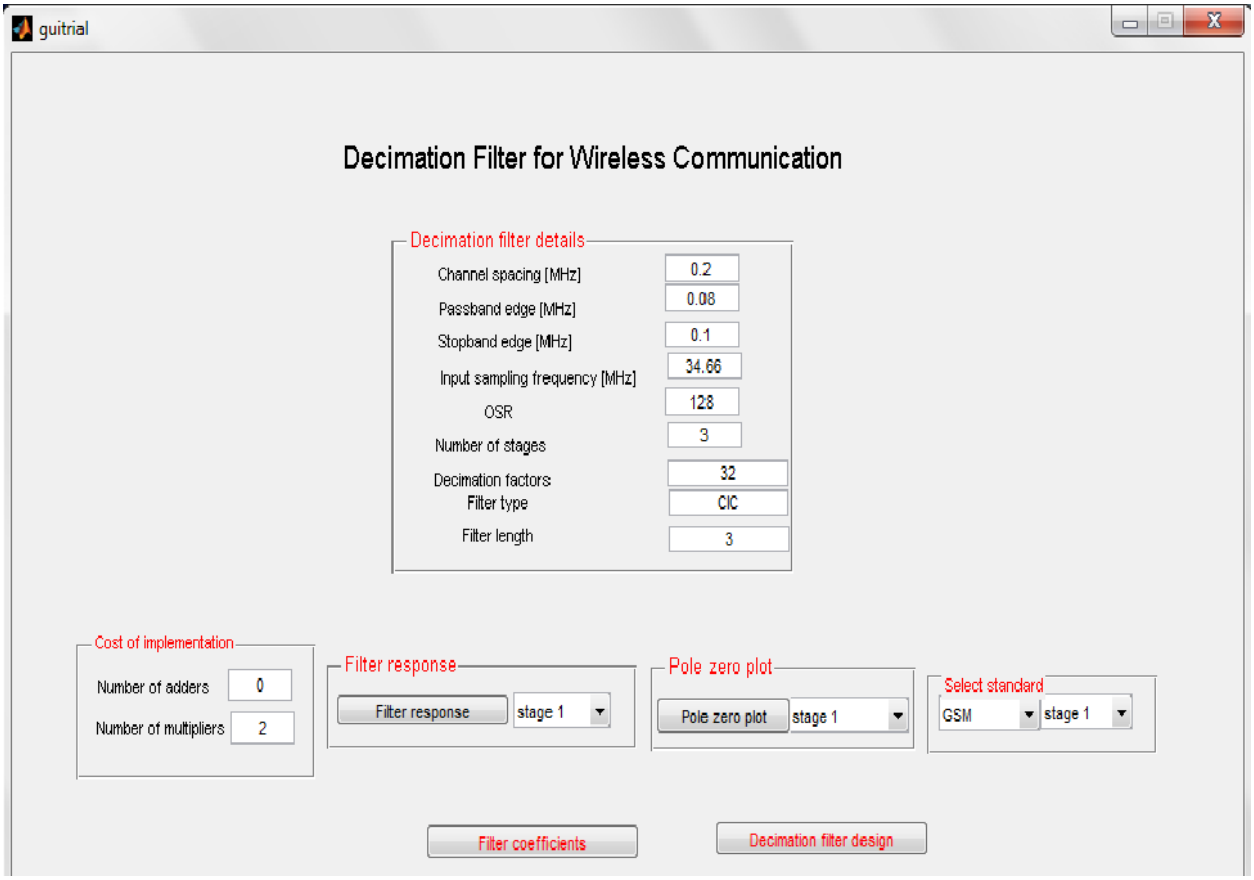
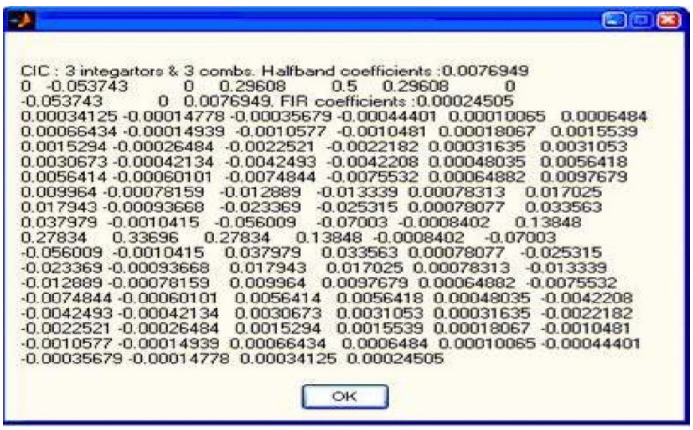


Fig.2 Decimation Filter Toolbox

A.Filter Co-efficient

The filter coefficients can be visualized by pressing the push button named Filter coefficient. Then a message box will pop up and it displays the filter coefficients for each stage. For GSM (current display), the message box displays the number of sections of the CIC filter as '3 integrators and 3 combs', 11 halfband filter coefficients and 101 droop compensation FIR filter coefficients



B.Filter Response

The push button named Filter response is used to display the magnitude response. The desired response such as the magnitude response for individual filter stages, cascaded responses after each stage or the multistage overall response, can be selected from the pop-up menu as in Fig. 2 The cascaded filter response and the overall response of the multistage decimator are displayed using filter visualization tool (FVTool) in MATLAB as in Fig. 3. The magnitude response of individual filter is displayed on the graphical window, called axes, embedded on the front panel of the GUI .

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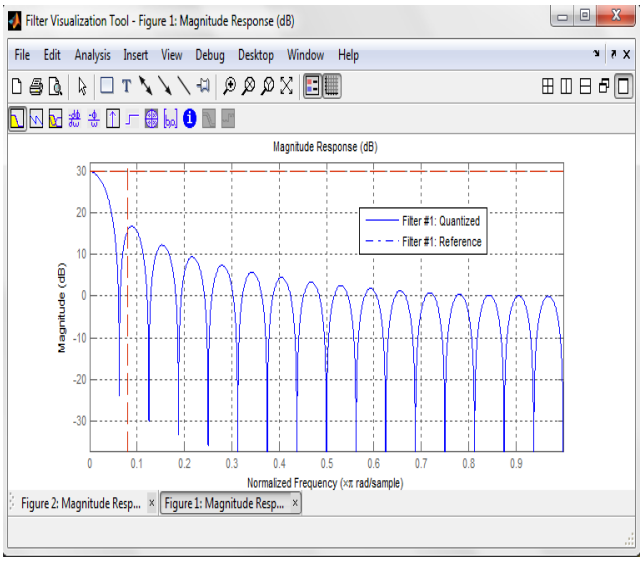
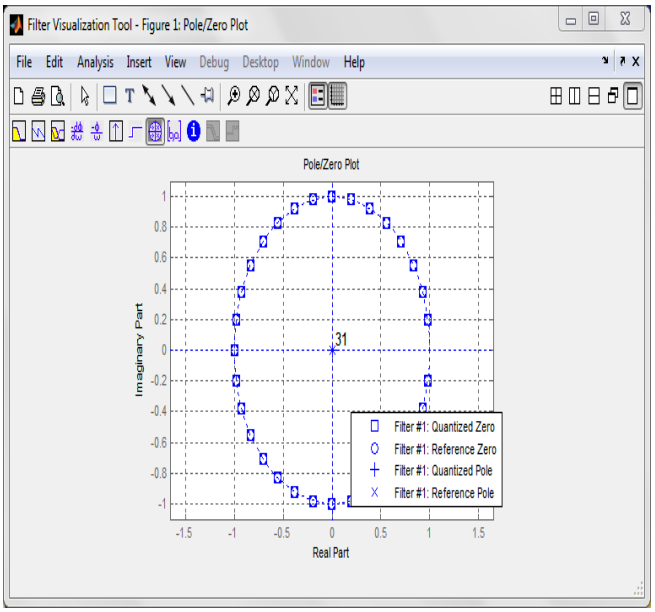


Fig.GSM stage 1filter response

C.Pole-Zero Plots

To get the pole-zero plot of individual filter, each stage can be selected from a pop-up menu as in Fig. 2 The push button named Pole-Zero Plot is used to display the corresponding plot on the front panel graphical window of the GUI .



V. CONCLUSION

This paper presents a toolbox for the design of multistage decimation filter for six popular wireless standards namely GSM, WCDMA, WLANa, WLANb, WLANg and WiMAX. The toolbox is developed using signal processing toolbox and filter design toolbox in MATLAB® using GUIDE environment. The user can select required wireless communication standard, and obtain the corresponding multistage decimation filter implementation using this toolbox. The toolbox will help the user or design engineer to perform a quick design and analysis of decimation filters for multiple standards without doing extensive calculation of the underlying methods. The tool provides the user with all necessary details of decimation filter designed for the selected standard including filter coefficients, frequency response, pole-zero plot etc.

REFERANCES

[1] F. Sheikh and S. Masud, "Efficient sample rate conversion for multistandard software defined radios", IEEE Int. Conf. on Acoustics, Speech and Signal Processing, Apr. 2007.

[2]"on design and implementation of decimation filter for Multistandard wireless transceiver" IEEE Int. conf,sep 2006.

[3]Shahana T.K.,Babita R.JOSE,"Decimation filter design toolbox for multistandard wireless transceivers using MATLAB.May 2009.

[4]Ze Tao and S. Signell, "Multi-standard delta-sigma decimation filter design", IEEE Asia Pacific Conference on Circuits and Systems Singapore, pp. 1212-1215, Dec. 2006.

[5]M. Kim and S. Lee, "Design of dual-mode digital down converter for WCDMA and cdma2000", ETRI Journal, Vol.26, No.6

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