A novel approach towards the design of self clocked D flip-flop using 90nm CMOS Process

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ABSTRACT

This paper proposes a novel approach to design high speed, low power self triggered D flip-flops with extremely small die area in comparison to the conventional flip-flops. Flip-flops are synchronous sequential machines that require an external clock pulse for synchronization. The proposed flip-flop generates an internal clock itself and due to this flip-flop does not require external synchronization. Proposed design has relatively less number of transistors than conventional designs, which drastically improved the performance in terms of compactness, speed and power consumption. Design and simulation of proposed flip-flop has been carried out in Microwind simulation tool using 90 nm CMOS technology.

KEYWORDS *– Self Triggered, CMOS, die area, power consumption, transistor count*

I. Introduction

Due to growing demand and popularity of portable electronic devices, designers are seeking for lesser silicon area, higher speed and long battery life.[1] Over past three decades technology scaling of transistors had a great impact upon die area, power dissipation and propagation delay. In digital systems static and dynamic power dissipation is a major factor that needs to be considered during the design phase .the dynamic power dissipation is generally expressed as-

$$P_d = CV_{dd}^2F$$

Where C is output capacitance, F is clock frequency and V_{dd} is supply voltage. For maintaining lower dynamic power dissipation supply voltage and clock frequency should be low. In a similar manner static power dissipation is dependent upon leakage current in transistors which increases dramatically as the technology scales down.[5]

In digital systems flip-flops are key elements which are used to store single bit of information and it has very diverse area of applications. Depending upon the edge of the clock at which the state of flip-flop changes, Flip-flops are classified as positive edge triggered, negative edge triggered and double edge triggered etc

In this paper a new methodology of clock generation is proposed to eliminate the requirement of external clock pulses. The paper is organized as follows: section II gives a brief idea of conventional single edge and double edge triggered flip-flops section III explains proposed self triggered D flip-flop architecture. In section IV the layout and Simulation results of self triggered flip-flop is presented. In section V conventional and proposed design are compared on the basis of various performance parameters and then paper ends in section VI with the major conclusion.

II. Brief literature

Flip-flops are the basic building block of modern memory systems. It is used to store a single bit of information. The flip-flop changes its state corresponding to the applied trigger signal. Based on the triggering used flip-flops are classified as.

1) *Single edge triggered flip-flops (SETFF)*
2) *Double edge triggered flip-flops (DETFF)*

In single edge triggered flip-flop, change in state takes place on the arrival of either positive or negative edge of clock pulses. If positive edge of clock cause change in state of flip-flop then it is said to be "Positive edge triggered flip-flop" and if negative edge of clock cause change in the state of flip-flop then it is said to be "negative edge triggered" flip-flop.

Single edge triggered flip-flop is designed by cascading a positive level triggered and negative level triggered latch. A Positive edge triggered flip-flop can be designed by joining a negative level triggered latch followed by positive level triggered latch whereas a negative edge triggered flip-flop can be designed conversely.

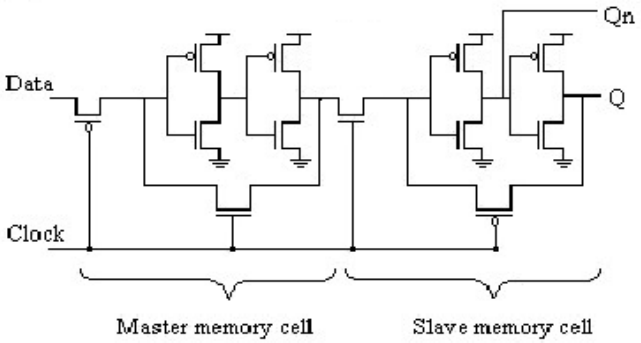

Fig.1: Single edge triggered flip-flop

A conventional single edge triggered flip-flop is shown in fig. 1. [2], it is composed by cascading two latches in Master-Slave configuration which triggers at complementary logic levels 0 and 1 of the clock signal. When the clock is at logic 0 master latch switch its current state according to the applied data D where as the slave latch holds its previous state. In a similar manner when the clock is at logic 1 level, Master latch does not change its state where as slave latch updates it state according to applied logic levels.

From the above discussion, it is evident that the flip-flop changes its states only either negative or positive level of clock. Whenever the output changes its state at the either rising edge or trailing edge of the clock pulses, flip-flops are said to be positive edge triggered and negative edge triggered respectively. In the present design single edge triggered (positive in this case) approach is used. The consequence of which, it have less transistor count and hence less die area are required. The single edge triggered flip-flop suffers the problem of higher propagation delay. To address this issue, researchers propose double edge triggered flip-flop, which also have limitations in terms of power dissipation and die area. These flip-flops are more efficient at high frequencies.

Double edge triggered flip-flop is formed by utilizing both positive and negative edge triggered flip-flops. The output of positive and negative edge triggered flip-flop is tied together to generate the output. During the rising edge of clock pulse, positive edge triggered flip-flop changes its state and negative edge triggered flip-flop holds its previous state. In a similar way during the trailing edge of the clock pulse, negative edge triggered flip-flop changes its state and positive edge triggered flip-flop remains in previous state. Since the outputs of both flip-flops are tied together the output changes at both rising and falling edge of the clock pulses.

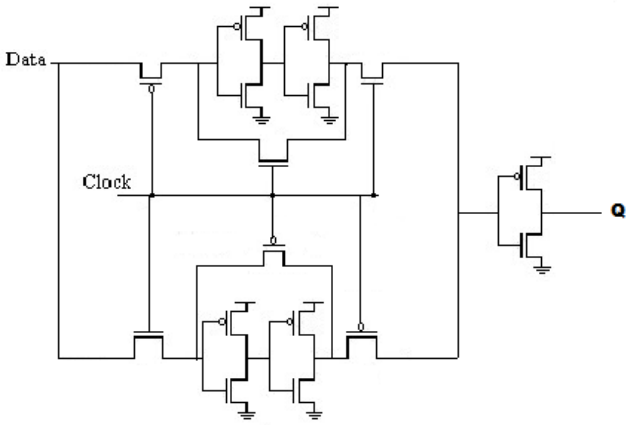

Fig. 2: High performance Double edge triggered flip-flop [2]

The double edge triggered flip-flops give better performance in comparison to single edge triggered flip-flops. Although the propagation delay is improved through the design but requires greater transistor count which results into comparatively larger die area.

III. Proposed self triggered Flip-Flop

In order to address the problem associated double edge triggered flip-flops, we proposed a self triggered flip-flop which have a small power dissipation in comparison of double edge triggered flip-flops with die area and packing density as comparative to single edge triggered flip-flop. Hence self triggered flip-flop offers the best features of single edge triggered and double edge triggered flip-flops.

The block diagram of proposed self triggered flip-flop is shown in fig. 3 here self-triggered flip-flop depicts that unlike other flip-flops it does not require external clock pulse for synchronization. This flip-flops itself derive the clock which triggers the flip-flop internally.

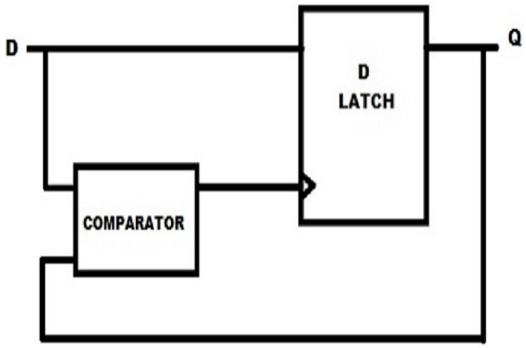

Fig. 3: self triggered flip-flop

The circuit is designed by a level triggered latch and a comparator. The comparator is used to provide feedback control to the flip-flop. The D latch changes its state on positive level of clock pulse only when the data input D and Latch output Q is dissimilar. When they identical the output remains unchanged. This fact can be utilized in order to track those instances when data D and output Q are different. A comparator is used to compare the present input and present output. Hence the comparator provides the output 1 whenever the data D and output Q attains different logic values and 0 at all other time. This output of comparator is applied as a clock signal for latch. Since the propagation delay between the input and output of latch is very small, the pulse-width of clock is also small. Clock pulse will be available at rising as well as trailing edge of data signals. The frequency of the clock depends upon the data rate of the input D. As input data rate increases, clock frequency also increases, similarly reduction in input data rate causes reduction in clock frequency

The CMOS implementation of self triggered flip-flop utilizing single latch along with the comparator circuit is shown in fig. 4.

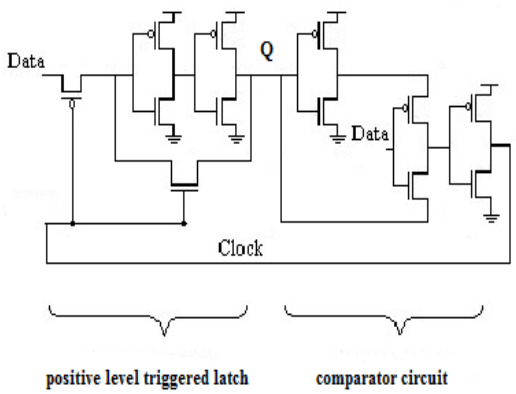

Fig. 5: Proposed self triggered flip-flop

The self triggered flip-flop is implemented with only 12 transistors thus it require less die area in comparison to conventional designs. The self triggered flip-flop offers a great advantage as a frequency of clock signal modulated in accordance with applied data. So the instance at which no data is applied at the input clock pulses doesn't change and hence dynamic power can be saved.

IV. Simulation Results

For the purpose of performance estimation of proposed self triggered D flip-flop, design is implemented using 90 nm CMOS technology. The layout is designed using back end design and simulation tool MICROWIND with 1.20 volt supply voltage at 27°C temperature. The CMOS implementation of self triggered D flip-flop is shown in fig. 6

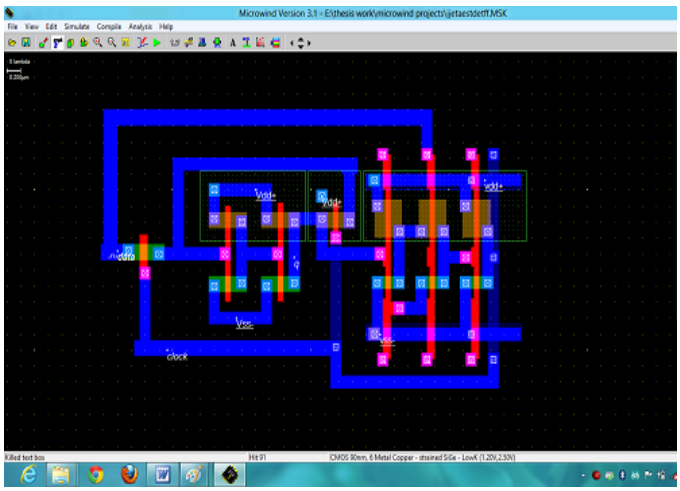

Fig. 6: Layout of proposed self triggered D flip-flop

Simulation results of proposed self triggered flip-flop are shown in fig. 7. The simulation of layout is performed on same simulation tool i.e. MICROWIND, the length of simulation is taken 10 nanoseconds with the step size of 0.1 picoseconds the applied data frequency is 500 MHZ. the output, clock and the delay between input data and output is shown in figure.

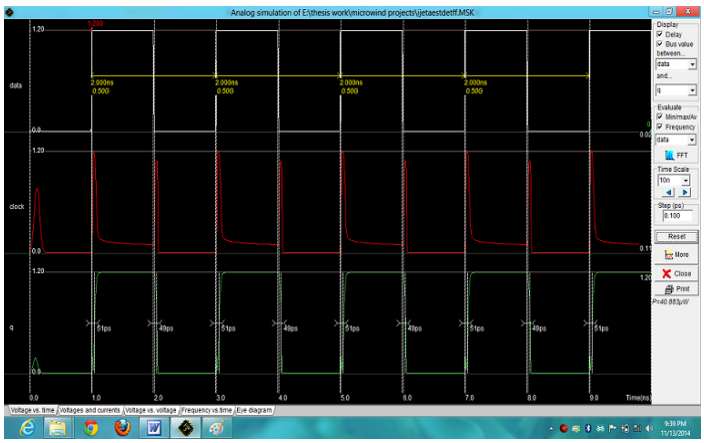

Fig. 7: Proposed self triggered flip-flop simulation output

From above simulation results it is evident that output Q is replica of the data input D and comparable to double edge triggered flip-flop, the clock is in form of very sharp pulse which arises during positive and negative level of data input.

V. Performance comparison

On the basis of simulation results the performance of proposed self triggered D flip-flop is compared with single and double edge triggered flip-flop on various parameters a comparable analysis of different performance parameter is done in table 1. [2]

S. no.	PARAMETERS	SETFF	DETFF	PROPOSED FLIPFLOP
1.	Power dissipation (μW)	6.48	51.60	40.88
2.	Propagation Delay (ps)	28	11	49
3.	Area (μm^2)	57.77	75.62	33.66
4.	Transistor count	14	16	12
Technology: CMOS 90nm, 6 Metal Copper-strained SiGe Low k (1.2V-2.5V).				

Table1: Performance comparisons of flip-flops

From above analysis it is evident that power consumption of proposed flip-flop is 40.88 microwatts which is less than double edge triggered flip-flop where as the output and efficiency is comparable with double edge triggered flip-flop. As far as transistor count is concerned proposed design until 12 transistors than others hence die area is reduced to 33.66 microns.

VI. Conclusions

A high performance self triggered flip-flop has been proposed and simulated in microwind simulation software using 90nm CMOS technology. Self triggered flip-flop offers the best features of self edge triggered flip-flop and double edge triggered flip-flop. Above analysis shows that a simple level triggered latch along with the comparator circuit can be used as a flip-flop which itself generates a sharp clock pulse for synchronization. In this manner it eliminates the possibilities of power consumption due to external clock generator and clock distribution circuits which consumes extra powers.

An important advantage proposed design is that it has relatively less number of transistors than conventional design, which drastically improved the performance in terms of compactness, speed and power consumption. The efficiency will also be high as in case of double edge triggered flip-flop. Propagation delay is always constant which can not be achieved through other topologies. As compared to DETFF its

Power dissipation is less i.e. 40.88 microwatts and hence offers longer battery life for portable devices.

VII. References

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