A COMPARATOR WITH REDUCED OFFSET VOLTAGE & DELAY TIME IN 130nm CMOS

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***Abstract**:*
Speed, low-offset voltage, and resolution are some essential factors for high-speed applications. The comparator circuit with preamplifier increases the power dissipation, as it requires higher amount of current than the latch circuitry. A novel topology of dynamic latch comparator is illustrated in this paper, which is able to provide high speed, low offset, and high resolution. As the topology is based on latch circuitry, the circuit is able to reduce the power dissipation. The cross-coupled circuit mechanism with the regenerative latch is employed for enhancing the dynamic latch comparator performance. In addition, input-tracking phase is used to reduce the offset voltage. The spice simulation results for the designed comparator in 130 nm CMOS process show that the equivalent input-referred offset voltage is 40mV & delay of 23.3 ps.
Keywords: Offset Voltage, Latch Comparator and regenerative latch.

I. INTRODUCTION

Analog-to-digital converters (ADC) have become a significant element driving the semiconductor industry over the past few years. Small size processes, low power indulgences, increased integration of different functional blocks within a single chip and a reduced propagation delay make them more acceptable to the semiconductor industry and they are able to provide high speed with low power dissipation. However, it is not straightforward to scale down transistor dimensions, as it requires high channel doping, gate-induced drain leakage, and band to band tunnelling across the junction.The supply voltages need to be decreased according to the small dimensions of the transistorswhen analog circuit design happens to be more complex to carry out the necessity of reliability [2]. All these concerns apply to the most usable representative of the ADCs: the comparator. The comparator is the key building block in the design process for ADCs. The comparators measure the smallest voltage differences in ADC's inputs, resolving the performanceand the precision of any ADCs. An application that requires digital information recovery from analog signals, such as I/O receivers and radio frequency identification (RFID) memory circuits, widely uses high performance comparators to intensify a little input voltage to a big voltage level. Several structures of high-speed comparators exist, such as the multistage open loop comparator, the preamplifier latch comparator, and the regenerative latch comparator.

Multistage open loop comparator has high resolution and high speed among the different structures.On the other hand, the latch-type comparator is the most usable one for the abovementioned applications.

Latch-type comparators are able to accomplish decisions more rapidly with no static power indulgence and strong positive feedback. Also they are able to generate high gain in regeneration mode due to their positive feedback features. Consequently, the most vital limitations of the dynamic latch comparator are the kickback noises which can affects the performance of the dynamic latch comparator due to random noise, input offset voltages, and component mismatch.

If large devices are used for the latching stage, a low offset can be achieved at the cost of the increased delay due to slowing the regeneration time and the increased power dissipation. To meet the specifications such as offset voltage and power dissipation in a limited area, it is necessary to fully understand the correlations between sizes of transistors.

II. DESIGN OF COMPARATOR

The flow chart shows in Fig. 1 shows the step of designing the low power CMOS dynamic latch comparator.

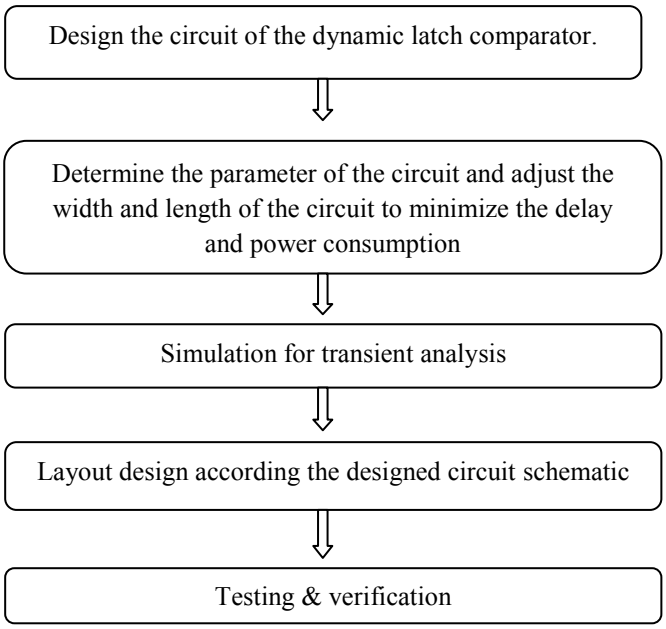

Fig. 1: Design & simulation flowchart

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III. PROPOSED COMPARATOR

Fig. 2 shows the circuit topology of a new dynamic latch comparator. To give low power during the regeneration mode, a latch with resistive comparing circuits in series with NMOS is used. Input is provided to two back to back connected MOS M1-M3 and M2-M4.

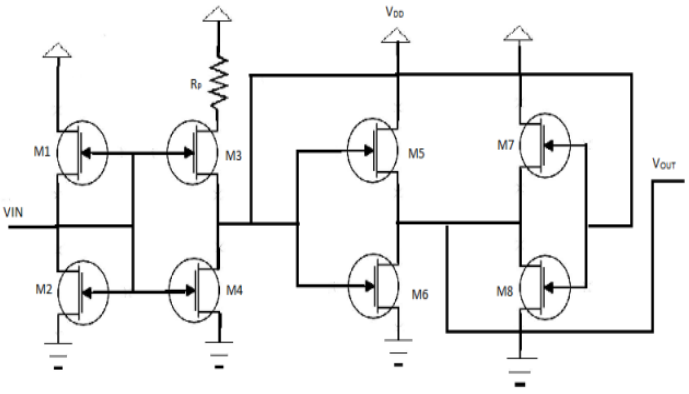


Fig. 2: Proposed design of Comparator

Table 1: CMOS Transistor parameters

	All PMOS	All NMOS
Width	1.0µm	0.60µm
Length	.13µm	.13µm

Figure 3 shows the dc output voltage waveform. If the input of the comparator is greater than the reference voltage, Vref, it has to give an output of '1' and if the comparator input is less than reference voltage then the output of the comparator should be '0'. Here the given reference voltage is 2.51 V. When V_{in} is less than Vref output is min. & maximum when input is greater than Vref. A simple comparator performs the required function efficiently.

Table 2:DC Analysis

Vdd=3.2V			
Offset voltage(output)		I/POffset	inputs(V)
out(mV)	out'(mV)	Vis(mV)	Vin1 ,Vin2
36.522	35.783	38.579	3.4,0
36.533	35.793	37.597	3.4,0
39.182	19.282	40	3.2,3.6

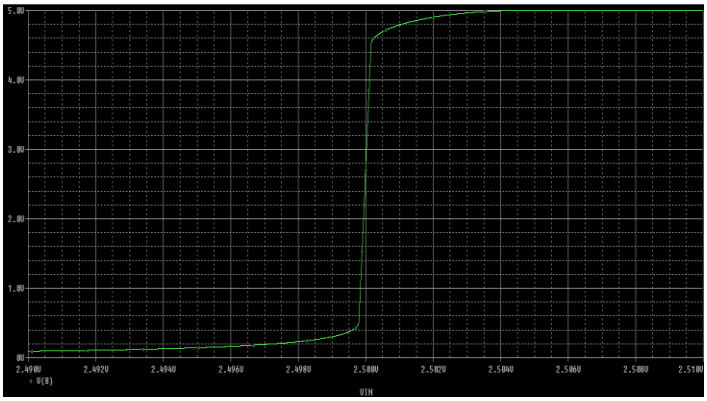
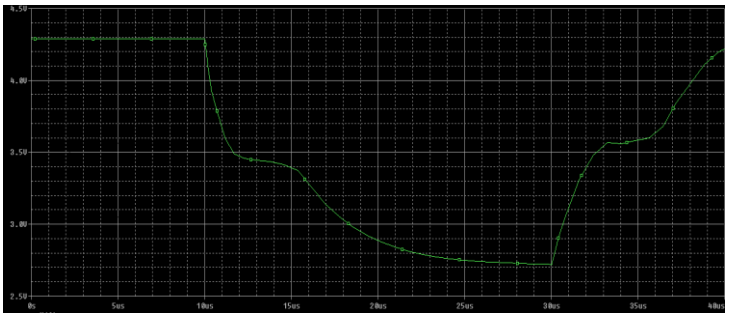


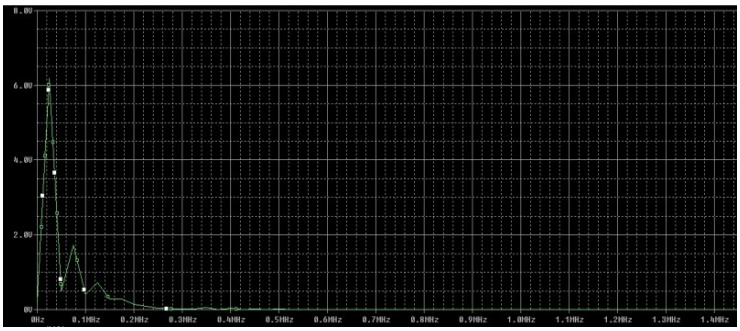
Fig.3: Output voltage waveform

IV. SIMULATION RESULTS

Simulation of reported design is done using the 0.13µm CMOS technology. In this project, 1.2 V supply voltage is used for operation. During the process, speed of the comparator is 100MHz. This design can be used where low power, high speed and low propagation delay are the main requirements. Finally simulation results of the comparator are shown here. The width of the transistor used is as in the Table I.



Transient response



Fourier analysis

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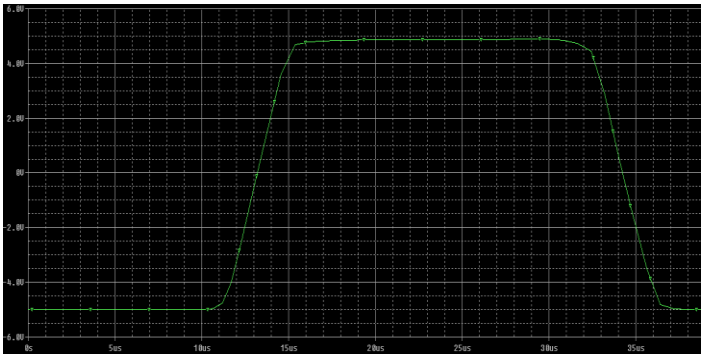

Propagation delay

V. PARAMETERS CHOSEN

a. Propagation delay of the comparator

Propagation delay and the settling time are most important dynamic parameters that determine the speed of a comparator. Propagation delay is the amount of time that it takes for a change in the input signal to produce a change in the output signal [6]. The shorter propagation delay, the higher the speed of the circuit and vice-versa. For reducing delay and increase sensitivity, latched comparators are used. Delay time is measured at 50% transition of the point. The propagation delay is determined using two basic time intervals, which is tplh and tphl. tplh is the delay time measured when output is changing from logic 0 to logic 1 and tphl is from logic 1 to 0.

b. Effect of the technology chosen

This project uses 0.13µm technology which is smaller length than technology used in the previous work by [2], so the minimum length for this project is 0.13µm. Simulation results shows that the smaller length will produce the higher speed due to less propagation delay.

c. Effect of the width of transistor

The study reference paper use width of transistor for PMOS is 10µm and NMOS is 5µm. This paper proposes 0.60µm width for PMOS and 1µm width for NMOS,the propose width produce the slower speed compared to the width of the previous work. Although the speed will be slower when using smaller width, but the area for this project will be smaller.

VI. CONCLUSION

A novel high-speed and low-offset dynamic latch type comparator method is presented in this research work. The proposed design does not use any preamplifier stages before the latch stage, which reduces the power dissipation and the area dramatically. The simulation results clearly reveal that the dynamic latch comparator is able to switch properly with different input stepping sizes. Moreover, the comparison study shows that the novel design is able to operate at a higher clock frequency of 50MHz with offset voltage 40mV and propagation delay 23.3 pS in 1.2V supply voltage, which is better than recently published research works.

VII. REFERENCES

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