LOGIC EFFORT OF CMOS BASED DUAL MODE LOGIC GATES

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ABSTRACT

This logic allows operation in two modes: 1) static and2) dynamic modes. DML gates, which can be switched between these modes on-the-fly, feature very low power dissipation in the static mode and high performance in the dynamic mode. A basic DML gate is very simple and is composed of any static logic family gate and an additional clocked transistor. In this paper, we introduce the logical effort (LE) methodology for the CMOS-based **DML family. The proposed methodology allows path length minimization, delay optimization, and delay estimation of DML logic .Finally we model the scheme on 32 nm CAD tools along with relevant analysis.**

Index Terms—Dual mode logic, high performance, logical effort, low power ,optimization.

I .INTRODUCTION:

LOGIC optimization and timing estimations are basic tasks for digital circuit designers. The logical effort (LE) method was first presented by Sutherland, for easy and fast evaluation and optimization of delay in CMOS logic paths. Because of its elegance, the LE method has become a very popular tool for designing and education purposes and is adopted to be the basis for several computer-aided-design tools. Although LE is mainly used for standard CMOS logic, it is also shown to be useful for other logic families, such as the pass transistor logic .The novel dual mode logic (DML),which provides the designer with a very high level of switching between two modes of operation: 1) static and 2) dynamic modes. In the static mode, DML gates achieve very low power dissipation, with some degradation in performance, as compared with standard CMOS. On the other hand, dynamic operation of DML gates achieves very high speed at the expense of increased power dissipation. A basic DML gate is composed of any static logic family gate, which can be a conventional CMOS gate, and an additional transistor. DML gates have a very simple and intuitive structure, requiring n conventional sizing methodology to achieve the desired performance. Conventional LE methodology cannot be used with the DML family as it does not consider its unconventional sizing rules and topology. The novel dual mode logic (DML),which provides the designer with a very high level of flexibility. It allows on-the-fly switching between two modes of operation: 1) static and 2) dynamic modes. In the static mode, DML gates achieve very low power dissipation, with some degradation in performance, as compared with standard CMOS. On the other hand, dynamic operation of DML gates achieves very high speed at the expense of increased power dissipation.

A basic DML gate is composed of any static logic family gate, which can be a conventional CMOS gate, and an additional transistor. DML gates have a very simple and intuitive structure, requiring n conventional sizing methodology to achieve the desired performance. Conventional LE methodology cannot be used with the DML family as it does not consider its unconventional sizing rules and topology. The objective of this paper is to develop a simple method for minimizing delays and achieving an optimized number of stages in logical paths containing CMOS-based DML gates. A unified LE method is introduced for the delay evaluation and optimization of logic paths constructed with DML logic gates. DML-LE answers complete (un approximate) design

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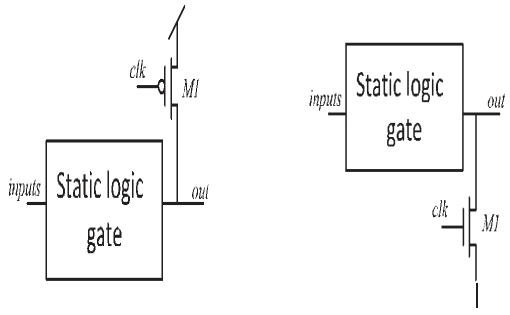
problems, which can be solved numerically, and simplifies these problems to a straightforward and easy computational problem [approximate and semi approximate (SA) solutions] with a unified analytic model. With this model, we can estimate the minimum to maximum error under delay approximation and the error in the target optimum number of stages for a given logic function. The efficiency of the developed method is shown by a comparison of the theoretical results, achieved using the proposed method with simulation results of Micro wind tool using a standard 32-nm technology

II.DML OVERVIW

As previously mentioned, a basic DML gate architecture is composed of a static gate and an additional transistor M1,whose gate is connected to a global clock signal . In this paper, we specifically focus on DML gates that utilize conventional CMOS gates for the static gate implementation. DML gates present two possible topologies: (1) Type A and (2) Type B, as shown in Fig. 1 accordingly. In the static mode of operation, the transistor M1 is turned off by applying the high Clk signal for Type A and low Clk for TypeB topology. Therefore, the gates of both topologies operate in a similar way to the static logic gate, which here is a standard CMOS operation. To operate the gate in the dynamic mode, the Clk is enabled, allowing for two separate phases: (1) pre charge (2) evaluation. During the pre charge phase, the output is charged to VDD in Type A gates and discharged to GND in Type B gates. During evaluation, the output is evaluated according to the values at the gate inputs.DML gates show a very robust operation in both static and dynamic modes under process variation at low supply voltages. The robustness in the dynamic mode is mainly achieved by the inherent active restorer (pull-up in Type A/pull-down in Type B) that also enabled glitch sustaining, charge leakage, and charge sharing. It is also shown that the proper sizing methodology is the key factor to achieve fast operation in the dynamic mode. Fig. 2 shows the sizing of CMOS-based DML gates that are optimized to a dynamic mode of operation, whereas Fig. 1(d)shows conventional sizing of a standard CMOS gate. The input and output capacitances of the DML gates are significantly reduced, as compared with CMOS gates, due to the utilization of minimal width transistors in the pull-up of Type 1 or pull-down in Type B networks. The size of the pre charge transistor is kept equal S*W min to maintain a fast pre charge period despite the increase in the output load. Contrary to CMOS gates, each DML gate can be implemented in two ways, only one of which is efficient. The preferred topology is such that the pre charge transistor is placed in parallel to the stacked transistors, i.e., NOR in Type A is preferred over NAND, and NAND in Type B is preferred over NOR. In this case, the evaluation is performed through the parallel transistors and therefore it is faster. As presented the optimal design methodology of DML gates is to serially connect Type A and TypeB gates, similarly to np-CMOS/NORA techniques. Even though this design allows maximum performance,area,minimizatio and improved power efficiency, serial connection of the same type gates is also possible. However, this case presents many drawbacks, such as the need of footer/header and severe glitching. These well-explored problems are standard for dynamic gates design . DML strength is that static mode CMOS-based DML gates with transistor sizes optimized for the dynamic mode is actually a semi energy-optimal CMOS construction of a gate because of reduced static and switching energy consumption. The static operation of the DML gates is used to significantly reduce energy consumption at the expense of 2–4 times reduction in performance.



Fig(1):DML TOPOLOGY TYPEA TYPE B

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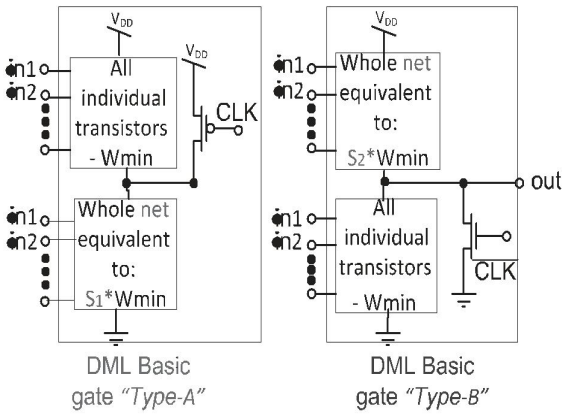

FIG (2): CMOS-based DML gate with sizing factors

A general approach is to optimize the delay for the dynamic mode of operation and operate the system in the static mode only in standby/low-energy mode without severe frequency restrictions, that is magnitude of 2–4 times in performance is reasonable.

III.DMLNAND,NOR,INVERTER GATES DESIGN:

Conventional NAND logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic NAND gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. The truth table of the 2-input NAND gate is given in Table 1. Table-1:

A	B	Q
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table I: 2-input NAND gate

To design a DML gate, the methodology that is to be followed is to place the pre-charge transistor in parallel to the stacked transistors of the basic CMOS gate. Then, the evaluation of the logic will be performed with the parallel transistors which will make the evaluation process faster

In the DML Type-B Static NOR topology, the switching element is an NMOS transistor connected parallel to the Pull-down network which is a parallel connection of 2 NMOS transistors. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOR topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation as shown in Fig. 4.

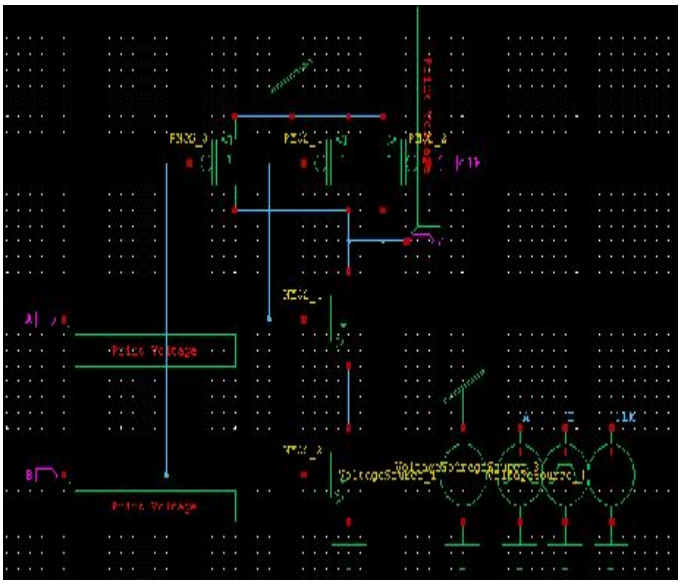

Fig-1: Schematic of type A Static NAND

In the DML Type-A Static NAND topology, the switching element is a PMOS transistor connected parallel to the Pull-up network as shown in Fig. 1. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NAND topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for

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dynamic mode of operation. In the DML Type-B Static NAND topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NAND topology shown in Fig. 2 is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation.

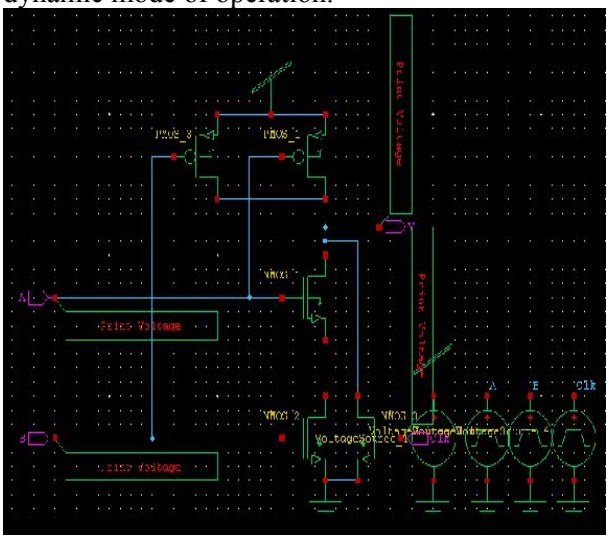

Fig-2: Schematic of type B Dynamic NAND

Conventional NOR logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found.

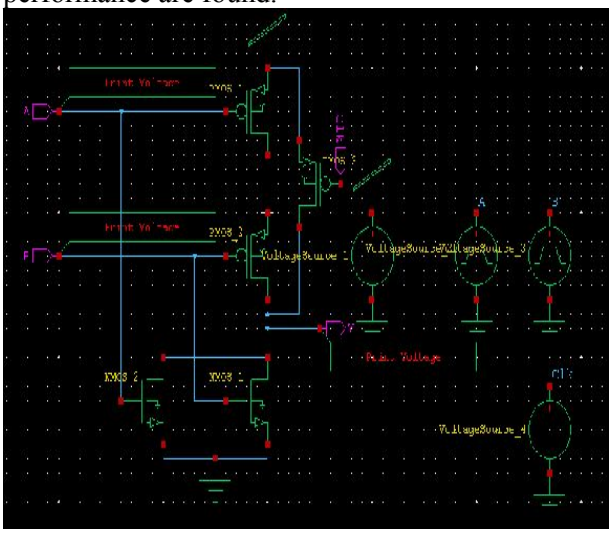

Fig-3: Schematic of type A Static nor

Also Dual Mode Logic NAND gate Type A and Type B topologies Fig-2: Schematic of type B Dynamic NAND Conventional NOR logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic NAND gate Type A and Type B topologies

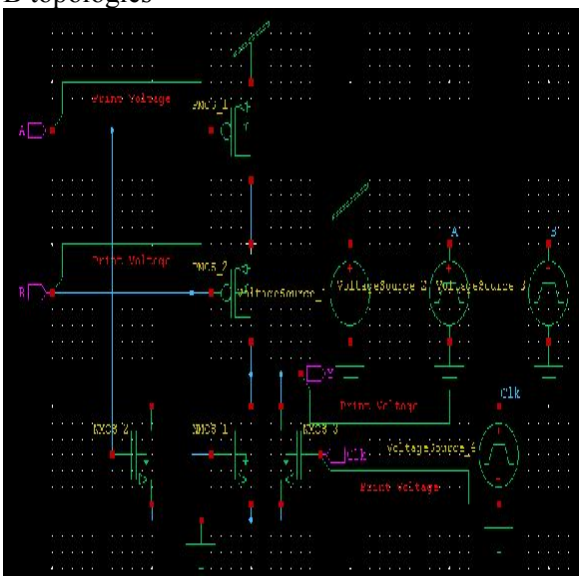

Fig-4: Schematic of type B Dynamic nor

Conventional inverter gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic NAND gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. The truth table of the NOT gate is given in Table.

A	Q
0	1
1	0

Table II: Truth Table of NOT

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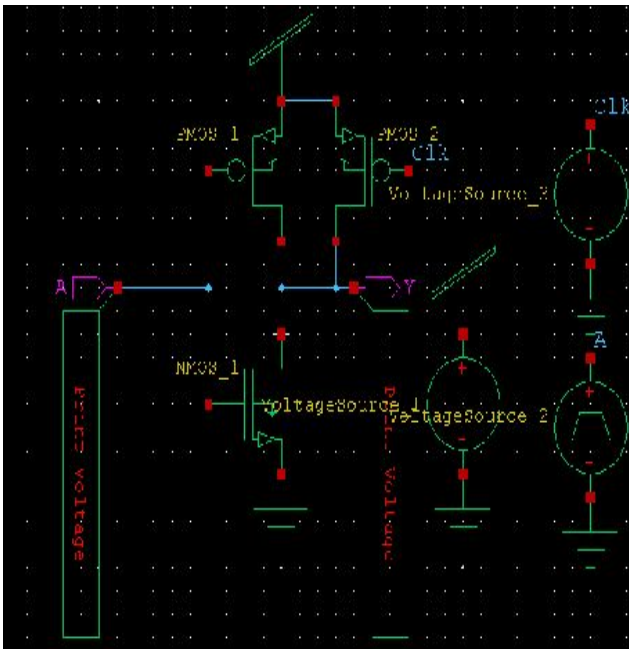

Fig-5: Schematic of type A Static not .

In the DML Type-B Static NOT topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation as shown in Fig. 6.

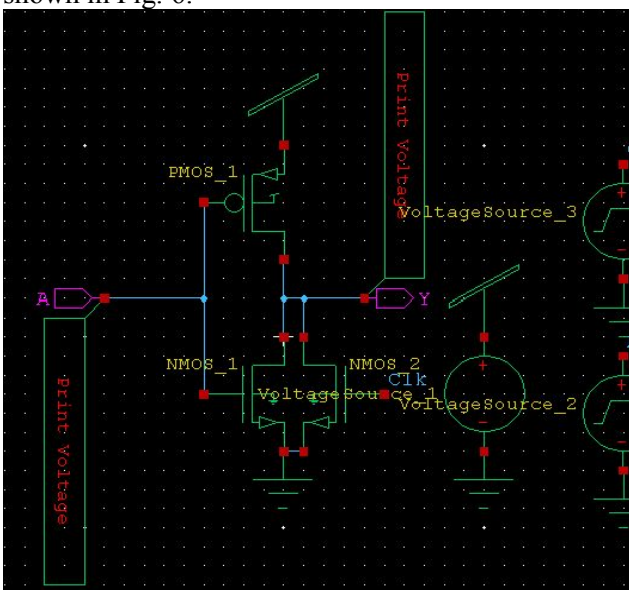

Fig-6: Schematic of type B Dynamic not .

IV.DML WITH POWER GATING :

TECHNIQUES Power Gating is an effective implementation that is used in Low Power Designs. Whereas Clock Gating saves the dynamic power of a circuit, Power Gating saves the leakage power. As the technology moves from micron technology to sub-micron technology, the leakage power dissipation dominates the dynamic power dissipation. The power gated sleep circuit has two modes of operations: (1) Active mode (2) Sleep mode In active mode, the sleep Signal SLEEP of the transistor is held at logic' 0 'and SLEEP` at logic „1" hence both the sleep transistors remain ON. In this case both transistors offer very low resistance and virtual ground (VGND) node potential is pulled down to the ground potential, making the logic difference between the logic circuitry approximately equal to the supply voltage. In sleep mode, the sleep Signal SLEEP of the transistor is held at logic' 1 'and SLEEP` at logic "0" hence both the sleep transistors are turned OFF

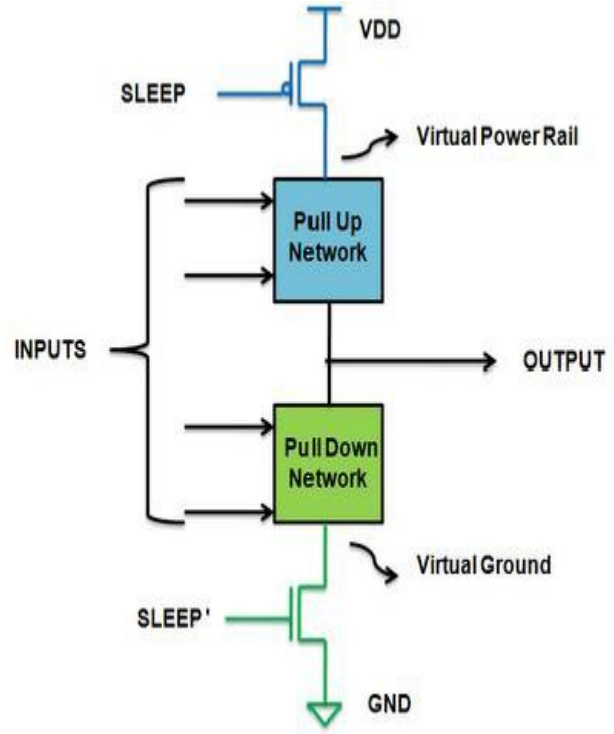

Fig-7: Power Gating structure

and the logic part is disconnected from the supply and ground leading to very less power

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consumption during sleep mode. Power gating is incorporated in to the DML architecture as shown in Fig. 8.

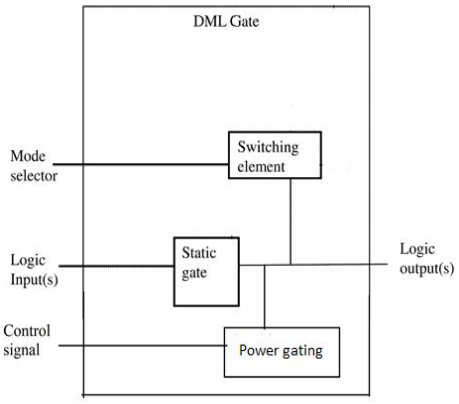

Fig-8: DML Architecture

DML gate with Power Gating Different methods of power gating like the sleep method, sleepy stack and dual sleep approaches added to the existing Dual mode logic NAND, NOR, NOT gates. The Sleep method is the basic power gating method. The sleep transistors isolate the logic networks and the sleep transistor technique or the sleep method dramatically reduces leakage power during sleep mode. Fig.8 shows Type A Dynamic Dual Mode Logic NAND with sleep power gating technique.

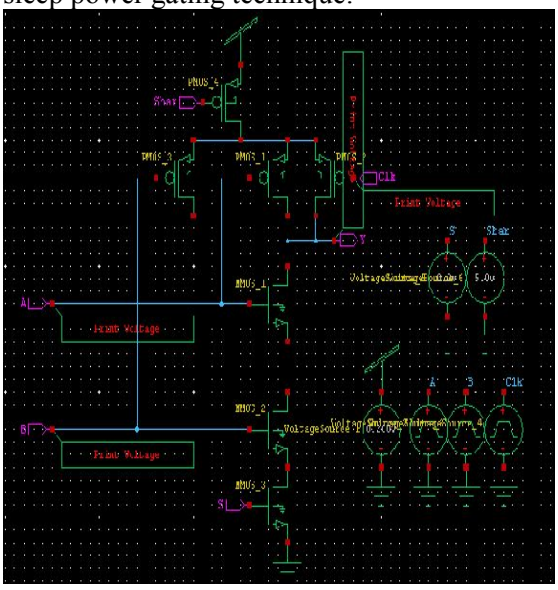

Fig-9: Type A dynamic NAND with Sleep Power Gating Technique

The sleepy stack approach merges the sleep and stack approaches. The sleepy stack technique splits the existing transistors into two half Size transistors like the stack approach. The activity of the sleep transistors in the sleepy stack method is same as the activity of the sleep transistors in the sleep method. The sleep transistors are turned on during the active mode and they are turned off during the sleep mode. Fig. 9 shows Conventional NOT gate with Sleepy Stack Power Gating Technique

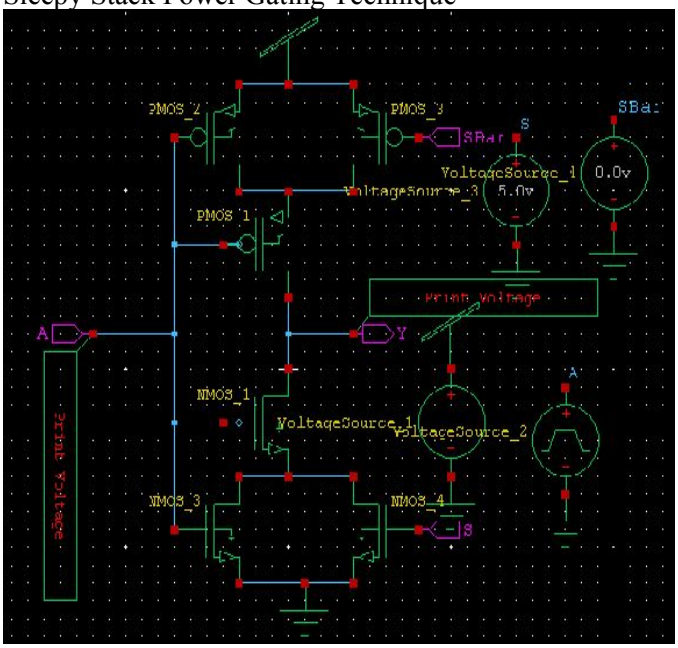

Fig-10: Conventional NOT gate with Sleepy Stack Power Gating Technique

The Dual sleep approach has the advantage of using the two extra pull- up and two extra pull-down transistors in sleep mode either in OFF state or in ON state. In normal mode when S=1 the pull down NMOS transistor is in ON state and in the pull-up network the PMOS sleep transistor is in ON state since S=0. During sleep mode state S is forced to 0 and hence the pull-down NMOS transistor is in OFF state and PMOS transistor is in ON state and in the pull-up network, PMOS sleep transistor is OFF while NMOS sleep transistor is ON. So in sleep mode state a PMOS is in series with an NMOS both in pull-up network and pull-down network which reduces the power dissipation. Fig.10 shows Type B Static NOR with Dual Sleep Power Gating Technique.

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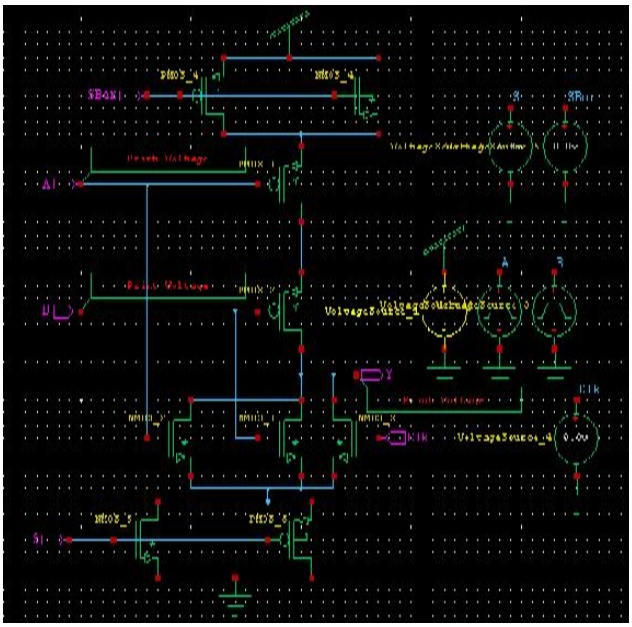

Fig-11: Type B Static NOR with Dual Sleep Power Gating Technique.

V. CONCLUSIONS

The result obtained leads to the conclusion that while operating in the dynamic mode, sub threshold DML gates achieve an improvement in speed compared to a standard CMOS, whereas dissipating more power and in the static mode, a reduction of power dissipation is achieved, at the expense of a decrement in performance. The different methods of power gating applied to the DML logic have reduced the power dissipation further.

LE approach for CMOS-based DML logic networks was presented. The proposed approach allowed an efficient optimization of DML logic networks for maximum performance in the dynamic mode of operation, which was the focus of this paper. DML logic, optimized according to the proposed LE methods, allowed extended flexibility in optimizing various structures of DML networks. This optimization utilized the DML inherent properties of significantly reduced parasitic capacitance and ultralow power dissipation in the static operation mode. This paper presented three different approaches, which traded off between computation complexity and accuracy. The complex CS method was only addressed for error analysis of the other methods. The CA method was identical to CMOS LE computation with very small error and the SA method was also identical to the CMOS LE computation aiding one more lookup table (which easily derived for all cases and loads). We showed that with these tools only a design can achieve very high performance results. Advantages and drawbacks of each one of the methods were discussed. Simulation results, carried out in a standard 32-nm process, proved the efficiency of the proposed approach and compared it with existing CMOS LE.

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