A REVIEW ON DESIGN OF PIPELINED ADC

J Monica B.E., (M.E)
Electronics and Communication Engineering
PET Engineering College, Vallioor

Prof.P.Kannan M.E., (PhD)
Head of ECE Dept
PET Engineering College, Vallioor

***Abstract*----Most of the communication systems today use DSP (Digital Signal Processing) to resolve the transmitted information. Therefore between the received analog signal and DSP system an analog to digital interface is necessary. Thus pipelined ADC is advantageous and widely used in many applications. This paper presents survey or review on many literature papers based on the analysis of power dissipation and SNR. Low power dissipation is very important in ADC design. There are several techniques discussed below for good performance. After surveying several papers double sampling technique is considered to have low power dissipation and better SNR.**

Keywords*----*Pipelined ADC, CMOS, low power, memory effect, op-amp sharing, sub sampling.

I INTRODUCTION

With the explosive growth of wireless communication system and portable devices, the power reduction of integrated circuits has become a major problem. In applications, such as PCS (personal communication system), cellular phone, camcorders and portable storage devices, low power dissipation, hence longer battery lifetime, is a must. An example for low power application is a wireless communication system. With the rapid growth of internet and information-on-demand, handheld wireless terminals are becoming increasingly popular. (i.e. UPS and FeDex handheld pad for package delivery.). With limited energy in a reasonable size battery, minimum power dissipation in integrated circuit is necessary. Many of the communication systems today utilize digital signal processing (DSP) to resolve the transmitted information. Therefore, between the received analog signal and DSP system, an analog-to-digital interface is necessary. This interface achieves the digitization of received waveform subject to a sampling rate requirement of the system. Being a part of communication system, the low power constraint, mentioned above, the A/D interface also needs to adhere to the low power constraint.

The demand on high resolution and high speed analog-to-digital converters (ADC's) has been growing in today's market. The pipeline ADC's present advantages compared to flash or successive approximation ADC techniques. High-resolution, high-speed requirements can relatively easier be achieved using pipelined architecture ADC's than other implementations of ADC's of the same requirements. Because the stages work simultaneously, the number of stages needed to obtain a certain resolution is not constrained by the required throughput rate. The first stage operates on the most recent sample, while the following stages operate on the remainder analog voltages, called residues from previous samples. The block diagram of pipelined ADC is given in Figure: 1. The goal of this paper is to survey on different literature papers based on high speed, low power and low voltage A/D converter.

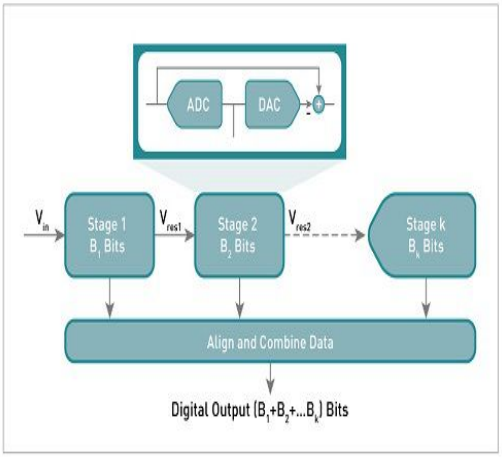

Figure 1: Block Diagram of Pipelined ADC

On analyzing Double sampling technique is the best technique to save power consumption without risking performance degradation. High resolution and low noise pose challenges in the op-amp design. Problems like gain, speed, noise, as well as power consumption, become more difficult to trade-off. Bootstrapped switches should be used at the front-end for low distortion input sampling [1]. ADC is sensitive to distortion introduced by the residue amplifiers in their first few stages, and residue amplifier distortion tends to be inversely related to both power supply voltage and power dissipation. Therefore, the residue amplifiers are usually the dominant consumers of power in high resolution pipelined ADCs, particularly in low supply voltage designs. Thus Common-mode drift issue occurs Since there is no common-mode feedback inside the loop the common mode drift caused by the mismatch of capacitors, offset of op amp and charge injection accumulate stage by stage [2]. In order to minimize capacitor mismatch, both of the gate-bootstrapped NMOS switches and conventional CMOS switches is used with highly linear integrated capacitors. The conventional CMOS sampling switches tend to show signal-dependent distortion in sampled input signals. The distortion degrades the dynamic performance of the SHA [3]. Speed-accuracy trade off are natural in ADC's. Slow-but-accurate ADC is itself calibrated, which means that the calibration is nested. The result is a fast-and-accurate ADC

that does not require any high-gain op-amps [4]. So op-amp with high gain is very essential. The input signal S/H function is combined into the first MDAC using an op-amp split-sharing scheme in order to prevent the aperture error. Signal path of the S/H and the signal path of the MDAC. The gain-boost technique, allowing for a larger output voltage swing and an extension of the technique boosting the dc gain to even higher values. While using this technique in the design of an op amp, care should be taken to avoid instability or slow settling components, and present a design guideline for optimal settling behavior. This op-amp configuration is used in double sampling technique.

In section II the methodology of above papers is explained. Section III deals with the performance analysis of discussed techniques.

II METHODOLOGY

Pipeline analog-to-digital converters have been extensively used in high-speed medium-accuracy systems due to their partitioned nature. The accuracy partitioning of pipeline ADCs significantly reduces the power and area requirements of a given ADC design, thus allowing designers to push pipeline ADCs to very high speeds. Normally in designing ADC there may be chance of occurrence of more noise. So it is necessary to design a system with better performance. This chapter covers various techniques for designing pipelined ADC.

A. NESTED DIGITAL BACKGROUND CALIBRATION

Among various background calibration techniques, the correlation based schemes are most promising because they involve minimum additional analog circuitry [4]. In this calibration scheme, the errors due to capacitor mismatches and finite op-amp gain are corrected by re-calculating the digital output based on the equivalent radix value of each stage. The equivalent radices are extracted on-line using a correlation-based algorithm. The small errors are modulated by a pseudorandom sequence in the analog domain. Then, they are converted to a digital code along with the input signal to the ADC. These small error terms are detected in the digital domain by correlating the ADC digital output with the same pseudorandom sequence.

Figure: 2 illustrate one possible (not optimum) background equivalent radix extraction scheme based on correlation. This calibration scheme incorporates a pseudorandom noise sequence, which is scale by a constant (1/4 in this figure) and then added to the input of the sub-DAC. This pseudo-random noise travels through the inter stage gain block which contains the actual radix number. Then, it is quantized by the back-end ADC. Finally, to maintain the same SNR, this added pseudo-random noise is subtracted from the back-end ADC's output in the digital domain. An estimated radix number has to be provided to do this pseudo-random noise cancellation.

It is a good initiative design to deal with the effect of op-amp sharing switch. This technique will be useful in low voltage design by a constant (1/4 in this figure) and then added to the input of the sub-DAC [1]. This pseudorandom noise travels through the inter stage gain block which contains the actual radix number. Then, it is quantized by the back-end ADC. Finally, to maintain the same SNR, this added pseudorandom noise is subtracted from the back-end ADC's output in the digital domain. An estimated radix number has to be provided to do this pseudorandom noise cancellation.

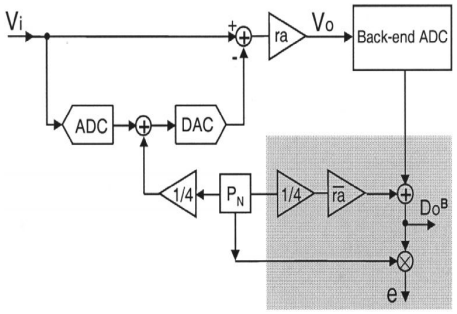

Figure 2: Background Equivalent Calibration with Radix Extraction

There are some important issue in the above technique, first is the amplitude of the ADCs input signal is reduced when injecting this pseudorandom noise. The reason is that each stage's analog output has a maximum full signal range. Therefore the adding of pseudorandom noise can make the ADC stage's analog output to go out of the full-scale signal range if the input signal's magnitude is not reduced. The second issue is how to inject a scaled pseudo-random noise sequence in the analog domain with a very accurately known magnitude (i.e., the accuracy of 1/4 in the analog domain). This is not a trivial task in a practical integrated circuit (IC) implementation. In using the digital background calibration technique 254mW power get dissipated and achieved peak SNR of 58.2dB with 12 bit precision.

B. SWITH EMBEDDED OPAMP SHARING MDAC WITH DUAL INPUT OTA IN PIPELINED ADC

The basic idea behind this technique is to eliminate the negative effect of "Op-amp sharing switches". In an op-amp sharing technique there will be a set of switch networks and there will be two different phases of clock used to connect these switch networks with the shared Op-amp. There are few common problems associated with op-amp sharing technique [2].

1. Memory Effect

2. Cross talk

3. Charge injection and clock feed through

Memory effect is a common problem in low voltage techniques where the gain of op-amp will always be less than intended. It is technology limited. Hopefully, it won't be a big problem in high voltages. Before analyzing the problem let us make a statement. The op-amp settling accuracy depends on step voltage change and its dc open

loop gain. Since in low voltages the open loop gain is less, the common mode settling at the virtual ground nodes of op-amp varies depends on the previous values stored at the input nodes of op-amp. In this paper they are avoiding it by providing a set of transistors which operates as input transistor in alternate clocks. During alternate clock cycles when the particular set is not used as input transistor, its gate node should be connected to common mode voltage. Thus in every cycle the input of transistor is initialized to Vcm. Thus it avoids the memory effect. Anyway, it won't be a big problem in our design because our design consists of high voltage transistors.

While connecting and disconnecting the alternate switch networks, the different sampled values induces some cross talk through these op-amp sharing switches. This is avoided by placing these switches inside the op-amp circuitry. That is the reason this technique uses the name "embedded switch". It also avoids clock feed through and charge injection [2].

Even though this technique has advantages the biasing of these switches which is in series with the input transistor is tough. It demands additional biasing circuitry. Also, the matching of these switches also important. Any difference in its parameters inherently creates an offset error. It is a good initiative design to deal with the effect of op-amp sharing switch. This technique will be useful in low voltage designs. An op-amp sharing technique there will be a set of switch networks and there will be two different phases of clock used to connect these switch networks with the shared Op-amp.

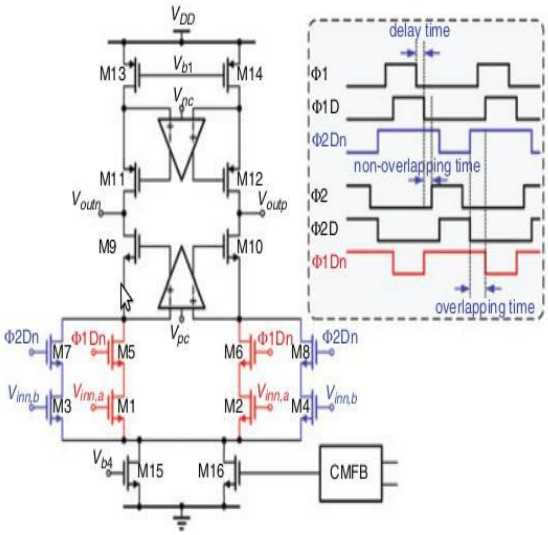

Figure 3: Switch Embedded Op-amp Architecture

C. TIME-SHIFTED CDS TECHNIQUE

In high speed pipeline ADC design the critical bottle neck is the trade-off between power dissipation, bandwidth and the open loop gain. The fact is open loop gain is inversely proportional to the current. So open loop gain decreases with increase in power dissipation. But, higher bandwidth demands higher current i.e higher power dissipation. This is the basic reason why gain boosted op-amps are widely used. One question may rise in everyone's mind. Is the open loop gain an important parameter. Yes, of course. It determines settling accuracy of the system.

Settling accuracy = V_{swing} / open loop gain

If 10 bit precision is needed for an input voltage swing of 1V then needed open loop gain is calculated as follows.

$$1/2^{10} = 1/G$$

$$G = 20 \log(2^{10}) = 60.2 \text{ dB}$$

Correlated double sampling makes use of a technique where the error introduced by the op-amp is canceled [3]. In this technique there are two set of capacitors and an op-amp with input "error storage capacitor". One set of capacitors is called "Pre-charging" capacitors. Another set is called "Sampling Capacitors". This is shown in Figure4.

Unlike the usual way of sampling CDS technique uses three different phases of clock. In the first phase both the PC and SC are used to sample the input. After that the PC (Pre-Charging Capacitance) is connected in amplification mode. During the second phase the error is stored in SC (Sampling Capacitance). In third phase the SC is connected in amplification mode. Since the error is stored already the correction can be made easily. This technique virtually squares the actual gain i.e twice in dB. It consists of several advantages but there is also some disadvantages in CDS technique. CDS technique posses three phases. As it has three phase the settling time of this is very less and at the same time it have good slewing and bandwidth.

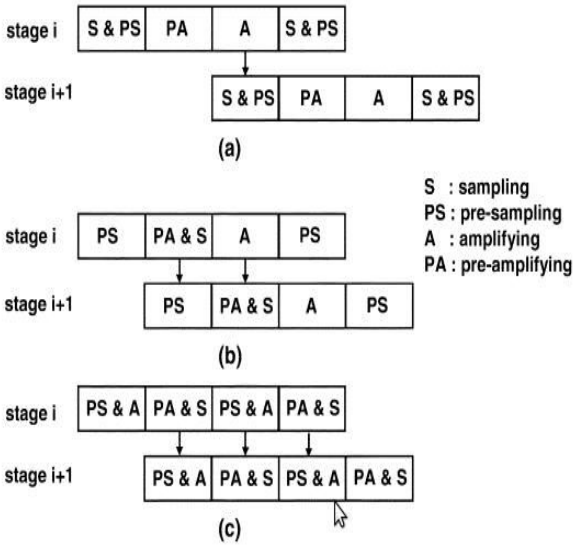

Figure 4: Sample & Hold Scheme of Time shifted CDS

CDS has its own disadvantages [3]:

1. The mismatch in PC and SC will affect the gain. Theoretically it squares the gain. But practical worst case achievable gain is 30dB.

2. Since it has three phases the time period available for settling is less. It demands more bandwidth. Therefore demands more power.

3. Since the sampling capacitance is doubled that also demands more current to have good amount of slewing and bandwidth. Therefore increases the power dissipation.

In order to avoid this power dissipation time shifted correlated double sampling technique is used. In this technique the number of components remains same. Only difference is that the clock timing is adjusted in such a way that in each phase either one set of capacitance will be in Sampling mode and other in the amplification mode.

First phase the PC is in sampling mode. Second phase PC in amplification mode. The error because of finite op-amp gain will be stored in the error storage capacitance. In this phase the SC will be in sampling mode. Final phase the SC will be in amplification mode and PC in per-charging mode. Thus the op-amp charges only PC or Sc at a time. So bandwidth requirement is less with reduced capacitive load in each phase. Therefore it alleviates the problem of power dissipation in conventional CDS.

The disadvantages of time shifted CDS are;

1. The mismatch in PC and SC may create difference between stored error and corrected value.

2. This technique creates a signal dependent offset at the input of Sub ADC. Until it's below the tolerable level of digital error correction this is not a real problem.

D. FLIP AROUND DAC ARCHITECTURE

In Pipeline ADC the major power consuming block is first stage MDAC Op-amp. It is because of two reasons [4].

1. Higher precision demands big S/H capacitance because of thermal noise and yield limitations. With higher capacitance the slewing current increases. Also, to achieve needed gain-bandwidth product the bias current needs to be increased.

2. Thus the power consumption increases.

3. The usual MDAC architecture posses a gain of 0.5 during the Hold phase. This doubles the settling time requirement. Settling time is directly related to Gain-Bandwidth product of Op-amp. Therefore, in order to increase the GBW the bias current increases

This paper adapts a technique in which above points are addressed in such way that the power consumption reduces dramatically. The only disadvantage is the output swing is reduced by 4 times if the sampling capacitances are same. The architecture of this technique is shown in Figure5.

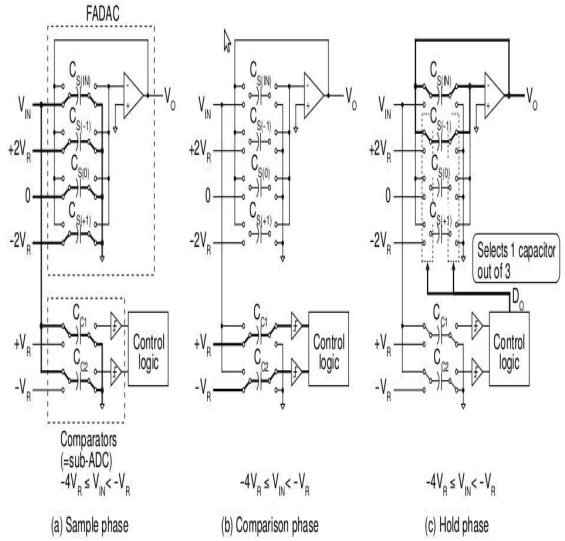

Figure 5: Block Diagram FADAC

Along with this technique the paper adapts the "Double sampling" technique which reduces settling time requirement by half [4]. Therefore the Bandwidth demand of MDAC Op-amp reduces by half. Thus the bias current linearly reduces by half.

III RESULTS AND DISCUSSION

By discussing and analyzing the results of above papers it is known that better performance is obtained in Op-amps sharing technique.

Ref No.	Technique	Specification & Results
1	Nested Digital Background Calibration	226 mW @ 3.3 V (12 Bit 20 Msps)
2	Switch Embedded Op-amp Sharing MDAC with DUAL input OTA in Pipelined ADC.	28 mW @ 1.8V (10 Bit 80 Msps)
3	Time Shifted correlated Double Sampling	67 mW @ 1.8V (10 Bit 100 Msps)
4	Flip Around Digital to Analog (FADAC)	40 mW @ 1.8V (10 Bit 125 Msps)

Table1: Performance Analyzes of Various Techniques

Other techniques also good in performance but by considering the low power consumption, high speed and high resolution Op-amp sharing technique is better suited [2]. The performance analyzes is tabulated in Table1.

IV CONCLUSION

The detailed study of above four techniques is done and the merits/demerits are listed under respective headings. Each technique is has its own advantages and disadvantages. So, it is better to choose the technique based on the end application area. The analysis shows that the selected "Op-amp Sharing" technique is well suited for low power applications.

REFERENCES

[1] "A 12-bit 20-MS/s Pipelined ADC with Nested Digital Background Calibration" X. Wang, P. J. Hurst, and S. H. Lewis

[2] "Switch-embedded opamp-sharing MDAC with dual input OTA in pipelined ADC" R. Yin, X. Wen, Y. Liao, W. Zhang and Z. Tang

[3] "A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique ' Jipeng Li, Member, IEEE, and Un-Ku Moon, Senior Member, IEEE

[4] "10-bit, 125 MS/s, 40 mW Pipelined ADC in 0.18 μm CMOS ' V Masato Yoshioka, V Masahiro Kudo.

[5] "Systematic Design of 10-Bit 50MS/s Pipelined ADC" Kehan Zhu, Sakkarapani Balagopal, and Vishal Saxena, Boise State University. 2013 IEEE on Microelectronics and Electron Devices.

[6] Thomas B.Cho and Paul R.Gray, "A 10-bit, 20MS/s Pipeline A/D Converter" IEEE J.Solid State Circuits,vol.27, Apr.2011.

[7] Andrea Panigada and Ian Galton, "A 130mW 100MS/s Pipelined ADC With 69dB SNDR Enabled by Digital Harmonic Distortion Correction" IEEE Journal of solid state circuits, vol 44, No.12 Dec.2010.

[8] "A 10 bit 200MS/S 1.8mm^2 83mW 0.13um CMOS ADC based on Highly linear integrated capacitors", Young-Ju Kim, Young-Jae Cho, D0-Hwan sa and Seung Hoon Lee. IEICE Transaction Electron Vol: 90- c No.10 Oct.2007.

[9] "A 12bit 20MS/S pipelined analog to digital converter with nested digital background calibration", Xiaoyue Wang, Paul J. Hurst, and Stephen H. Lewis, Apr.2004 Computer engineering, University of California,USA.

[10] "Design and implementation of low power 12bit 100MS/S pipelined ADC using open loop residue amplification" , Appa Rao M., Dr. Ramana Reddy P. and Cyril Prasanna Raj P. Global Journal of Researches in Engineering, Electrical and Electronics Engineering, Vol:12 Issue:11 Version 1.0 Year 2012.

