OPTIMIZED MULTIPLIER USING REVERSIBLE LOGIC GATES: A VEDIC MATHAMATICAL APPROACH

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***Abstract*-Multipliers are major components of any processor or computing machine. Digital signal processors(DSP) and performance of microcontrollers are evaluated on the basis of number of multiplications performed at unit time. Hence multiplier architectures are bound to increase the efficiency of the system. Vedic mathematics is one of the multiplier algorithms to perform multiplication operation. It is simple architecture with increased speed forms an unparalleled combination for serving any complex multiplication computations. with these additional highlights, implementing multiplier using reversible logic and further reduces power dissipation. Power dissipation is another important constraint in an VLSI design , which cannot be neglected. Here the type of multiplier is "Urdhva Tiryagbhyam(UT) multiplier". The operation of UT performs vertical and crosswise multiplication, implemented using reversible logic, which is simple procedure. This multiplier may find applications in Fast Fourier Transforms (FFTs), Embedded Systems and other applications of DSP like imaging, wireless communications. By using reversible logic implementation the speed and power dissipation is reduced. The quantum cost, garbage output, constant inputs and Total Reversible Logic Implementation Cost (TRLIC) are also reduced using reversible logic gates implementation.**

Index Terms- Vedic Multiplier, Reversible Logic, Urdhva Tiryagbhyam, TRLIC

I.INTRODUCTION

The Sanskrit word Veda is derived from the root Vid, meaning to know without limit. Vedic mathematics is one of most ancient method to perform mathematical calculations and It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus in simple way. It can perform large arithmetic operations to simple mind calculations. The
Vedic mathematics having 16 different sutras introduced by Jagadguru swami Sri Bhakti Krishna Tirtha Maharaja (1884- 1960), from that UT Vedic multiplier is one type of multiplier which performs crosswise and vertical operations between the two numbers. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time and useful in digital hardware.The beauty of vedic mathamatics is perform operations in simple way. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing etc.

With the advancement in the VLSI Technology, there is an ever increasing demand for the multiplication. Multiplication in DSP is omnipresent in almost every engineering discipline. In DSP Faster additions and multiplication operations are very important and Multiplication is the most basic and frequently used operations in a CPU(central processing unit). Multiplication is an operation performs multiplication between two binary numbers. Multiplication operations are also important for other complex operations such as convolution, Discrete Fourier Transform (DFT), Fast Fourier Transforms (FFT), etc. DSP engineers are awaited for new method and hardware implementation for the multiplication. For the multiplication DSP engineer has to concentrate on power dissipation and speed. There is a relation between power and speed. The reversible logic computation which takes zero power dissipation. So reversible logic delay is reduced .The reversible UT multiplier has been proposed. The paper is organized as follows: The section II gives the information about reversible logic along with the conventional combinational logic. Section III explains the UT Vedic multiplier algorithm. The section IV

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describes the UT multiplier using conventional logic. Section V compares the proposed design and draws a conclusion claiming the versatility of reversible UT multiplier.

II. REVERSIBLE LOGIC

A. REVERSIBLE LOGIC CIRCUITS

Energy is very important in digital system design. Irreversible circuits (conventional logic circuits) loosing one bit of information and generates heat by the second law of thermo dynamics. The irreversible logic information dissipates (KTln2) joules of heat energy, where K is Boltzmann's constant and T is the absolute temperature.

The reversible logic circuits do not dissipate energy as much as irreversible circuits. The irreversible circuits mapping between input and output is many- to-one (number of inputs=single output).Thus energy dissipation and the number of bits lost during computation are in direct prapotion. Threshold voltage and power supply applied for the circuit at that time energy consumption is reduced. In 1973, Bennett, proved that in order to avoid kTln2 joules of energy dissipation for a circuit it must be built from reversible circuits.

In Reversible logic circuits the mapping between input and output is one-to-one mapping (number of inputs=number of outputs). In reversible circuits the input data can uniquely recovered from output data .By using of this technique there is no information lost. In order to achieve low power designs Quantum computing and reversible circuits are used.

B. REVERSIBLE LOGIC GATES:

The reversible logic gates are n-input and n-output logic gates. Reversible logic is similar to the convention logic but reversible logic circuits are constructing by reversible logic gates and conventional logic gates are designed by normal gates i.e. AND, OR, XOR etc. Reversible logic gates has received great attention on power dissipation. Which is main factor in VLSI design. The synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is in reversible . However fanout in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates. From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits .We have different reversible logic gates are present for the UT Vedic multiplier.

The following constraints are the important for reversible logic circuits.

1. Minimized Constant inputs (CI): The constant inputs 0 and 1 are maintained as inputs in reversible logic in order to synthesize the given logical function.
2. Minimize the garbage: The garbage outputs which are not used in the synthesis of a required function are very essential, without reversibility we can't achieved.
3. Minimize the width of the circuit: In reversible logic one output given one time as the input of another gate .so the width of the circuit is reduced by number of additional inputs.
4. Minimize the total number of gates: Based on number of gates usage the delay of the circuit is reduced. Here we are using less number of gates for circuit implementation.
5. Quantum cost (QC): Quantum cost depends on the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1X1 or 2X2) required to realize the circuit.
6. Total Reversible Logic Implementation Cost (TRLIC): In a reversible logic circuit. TRLIC calculated as number of garbage outputs, quantum cost, constant inputs and number of Reversible logic gates .

$$TRLIC=\sum (NG+CI+GO+QC)\ldots. (1)$$

The basic reversible logic gates encountered during the design are listed below:

NOT GATE: 1X1 NOT Gate performs complement output of present input as shown in fig1(a) and gives zero quantum cost. The

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quantum implementation cost of NOT gate as shown in figure 1(b).

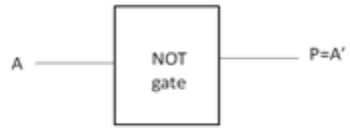

Fig1(a): Reversible NOT gate

fig1(b):Quantum implementation of NOT

FEYNMAN GATE: 2X2 Feynman Gate mainly used for fan-out purposes. It performs complementing and XOR operations are shown in fig 2(a) . It is also called as CNOT gate. The quantum cost of Feynman gate is one and the quantum implementation of Feynman gate as shown in fig 2(b).

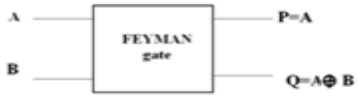

Fig2(a) :Reversible Feynman gate

Fig 2(b): Quantum implementation of Feynman gate

PERES GATE: 3X3 Peres gate performs AND, XOR, complementing operations are shown in fig 3(a). The quantum cost of Peres gate is four. The quantum implementation of Peres gate as shown in fig3(b).

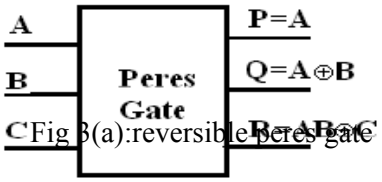

Fig 3(a):reversible peres gate

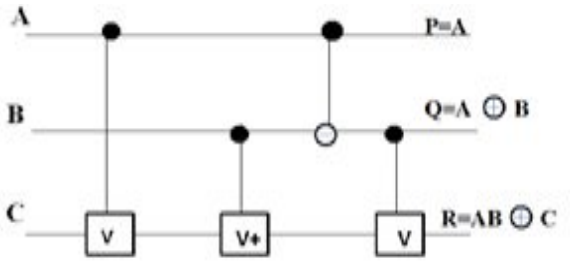

Fig 3(b):Quantum implementation of peres gate

HNG GATE: 4X4 HNG GATE Performs full adder operation as shown in fig(4) and provide minimum quantum cost. The quantum cost is six.

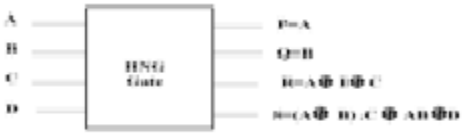

Fig4(a):Reversible HNG gate

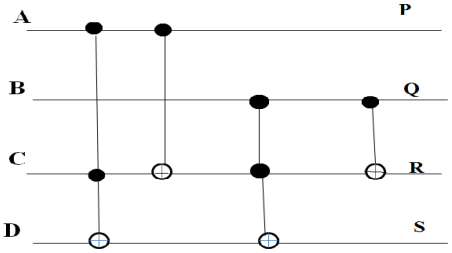

Fig 4(b):Quantum implementation of HNG gate

BVP GATE: 5X5 BVPPG Gate performs AND, XOR, complementing operation and its quantum implementation is as shown in the fig5(a). The quantum cost of BVPPG gate is ten and quantum implementation of BVPPG Gate as shown in fig 5(b).

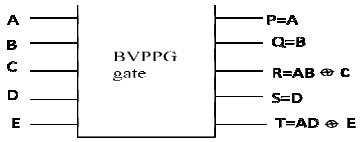

Fig5(a): Reversible BVPPG gate

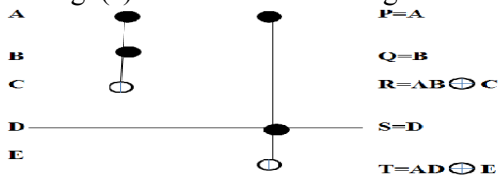

Fig 5(b):Quantum implementation of BVPPG gate

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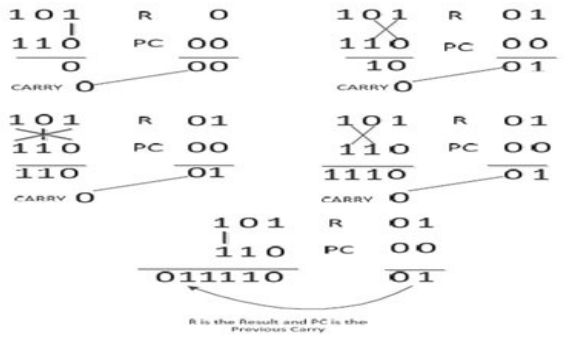
III. URDHVA TIRYAGBHYAM MULTIPLICATION ALGORITHM

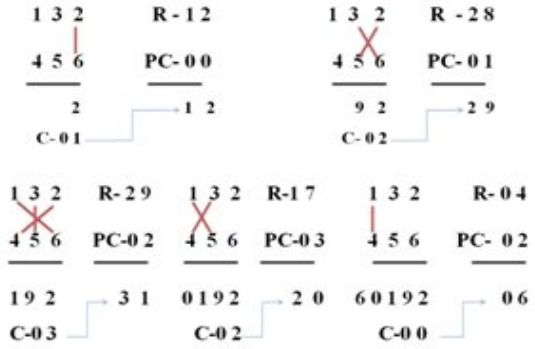
UT multiplier is one type of multiplier based on Vedic mathematical algorithm. UT sutra is the General Formula applicable to all cases of multiplication like binary, hexa and decimals. The formula itself is very short and terse, consisting of only one compound word and means "vertically and cross-wise." The applications of this brief and terse sutra are manifold. In this concept that generation of all partial products and their additions are performed. This algorithm performs nXn bit number. The partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to multipliers regular structure, it can be easily layout in a silicon chip. The Vedic Multiplier based on this sutra has the advantage that gate delay, the number of bits increases, and area increases very slowly as compared to other conventional multipliers. The binary and decimal multiplication of UT algorithm as shown in fig(7) and fig(8).



Fig(7): UT procedure for multiplication algorithm in binary form

Multiply 101 with 110:

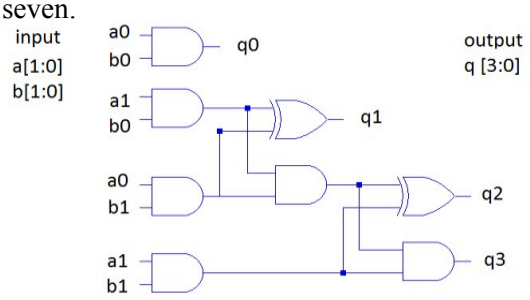
1. First take the right hand side digits of 101 and 110 i.e.'1'and '0' multiply both and result will be at LSB side.
2. Multiply 2nd right digit of top number with 1st right digit of bottom number and 1st right of top number with 2nd right of bottom number , add each other and placed at 2nd LSB position.
3. Multiply 1st left of top number with 1st right of bottom number, 1st right of top number with 3rd right of bottom number and 2nd digits of both numbers, add each other and result place at 3rd LSB position.
4. This step is similar to 2nd step, move one place to left and multiply the numbers and place the result at 4th LSB position.
5. Finally multiply 1st right digits of top and bottom numbers, place that result on next LSB position and if it having any carry place at MSB position either '1' or '0'. That result will be the final product of 101 and 110. Procedure is same for decimal(fig(8)) multiplication also.



Fig(8): Urdhva Tiryagbhyam procedure for multiplication algorithm in decimal form

IV. EXISTING METHODS

Conventional logic design implementation of 2X2 Urdhva Tiryagbhayam multiplier with irreversible logic as show in fig (9).Here we have four expressions by using irreversible logic and numbers of gates are seven.



Fig(9): Conventional 2X2 Urdhva Tiryakbhyam Multiplier.

The 2X2 multiplier circuit using reversible logic implementation as shown in fig (10). This reversible logic does n't allow the fan outs. The performance of the UT multiplier is optimizing

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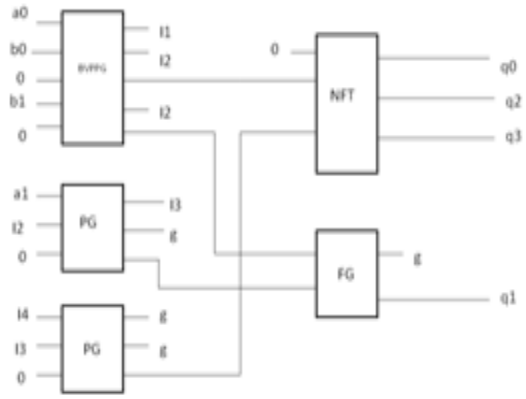
each individual unit in terms of quantum cost, garbage outputs etc.

A.2X2 URDHVA TIRYAGBHYAM MULTIPLIER:

The design expressions of multiplier can be logically modified, so as to optimize the design. This optimized design makes use of on considers the fan out using BVPPG, two Peres gates, one Feynman gate and one NFT gate as shown in the figure (10) .

The new optimized circuit quantum cost of the circuit is 24; number of garbage outputs as 4, number of gates 5 and the number of constant inputs is 5. I1, I2, I3 and I4 are the intermediate outputs that are used for the purpose of fan-out.



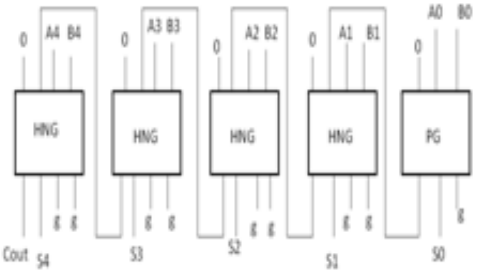
Fig(10): Design of 2X2 UT multiplier using reversible logic

B.4X4 URDHVA TIRYAGBHYAM MULTIPLIER

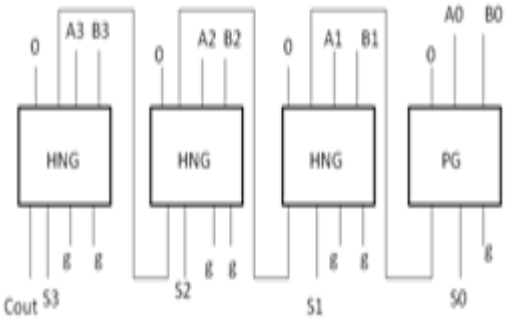
The reversible 4X4 Urdhva Tiryagbhyam Vedic multiplier design can be implemented by using 2X2 multiplier. By using four 2X2 multipliers the 4x4 multipliers are implemented .2x2 multiplier as show in fig (10). Each 2X2 multiplier of which procures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication and two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these two four bit ripple carry adders are in turn 5 bits each which need to be summed up. This five bit ripple carry adder generates a six bit output. These six bits from the upper bits of the final result.

B.DESIGN OF RIPPLE CARRY ADDERS

By using all HNG gates quantum cost and garbage outputs are more .so the ripple carry adder is modified as one Peres gate can efficiently replace a HNG. Then the number of HNG gates is 4 and one Peres gate. This 5 bit ripple carry adder is used in the second stage of the 4X4 Urdhva Tiryagbhyam Multiplier. Since for any ripple carry for the first full adder is zero, this implicitly means the first adder is a half adder. Thus a Peres gate HNG.



Fig(11):5-Bit ripple carry adder



Fig(11): 4-Bit ripple carry adder

This cut down the quantum cost by two for any ripple carry adder and the garbage output by one. The Constant inputs and the gate count remain constant. The 4X4 UT multiplier structure is as shown in figure (13).

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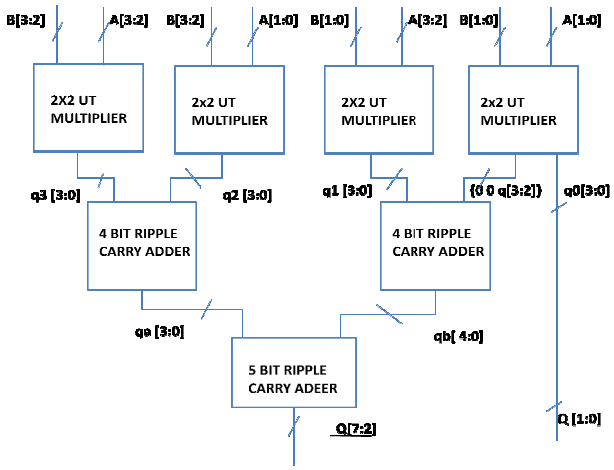
The design of the UT multiplier reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i and MODELSIM. The simulation results are as shown in figures 10 and 11 respectively. The following are the important design constraints for any reversible logic circuits.

V. RESULTS AND COMPARISONS

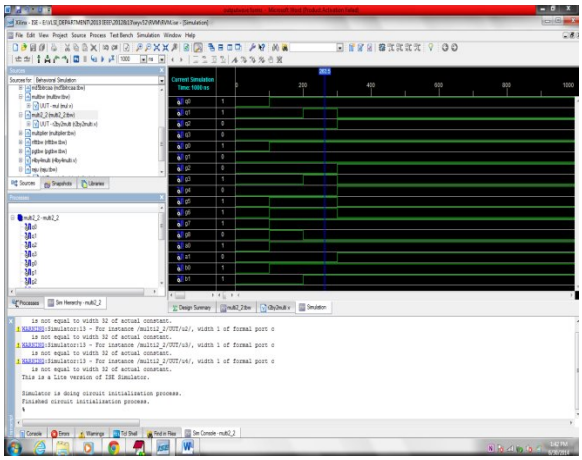
The design of the Urdhva Tiryagbhyam multiplier reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i and MODELSIM. The simulation results are as shown in figures 10 and 11 respectively. The following are the important design constraints for any reversible logic circuits.

1. Quantum cost of Reversible logic circuit should be minimum.
2. Number of garbage outputs of Reversible logic circuit should be minimum.
3. Number of constant inputs of Reversible logic circuit should be minimum.
4. Number of reversible gates of Reversible logic circuit should be minimum.

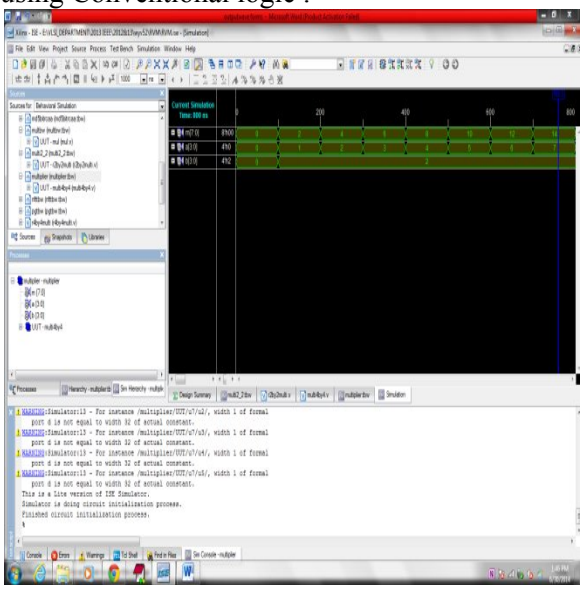


Fig(14):Block diagram of 4X4 UT multiplier

Total reversible logic implementation cost calculated as summing of all constraints and based on above constraints the total reversible logic implementation cost is reduced. The 4X4 Vedic multiplier using reversible logic compared with another multipliers as shown in table 1. The 4x4 multipliers are take care of fan outs also. So the quantum cost of 2x2 UT multipliers quantum cost is increased compare to previous designs.



Fig(14):Output waveform for 2X2 Multiplier using Conventional logic .



Fig(15):Output waveform for 4X4 Multiplier using Reversible logic.

CONCLUSIONS

The main aim of UT algorithm is mainly to design a low power and high speed multipliers using reversible logic gates. This is the optimized design as compared to conventional multiplier. The efficiency of reversible logic circuit is realized in terms of number of gates, quantum cost, constant inputs, and garbage outputs. If these parameters are less the circuit is efficient. By reducing these parameters the TRLIC is reduced and also lower

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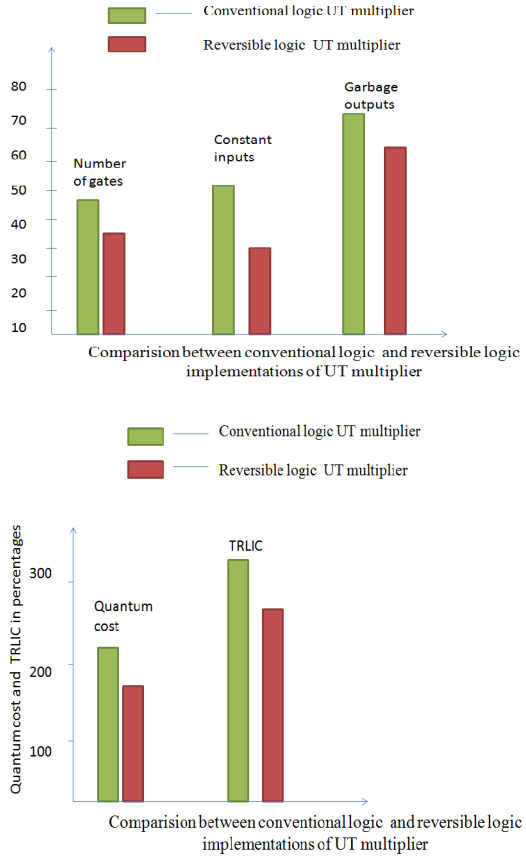
TRLIC implicitly means lower the quantum cost, hence lower the delay and vice versa. Besides combining the design criterion that fan-out must be generated with the reversible logic. The further optimization of the circuit in terms of high speed and low power as future work.



Fig(16) :graph between conventional logic and reversible logic components of UT multiplier.

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