Leakage Power Reduction Using Power Gating And Multi-Vt Technique

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Abstract -In today's deep sub-micron SoCs, power lose has become an important parameterin the power consumption techniques.The objective of many networking and consumer products is to meet performance goal with the lowest achievable power. Leakage power especially becomes considered carefully for portable consumer applications. There are various techniques bring it up to optimize for leakage-power including power shut-down of logic modules, using mixed threshold libraries. Each of these approaches in power saving is associated with flow planning,Performance implementation and verification challenges. Power gating is a very popular technique to reduce the leakage power.It is a technique used in integrated circuit design to reduce power consumption, where blocks are powered down when not in use and also to reducing stand-by or leakage power the implementation of power gating using power switches and the isolation and the retention techniques have been touch upon.Power management is a design which uses Power Gating techniques as a reference.Calculation of the number of power switches required, its effects on IR drop and other trade-offs are also studied.

Index Terms - Leakage power,Power gating,Column Based Methodology, IR-Drop.

I.INTRODUCTION

A direct consequence of Moore's law is that the "power density of the integrated circuit increases exponentially with every technology generation".

Since the 1970s, most popular electronics manufacturing technologies used bipolar and NMOS transistors. However, bipolar and NMOS transistors consume energy even in a stable combinatorial state, and consequently, by 1980s, the power density of bipolar designs was considered too high to be indefinite. IBM and Cray started developing liquid, and nitrogen cooling solutions for high-performance computing systems. The 1990s lower-power CMOS technology was introduced. CMOS transistors consume lower power largely because, to a first order of exact calculation, power is dissipated only when they switch states, and not when the state is steady. Now, in the late 2000s, we are witnessing a paradigm shift in computing the shift to multi-core computing. The power density has once again increased so much that there is little option but to keep the hardware simple, and transfer complexity to higher layers of the system design abstraction, including software layers.

This paper providing the detailed explanation of the power consumption and dissipation in the operation of CMOS transistors,and also examining the fundamental mechanisms for power reduction. Leakage power is primarily due to the sub-threshold currents and reverse biased diodes in a CMOS transistor. Thus,

$$P_{total} = P_{dynamic} + P_{short\_circuit} + P_{leakage}$$

(A) Leakage Power

Even though a transistor is in a stable logic state, just because it is powered-on, it continues to leak small amounts of power at almost all junctions due to various effects.(1) Reverse Biased Diode Leakage, (2) Gate Induced Drain Leakage (3) Gate Oxide Tunneling (4) Sub-thresholdLeakage.

In the below fig 1.1 when the input of inverter is high, a reverse potential difference of Vddis established between the drain and the n-well, which causes diode leakage through the drain junction. In addition, the nwell region of

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the pMOS transistor is also reverse biased with respect to the p-type substrate.

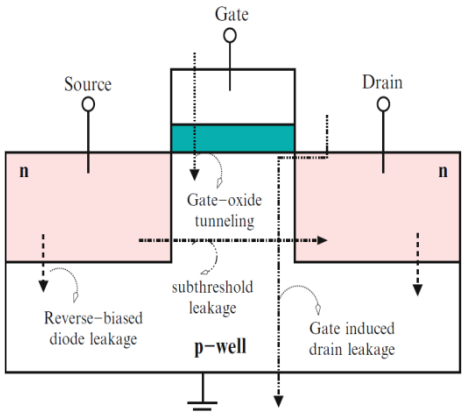

Fig 1.1 Components of Leakage Power: (i) Sub-threshold current flows between source and drain;(ii) Reverse-biased diode leakage flows across the parasitic diodes; (iii) Gate induced drain leakage flows between the drain and substrate

(B) Power Gating

Power Gating is an extremely effective scheme for reducing the leakage power of idle circuit blocks. The power (Vdd) to circuit blocks that are not in use is temporarily turned off to reduce the leakage power. When the circuit block is required for operation, power is supplied once again. During the temporary shutdown time, the circuit block is not operational – it is in low power or inactive mode. Thus, the goal of power gating is to minimize leakage power by temporarily cutting-off power to selective blocks that are not active.

Power gating is implemented by a pMOS transistor as a header switch to shut off power supply to parts of a design in standby or sleep mode. nMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into two parts: a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

In addition, coarse-grain power gating results in a large switched capacitance, and the resulting rush current can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this. Finally, since power gates are made of active transistors, the leakage of the power gating transistor is an important consideration in maximizing power savings.

II.RELATED WORK

A top-down design methodology to implement fine-grained RTPG. The primary contributions of this work are two-fold: a proposal for a design flow to use locally extracted sleep signals for fine-grained RTPG, and an analytical model to estimate the break-even point for applying the RTPG to fine-grained domains.They use a local virtual ground scheme in which logic cells and power switch cells within a PG-domain are connected with a local virtual ground line the power switch cell contains an NMOS power switch transistor whose drain and gate are connected to a virtual ground pin and an enable pin, respectively. The virtual ground pin of logic cells are connected to those of power switch cells through a local virtual ground line, which is routed as an inter-cell wire at the routing stage.The main advantages are Exploiting Enable Signals of Gated Clock, Algorithm to Partition into Power Gating Domains.

The Integer Linear Programming was introduced. This technique is used to improve the effectiveness of negative-bias temperature instability and also reduce leakage power consumption and also propose a virtual input pin technique to improve leakage reduction and use path sensitization to reduce area overhead. The main contribution of this paper is to propose an ILP formulation for a TG-based technique intended to reduce the NBTI effect and leakage simultaneously.

The critical challenges and present a low power methodology that was developed and applied to a high performance SoC during the physical design phase. It presents the details of the power optimization methods and techniques used during the physical design implementation using Synopsys IC Compiler, Star RC and Prime Time-SI. It also presents the IC Compiler and Prime Time-SI based signoff-opt FSLR (Final Stage Leakage Recovery) flow adopted to further achieve the leakage power saving goals.

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Leakage power has been an integral step throughout our design flow. Final Stage Leakage Recovery (FSLR) is one such technology from Synopsys which is based on sign-off based optimization algorithms. The underlining technique of FSLR is to swap high leakage cells with low leakage cells while simultaneously preserving the timing. The unique algorithm in FSLR looks across all Vt libraries to find the best fit for cell swapping to improve the leakage power but at the same time preserve the timing QoR of the design. FSLR based optimization is added on top of the power optimization used throughout the IC Compiler based physical implementation flow. FSLR provides significant gain in leakage power; however, it comes with its own challenges depending on the design flow, use of different threshold voltage libraries, and number of sign-off corners, resource requirements and flow setup.

The static, statistical variations coming from process variability.The proposed of a Monitor and Control design methodology that improves the timing yield of a system by using sleep transistors (used in the traditional power-gating paradigm) as power and performance control knob.

In particular a new design of a tunable-size sleep transistor and its implementation as a new cell in an industrial technology library.A methodology for inserting in a row-based fashion, the tunable-size sleep transistors; 3)a clustered power-gating strategy for power-gating, by means of tunable-size sleep transistors, the timing critical cells only for minimizing area and power overhead.

Experimental results has shown that the proposed design methodology guarantees 100% of timing yield with a leakage power savings of about 29% during the standby periods.

III. PROPOSED WORK

In power gating designs, one extra component, called sleep transistor, is needed. Sleep transistor is used to cut-off the power supply to the shut-off blocks. Sleep transistor can be composed of either PMOS or NMOS, depending on the needs to cut off power or ground.

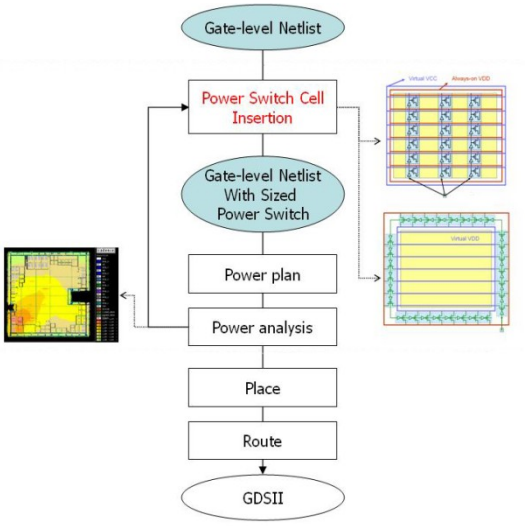

Fig.3.1 Flow Chart of Power Gating Design

First, the sleep transistors are treated as resistance in the whole chip power plan. Resistance induces voltage difference, or IR drop, among power plan. The value of resistance caused by sleep transistor is inverse proportional to its size. That is, the larger switches induce smaller IR drop. However, the larger switches occupy more area and dissipate more leakage as well. It is important to find out the optimal size of sleep transistor in order to save chip area and IR drop. The size of sleep transistor has strong relation to the gate count of driven logics. Through static power analysis, the sleep transistor fabric can be decided with respect to acceptable IR drop.

(A) Principles of power gating design

Power gating consists of selectively powering down certain blocks in the chip while keeping other blocks powered up.

Internal switches are used to control power to selectedblocks.In below it shows a block diagram of a SoC using power gating techniques. Power gating controller provides the control signal to the power switching fabric.Power gated block receives its power through a power switching fabric. Power switching fabric typically consists of large

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number of CMOS switches distributed around or within the power gated block.

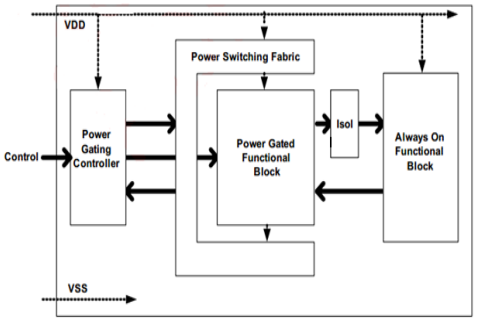

Fig 3.2 SoC using power gating techniques.

Power switching network switches either VDD or VSS to the power gated block. In this example VDD is swapped, VSS is provided directly to the entire chip. One challenge for power gating design is that the output of power gated block may ramp off very slowly. The result could be that these outputs spend a significant amount of time at threshold voltage, causing large crowbar currents in the always powered on block. To prevent the crowbar currents, isolation cells are placed between the outputs of power gated blocks and inputs of always powered on block. Isolation cells are designed so that when one of the inputs is at threshold, as long as the control input is off. Power gating controller provides this isolation control signal. For some power gated blocks, it is highly desirable to retain the internal state of the block during power down, and to restore this state during power up. Such retention strategy can save significant amount of time and power during power up. One way of implementing such retention strategy is to use retention register instead of normal flip -flops.

(B)Methods of power switching

There are two methods of power gating

1.Fine –grain power gating

2.Coarse-grain power gating.

1.Fine-grain power gating

In fine-grain power gating switch is placed locally inside each standard cell in the library. The main Disadvantage is the size of the gate control is designed with the worst case consideration that this circuit will switch during every clock cycle. This is the only way to size, as the module level function is not known at this time. This is the biggest disadvantage of this method.

2. Coarse-grain power gating

In coarse-grain power gating, a block of gates has its power switched by a collection of switch cells. Two prominent ways of implementing a coarse-grain structure have emerged

2.1 Ring-based methodologies.

2.2 Grid-based methodologies.

2.1 Ring based implementation

In a ring-based methodology, the power switches are placed around the perimeter of the module that is being switched-off as a ring. In coarse-grain power gating, a ring of VDD surrounds the power gated block. A ring of switches connects VDD to a switched or virtual VDD (VVDD) power mesh that covers the power gated block.

It has the advantages of less complex power plan than the grid style because of separation of the permanent power network and the virtual power network.Virtual power network is not mixed with other logic cells.The major drawback is that it does not support retention registers, since the require access to the always on supply.Cost is high compared to a grid approach.

2.2 Grid based implementation

It requires fewer sleep transistors to achieve IRdroptarget.The permanent power supply is available across the power-down domains areas. Consequently, special cells, such as retention registers and always-on buffers, which require the permanent power supply, can be connected to the permanent power network in the power-down areas.It provides better trickle charge distribution for management of in-rush current.It has a less impact on the area of a power gated block. Typically the utilization of any blocks is less than 100%, so there are places where switch cells can be placed without increasing the area of the block.

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(A) Column based grids

In the grid style (column based) of implementation the power switches are placed throughout the power gated region. They form a grid to connect permanent power network and switched power network. A column based topology employs columns of switch cells spaced evenly across the switched design. These switch cells effectively switch the power rail to each segment of a standard cell row and provide very fine control over the switching function. Each power switch only has to provide power to a small segment of the standard cell row thereby minimizing any potential voltage drop problem.

(B) Row based Grids

The row based approach can impact routing resources in lower layer metal. This problem can be avoided in column based approach, the lower layer power straps can be routed in metal 2 directly above the power switches with minimal impact to routing resource.

Among those types of implementation Grid style implementation is the right choice. In the grid style implementation, use wide straps in the permanent power network to reduce the IR drop. The virtual power network should be implemented at metal 1 and metal 2 layers with narrow straps sufficient to drive local logic cells and satisfy the IR drop target. It is worth nothing that the total IR drops in the permanent power network, the sleep transistor and the virtual power network. It is preferable to minimize IR drop in the permanent power network so as to make it easier to achieve to total IR drop specification with fewer sleep transistors.

Switch cells

Power switches of a power management design. Switch cells are special library cells that act as a connection point between two voltage rails when they are turned on and a break point in the current path between the two rails when they are turned off. Turning off the power gating cells causes the switched rail to be disconnected from its source, which removes power from all cells connected to that switched rail.

Signal isolation

Every interface of a power gated region needs to be managed. We need to ensure that powering down the region will not result in crowbar current in any of the powered up blocks. We need to ensure that none of the floating outputs of the power down mode block will result in spurious behavior in the power-up blocks.

Isolation cells

Isolation cells are used to prevent short circuit current. As the name indicates these cells isolate power gated block from the normally ON block. Isolation cells are specially designed for low short circuit current when input is at threshold voltage level. Isolation control signals are provided by power gating controller. Usually a simple OR/AND logic can function as an output isolation device. There are three basic types of isolation cells: to clamp the signal to “0”, to clamp the signal to “1”, and to latch the signal to the most recent value.

Isolation cells require permanent power supply and are recommended to be placed inside the power gated block near the boundary.

Retention registers

The main register is powered by switched power rail. The CLK, D and RESETN pins operate on the main register .The shadow register is powered by always on rail. When RETAIN goes high state of main register is loaded into the shadow register and when RETAIN goes low state of shadow register is loaded back into the main register.

IV. RESULTS ANALYSIS

The grid style implementations are the better IR-drop management because each sleep transistor drives local cells. The ring style sleep transistor implementation could result in moreIR-drop at center of the design due to the

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limited drive of the sleep transistors distance from the center.

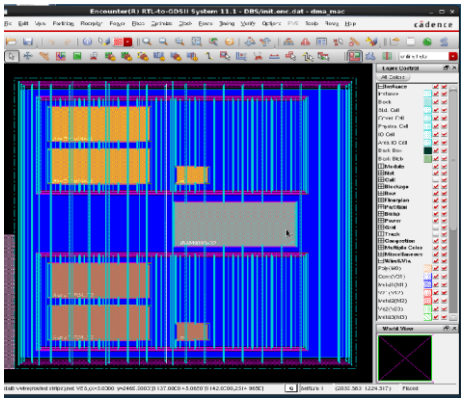

Fig 5.1 Power Switch Insertion

These 5.1 Figure Shows those switches are inserted in the switchable domains after power domain floor plan by addPowerSwitch.

Switch Cell Placement Constraints

In a column based switch cells they effectively switch the power rail to each segment of a standard cell row and provide very fine control over the switching function.

Number of Switch Cells and its effect on IR drop-

The drop between VDDC and VDD of each switch cell determines the number of switch cells to be used in a design. We have done a case study on a 45nm subchipof die size 146.7 X 146.7u, with different number of switch cells. With increase in the number of switch cells, VDD drop decreases and the voltage drop for each switch cell between VDDC and VDD decreases at the cost of increased routing resources.

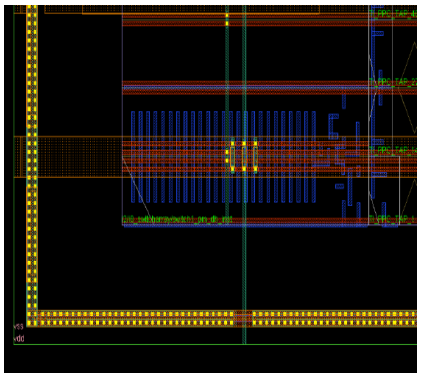

Fig 5.2 Switch cell Placement

Table 5.1

Ring based - IR drop report

Node	X(um)	Y(um)	Layer	Voltage drop	Percentage of supply
1336	130.860	142.575	MET2	11.736mV	1.40%
1338	130.860	142.425	MET2	11.736mV	1.40%
1337	127.260	142.575	MET2	11.735mV	1.40%
1339	127.260	142.425	MET2	11.735mV	1.40%
1206	145.440	142.575	MET2	11.734mV	1.40%
1205	145.440	142.425	MET2	11.734mV	1.40%

Table 5.2

Grid Based (Column) - IR Drop report

Node	X(um)	Y(um)	Layer	Voltage drop	Percentage of supply
1300	145.440	87.225	MET2	8.480mV	1.01%
1298	145.440	84.975	MET2	8.480mV	1.01%
1303	145.440	87.375	MET2	8.480mV	1.01%
3444	130.860	87.225	MET2	8.480mV	1.01%
3527	130.860	84.975	MET2	8.480mV	1.01%
3485	141.660	87.225	MET2	8.480mV	1.01%

Table 5.1 and Table 5.2 illustrate the IR drop report in a Ring based and Grid based manner. From these tables it is clear that there is a

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Maximum IR drop goes down from 1.40% to 1.01%.

V. CONCLUSION

Leakage power reduction has become one of the main optimization challenges for today's sub-micron design. This paper described about power gating & leakage power optimization techniques using Cadence-Encounter tool. In order to meet the power consumption target, leakage power optimization is a main focus throughout this paper. Power switches added to the Power-Gating domains are dynamically controlled by the enable signals to reduce active leakage power. Although the concept of sleep transistor is simple, best sleep transistor design and implementation require optimizing all together the gate length, width and body bias with overall opinion of effective, leakage, drive, area and IR-drop effects which are often conflicting and need to be weighted based on application requirements.

Case studies prove that with the increase in number of switch cells and associated changes in power routing, the total vdd IR drop and the IR drop for each switch cells between vdd and vddc deceases. Isolation cells should be used in a power gating design to avoid the short circuit current due to the floating outputs during power down mode. Retention flops can be used to store the state during power down mode so that it can be retrieved during power up.In future the wok can be extended by adding Multi-Vt technique along with the coarse grain to analyze how efficiently we can reduce leakage power.

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