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Comparative Performance Analysis of Different CMOS Adders Using 90nm and 180nm Technology

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***Abstract* — Adders are key components of digital design and are necessary part of any digital signal processor (DSP) architecture and microprocessors. Apart from the basic addition they also perform other operations such as subtraction, multiplication, division, address calculation. Adders of various bit widths are frequently required in Very Large Scale Integration (VLSI) circuits from processors to Application Specific Integrated Circuits. In most of these systems the adder lies in the critical path that determines the overall performance of the system. In this paper, different type of 8-bit full adders are analyzed and compared for transistor count, power dissipation, delay and power delay products. The investigation has been carried out with simulation runs on Tanner environment using 180nm & 90nm CMOS process technology at 2V. The result shows that the carry skip adder has the lowest power-delay product.**

***Index Terms* — Carry Select Adder, Carry Increment Adder, Carry Skip Adder, Carry Look-Ahead Adder, Area-Efficient, 8-Bit Adder, CMOS, Power Delay Product.**

I. INTRODUCTION

Continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing Modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. The carry-ripple adder is composed of many cascaded single-bit full-adders. The circuit architecture is simple and area-efficient. However, the computation speed is slow because each full-adder can only start operation till the previous carry-out signal is ready. The other types of adder circuits such as carry look-ahead adder, carry skip adder, carry select adder and carry increment adder are more complex than the conventional carry ripple adder and consume more power but these are very fast in operation.

The research efforts of the past years in the field of digital electronics have been directed towards the low power of digital systems. Recently, the requirement of probability and the moderate improvement in battery performance indicate power dissipation is one of the most critical design parameters day by day the demand of probability and mobility is increasing. Also the area of chip design is taken into consideration while talking about probability. Hence three most widely accepted parameters to measure the quality of a circuit or to compare various circuit styles are area, delay and power dissipation.

There are three major sources of power consumption in digital CMOS circuits, which are summarized in the following equation**.**

$$P_{total} = P_{switching} + P_{short\text{-}circuit} + P_{leakage}$$

$$= (\alpha_{0\to1} \times C_L \times V_{dd}^2 \times f_{clk}) + (I_{sc} \times V_{dd}) + (I_{leakage} \times V_{dd}) \quad (1)$$

The first term represents the switching component of power, where C is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0\to1}$ is the node transition activity factor. The second term is due to the direct path short circuit currents, I_{sc}, which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current, $I_{leakage}$, which can arise from substrate injection and sub threshold effects, is primarily determined by fabrication technology considerations. However, while supply voltage reduction is the most effective way to reduce the power consumption, such a reduction require new design methods for low-voltage and low power integrated circuits. Since an average of 15-20% of the total power is dissipated in glitching, low power can also be achieved by reducing the glitches of the circuit.

Propagation delay and power dissipation generally form a design trade off improve one and you degrade the other!

To quantify how effective or efficient a digital design technology is in terms of delay and power; we use the product of the propagation delay and the power dissipation. To measure system efficiency we look at the power delay product of system.

This paper is organized as follows. In Section II, we will review the different adder architectures. Section III describes the simulation results and the conclusions are summarized in Section IV.

II. ADDER ARCHITECTURES

Multiple-bit addition can be as simple as connecting several full adders in series or it can be more complex. How the full adders are connected or the technique that is used for adding multiple bits defines the adder architecture. Architecture is the most influential property on the computation time of an adder. This property can limit the overall performance. In general the computation time is proportional to the number of bits implemented in the adder. Many different adder architectures have been proposed to reduce or eliminate this proportional dependence on the number of bits. Several adder architectures are reviewed in the this section.

A. Ripple Carry Adder (RCA)

An n-bit ripple carry adder consists of N full adders with the carry signal that ripples from one full-adder stage to the next, from LSB to MSB. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. Each full adder inputs a Cin which is the Cout of the previous adder. Addition of k-bit numbers can be completed in k clock cycles. A N-bit ripple carry adder structures is shown in Fig. 1.

The ripple-carry adder has many advantages like low power consumption, low area and simple layout. The drawback of the ripple carry adder is its slow speed because each full adder must wait for the carry bit to be calculated from the previous full adder.

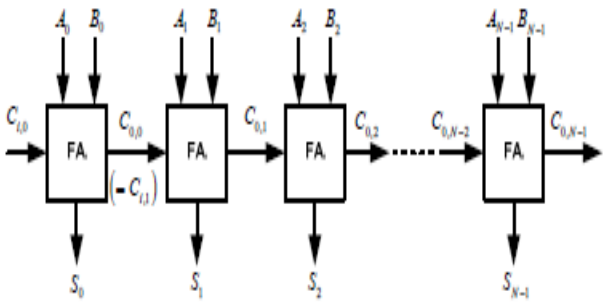

Fig. 1 N-bit Carry Ripple Adder

B. Carry Select Adder (CSA)

The carry select adder comes in the category of conditional sum adder. The carry select adder is constructed by sharing the common Boolean logic term in summation generation. To share the common Boolean logic term, only one XOR gate with one INV gate is needed to generate the summation signal pair as shown in Fig. 2. As the carry-in signal is ready, we can select the correct summation output according to the logic state of carry-in signal. As for the carry propagation path, we construct one OR gate and one AND gate to anticipate possible carry input values in advance. Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of carry-in signal.

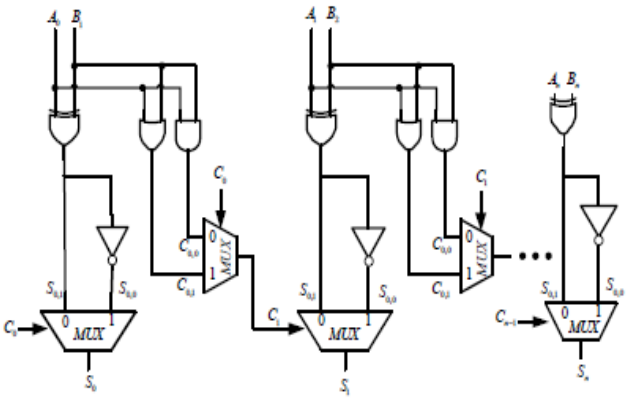

Fig. 2 Carry Select Adder

C. Carry Skip Adder (CSKA)

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder. The carry-skip adder is much like the RCA only it has a carry bypass path. This architecture divides the bits of the adder into an even number of stages M. Each stage M has a carry bypass path that forwards the carry-in of the Mi stage to the first carry-in of the Mi+1 stage. If the binary inputs are such that the carry would normally ripple (or propagate) from the input of the Mi stage to the input of the Mi+1 stage, then the carry takes the bypass path. The Carry Skip Adder reduces the delay

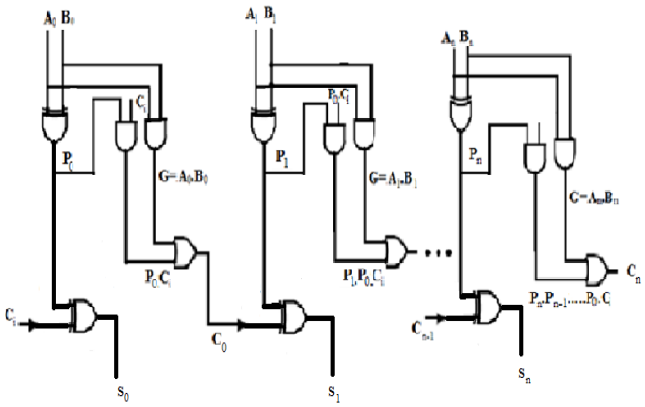

Fig. 3 Carry Skip Adder

due to the carry computation i.e. by skipping over groups of consecutive adder stages.

D. Carry Look-ahead Adder (CLA)

To reduce the computation time, faster way is to add two binary numbers by using carry look ahead adders. It is done by creating two signals (P and G) for each bit position, based on if a carry is propagated through from a less significant bit position (at least one input is a '1'), a carry is generated in that bit position (both inputs are '1'), or if a carry is killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half-adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created.

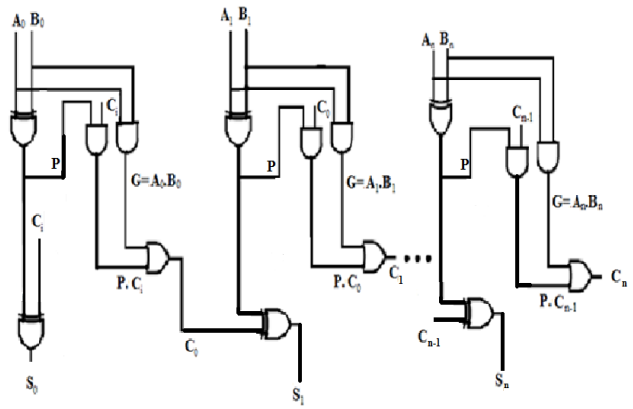

Fig. 4 Carry Look-ahead Adder

In carry look-ahead architecture instead of rippling the carry through all stages (bits) of the adder, it calculates all carrys in parallel based on equation (2).

$$Ci = Gi + Pi \cdot Ci\text{-}1 \qquad (2)$$

In equation (2) the Gi and Pi terms are defined as carry generate and carry propagate for the ith bit. If carry generate is true then a carry is generated at the Ith bit. If carry propagate is true then the carry-in to the Ith bit is propagated to the carry-in of i+1 bit. They are defined by equations (3) and (4) where Ai and Bi are the binary inputs being added.

$$Gi = Ai \cdot Bi \qquad (3)$$

$$Pi = Ai \oplus Bi \qquad (4)$$

E. Carry Increment Adder (CIA)

In carry increment adder architecture instead of computing two results for each block and selecting the correct one, only one sum is calculated and incremented afterwards if necessary, according to the carry input. Thus the second adder and the multiplexers in the carry-select scheme can be replaced by a much smaller incrementer structure as shown in Fig. 5. Put differently, the computation of a second sum and carry bit is reduced to the generation of a propagate signal per bit position.

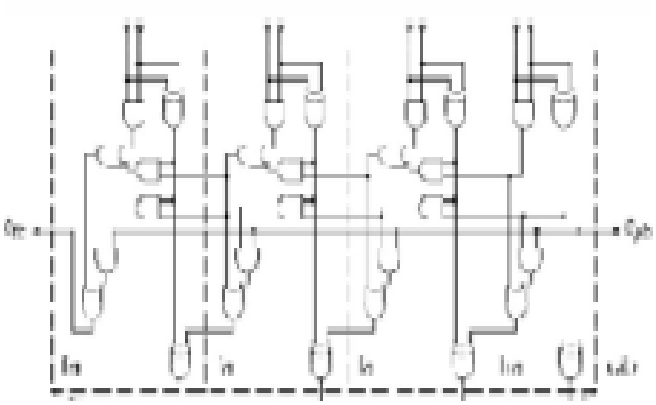

Fig. 5 Carry Increment Adder

III. SIMULATION RESULTS

The different adder circuits are designed in Tanner tool (S-edit, T-SPICE) using CMOS. The simulations are carried out to determine the performance comparison regarding number of transistors, propagation delay, power consumption and power delay product (PDP).

Table I shows the simulation results for adder's performance using 90nm technology and 2V supply voltage.

ADDER	NO. OF TRANS ISTORS	POWER DISSIPA-TION	DELAY	PDP
CSKA	240	32.061uW	0.14ns	4.488*10^-15
CLA	240	32.83uW	0.1401ns	4.599*10^-15
CSA	256	54.198uW	0.476ns	25.798*10^-15
CIA	284	354.556uW	0.1574ns	55.807*10^-15

Table I Simulation results using 90nm technology

Table II shows the simulation results for adder's performance using 180nm technology and 2V supply voltage.

ADDER	NO. OF TRANS ISTORS	POWER DISSIPA-TION	DELAY	PDP
CSKA	240	27.046uW	0.1331ns	3.599*10^-15
CLA	240	27.287uW	0.1333ns	3.637*10^-15
CSA	256	44.894uW	0.4798ns	21.54*10^-15
CIA	284	155.097uW	0.1278ns	19.821*10^-15

Table II Simulation results using 180nm technology

IV. CONCLUSION

In this paper, different type of adders (Carry Skip, Carry Look Ahead, Carry Select and Carry Increment) has been designed and evaluated on power, delay and area parameter. Both Carry Skip and Carry Look Ahead uses least number of transistors while Carry Increment has highest number of transistors i.e. 284 transistors. The Carry Skip Adder (CSKA) has the least Power Delay Product (PDP) in both 180nm and 90nm technology implementation. The overall performance of Carry Look Ahead Adder is comparable to that of Carry Skip Adder in both implementations. The delay of Carry Increment Adder is lowest among all adder types in 180nm technology and hence it emerges as the fastest adder but its power dissipation is very high.

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