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Signal Delay Control Based on Different Switching Techniques in Optical Routed Interconnection Networks

Ahmed Nabih Zaki Rashed
Electronics and Electrical Communications Engineering Department
Faculty of Electronic Engineering, Menouf 32951, Menoufia University, EGYPT
E-mail: ahmed_733@yahoo.com

Abstract- This paper has investigated the different switching techniques to reduce signal latency for different optical interconnection network architectures that provide sufficient quality of service (QoS) and are suitable for reconfigurable systems. The network parameters, like network topology, routing, and switching are taken into consideration in order to meet the specific requirements of the system that enables QoS. As well as the study suggest different switching techniques to control signal latency in optical routed interconnection networks.

Keywords— Switching techniques, Signal latency, QoS, Interconnection networks, and Routing signal.

I. INTRODUCTION

The performance of most digital systems today is limited by their communication or interconnection, not by their logic or memory [1, 2]. In the fourth generation systems today, most of the power is used to drive wires and most of the clock cycle is spent on wire delay, not gate delay. As technology improves, logic components become small, fast and inexpensive. The pin density and wiring density that govern interconnections between system components are scaling at a slower rate than the components themselves [3]. Also, the frequency of communication between components is lagging far behind the clock rates of modern processors. These factors combine to make interconnection the key factor in the success of future digital systems. Interconnection networks are currently being used for many different applications, ranging from internal buses in very large-scale integration circuits to wide area computer networks. Among others, these applications include backplane buses and system area networks, telephone switches, internal networks for asynchronous transfer mode (ATM) switches, processor/memory interconnects for vector supercomputers, interconnection networks for multicomputers and distributed shared-memory multiprocessors, clusters of workstations, local area networks, metropolitan area networks, wide area computer networks and networks for industrial applications. Additionally, the number of applications requiring interconnection networks is continuously growing. [4].

The theory of the interconnection networks was initially developed for board-level implementations. In a System on a Chip context big part of the assumptions have to be reevaluated and potentially changed in order to reflect the effects of very large scale integration and deep sub-micron technologies [5, 6]. Especially, the assumptions about the cost of the links are going to change a lot. There are many factors that may affect the choice of an appropriate interconnection network for the underlying parallel computing platform. These factors include: Performance requirements: Processes executing in different processors synchronize and communicate through the interconnection network. These operations are usually performed by explicit message passing or by accessing shared variables. Message latency is the time elapsed between the time the message is generated at its source node and the time the message is delivered at its destination node. Message latency directly affects processor idle time and memory access time to remote memory locations. Also, the network may saturate, it may be unable to deliver the flow of messages injected by the nodes, limiting the effective computing power of a parallel computer. The maximum amount of information delivered by the network per time unit defines the throughput of that network. Scalability: A scalable architecture implies that as more processors are added, their memory bandwidth [7], I/O bandwidth and network bandwidth should increase proportionally. Otherwise the components whose bandwidth does not scale may become a bottleneck for the rest of the system, decreasing the overall efficiency. Incremental expandability: Interconnection networks should provide incremental expandability, allowing the addition of a small number of nodes while minimizing resource wasting. Simplicity: Simple designs often lead to higher clock frequencies and may achieve higher performance [8, 9].

II. MODEL ANALYSIS BASED ON DIFFERENT SWITCHING TECHNIQUES

Switching techniques have a very strong impact on the performance and the behavior of the interconnection network. Performance is more heavily influenced by the switching technique than by the topology or the routing algorithm. Switching techniques also have a considerable influence on the architecture of the router [9].

II. 1. CIRCUIT SWITCHING

In circuit switching, a physical path from the source to the destination is reserved prior to the data transmission. This is realized by injecting the routing header into the network. This routing probe contains the destination address and some additional control information. This routing probe progresses towards the destination node reserving physical links as it is transmitted through intermediate routers. When the probe reaches the destination, the complete path has been set up and an acknowledgement is sent back to the source. The message contents may now be transmitted at the full bandwidth of the hardware path. The circuit may be

released by the destination or by the last few bits of the message. Circuit switching is generally advantageous when messages are long and infrequent, i.e. the message transmission time is longer compared to the path set up time. The disadvantage is that the physical path is reserved for the duration of the message and may block other messages. For example, if the header is blocked, waiting for a physical link to become free, all of the links reserved by the probe until that point remain reserved and cannot be used by other circuits. Thus, if the size of the message is not much greater than the size of the header, it would be advantageous to transmit the message along with the header and to buffer it within the intermediate routers, while waiting for a free link. This alternative technique is called packet switching [10]. Then the basic signal latency for circuit switching using the following formulas [10-12]:

$$t_{circuit} = t_{setup} + t_{data} \quad (1)$$

Where $$t_{setup} = D\left[t_r + 2\left(t_s + t_w\right)\right] \quad (2)$$

$$t_{data} = t_w \left\lceil \frac{L}{W} \right\rceil = \frac{1}{B}\left\lceil \frac{L}{W} \right\rceil \quad (3)$$

Where t_{setup} is the time it takes to set up a connection in sec, t_{data} is the time it takes to transmit the data, t_r is the routing decision time, t_s is the switching delay, t_w is the propagation delay across the channel, B is the physical channel bandwidth in bits/sec, L is the message length in bits, D is the number of links between source and destination node, and W is the physical channel width in bits.

II. 2. PACKET SWITCHING

Packet switching is advantageous when messages are short and frequent. Unlike the circuit switching where a segment of a reserved path may be idle for a significant period of time, a communication link is fully utilized when there is data to be transmitted. Many packets, belonging to a message can be in the network at the same time, with no respect to that if the first message has arrived at the destination or not. However, splitting the message into packets produces some overhead. If the packets are routed adaptively, i.e. not following the same path as the first packet, the packets may arrive at the destination out of order. In this case the headers must contain also sequencing information, so that the messages can be reconstructed at the destination. To be viable, the messages must be buffered and processed within the routers. Storage requirements can be reduced by using central queues that are shared by all input channels rather than providing buffering at each input channel, output channel or both [13].

II. 2. 1. SAVE-AND-FORWARD SWITCHING

The message can be partitioned and transmitted as fixed-length packets. The first few bytes of a packet contain routing and control information and are referred to as packet header. Each packet is individually routed from the source to the destination. The packet is completely buffered at each intermediate node before it is forwarded to the next one. This is the reason why this technique is also referred to as save-and-forward (SAF) switching. The header information is extracted at the intermediate node and used to determine the output link over which is to be forwarded. The basic latency of a SAF-switched message can be computed as follows [14-16]:

$$t_{SAF} = D\left[t_r + \left(t_s + t_w\right)\left(\frac{L+W}{W}\right)\right] \quad (4)$$

II. 2.2. VIRTUAL CUT-THROUGH SWITCHING

When the packet is bigger than the channel bandwidth, the transfer of the packet will take multiple cycles. However, the first few bytes contain the routing information, which is available after the first cycles. Rather than waiting for the entire packet to be received, the packet header can be examined as soon as it is received. The router can start forwarding the header and the following data bytes as soon as routing decisions have been made and the output buffer is free. The message does not have to be buffered at the output and can cut through to the input of the next router before the complete packet has been received at the current router. In the absence of blocking, the latency, experienced by the header at each node is the routing latency and propagation delay through the router and along the physical channels. The message is effectively pipelined through successive switches. If the header is blocked on an output channel, the complete message is buffered at the node. Thus at high network loads, VCT switching behaves like packet switching. The base latency of a non-blocked message can be computed as follows [17]:

$$t_{VCT} = D\left(t_r + t_s + t_w\right) + \max\left(t_s, t_w\right)\frac{L}{W} \quad (5)$$

II. 2.3. WORMHOLE SWITCHING

Cut-through routing is assumed to occur at the flit level with the routing information contained in 1 flit. But, the unit of message flow control is a packet, sufficient buffer space must be allocated for a complete packet in case the header is blocked. The need to buffer complete packets within a router can make it difficult to construct small, compact and fast routers. In wormhole switching, message packets are also pipelined through the network. However, the buffer requirements within the routers are substantially reduced over the requirements for VCT switching. A message packet is broken up into flits. The flit is the unit of message flow control and input and output buffers are typically large enough to store a few flits. Thus, at any instant in time a blocked message occupies buffers in several routers The base latency of a wormhole-switched message can be computed as follows [18]:

$$t_{wormhole} = D\left(t_r + t_s + t_w\right) + \max\left(t_s, t_w\right)\frac{L}{L+W} \quad (6)$$

II. 2.4. MAD POSTMAN SWITCHING

VCT switching improved performance over packet switching by enabling message flow while retaining the ability to buffer complete message packets. Switching provided further reductions in latency by permitting buffer VCT so that routing can be completely handled within single-chip routers, therefore providing low latency necessary for tightly coupled parallel processing. This trend toward increased message pipelining is continued with the development of the mad postman switching mechanism in an attempt to realize the minimal possible routing latency

per node. The mad postman switching attempts to reduce the per-node latency further by pipelining at the bit level. When a header flit starts arriving at a router, it is assumed that the message will be continuing along the same dimension. Therefore header bits are forwarded to the output link in the same dimension as soon as they are received (assuming that the output channel is free). Each bit of the header is also buffered locally. Once the last bit of the first flit has been received, the router can examine this flit and determine if the message should indeed proceed further along this dimension. If it is to proceed along the second dimension, the remainder of the message starting with the second flit of the header is transmitted to the output along the second dimension. If the message has arrived at its destination, it is delivered to the local processor. In essence, the message is first delivered to an output channel and the address is checked later, hence the name of this switching technique. This strategy can work very well in 2-D networks since a message will make at most one turn from one dimension to another. The base latency of a message, using mad postman switching technique can be computed as follows [19, 20]:

$$t_{madpostman} = t_h + t_{data} \quad (7)$$

Where $t_h = D(t_s + t_w) + \max(t_s, t_w)W$ (8)

$$t_{data} = \max(t_s, t_w)L \quad (9)$$

Where t_h is the time taken to completely deliver the header, t_{data} is the time taken to deliver the data.

III. Performance Analysis

This study has presented the performance analysis and evaluation of different switching techniques over wide range of the affecting operating parameters as shown in Table 1. Signal latency, and switching time and switching speed are the major interesting design parameters in current research.

Table 1. List of the parameters used in the simulation [1, 12, 18].

Operating parameter	Symbol	Value
Routing decision time	t_r	5 msec-50 msec
Switching delay	t_s	10 µsec-100 µsec
Channel propagation delay	t_w	1 µsec-10 µsec
Channel bandwidth	B	2.5 Gbit/sec-40 Gbit/sec
Message length	L	8 bits-256 bits
Number of links	D	4 links -24 links
Physical channel width	W	4 bits-64 bits

Based on the modeling equations analysis over wide range of the operating parameters, and the series of the Figs. (1-9), the following features are assured:

i) Fig. 1 has assured that set up connection time increases with increasing both number of links between different messages and routing decision time.
ii) Figs. (2-4) have indicated that set up connection time increases with increasing switching delay time, channel propagation delay time and number of links between different data transmission messages. It is observed that the increased number of links and routing decision time, this makes set up connection time very large.
iii) Fig. 5 has assured that data transmitting time increases with increasing message length and decreasing channel bandwidth.
iv) Fig. 6 has indicated that data transmitting time increases with decreasing both channel bandwidth and channel width for transmitting data messages.

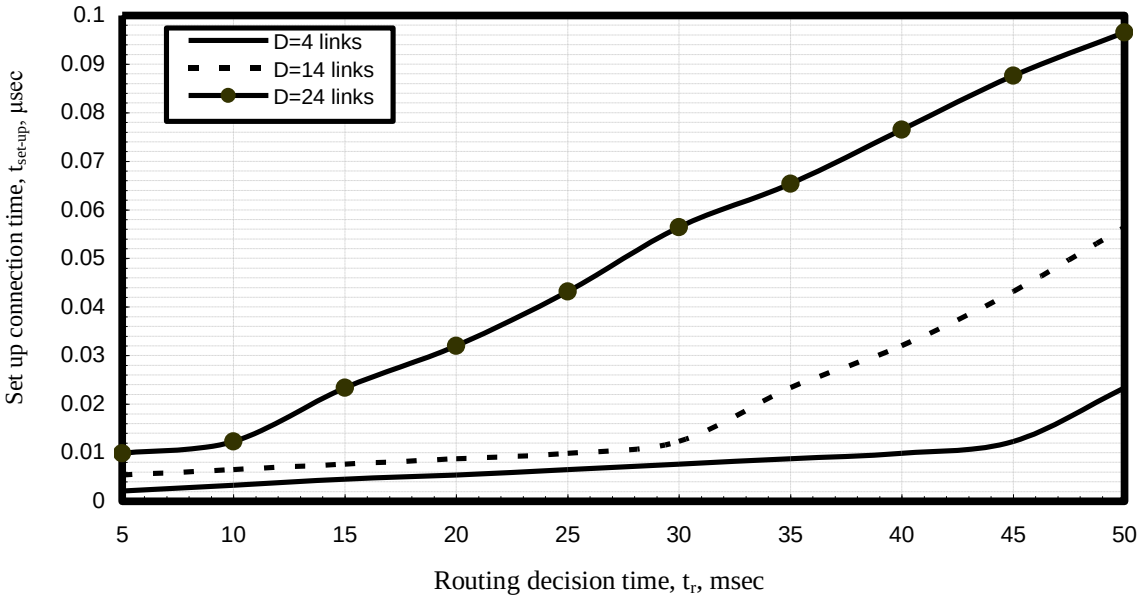

Fig. 1. Variations of set up connection time against variations of routing decision time and number of links at the assumed set of the operating parameters.

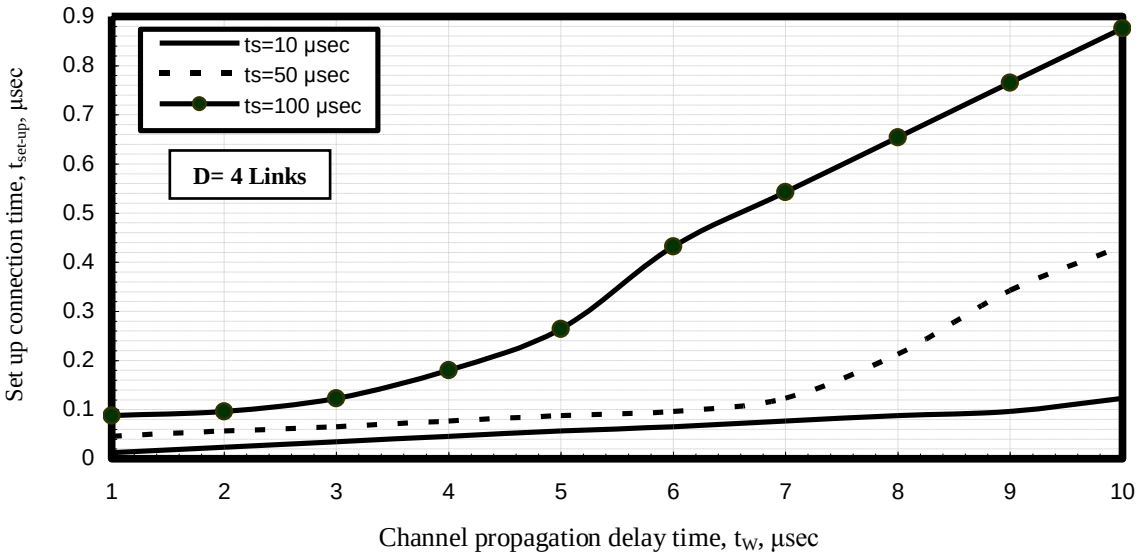

Fig. 2. Variations of set up connection time against variations of channel propagation delay time and switching delay time at the assumed set of the operating parameters.

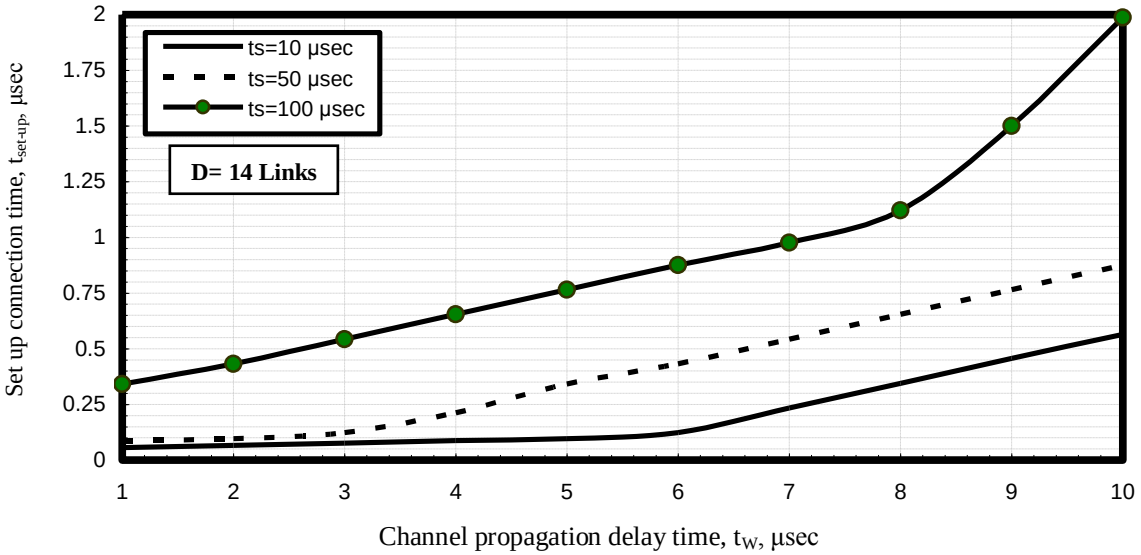

Fig. 3. Variations of set up connection time against variations of channel propagation delay time and switching delay time at the assumed set of the operating parameters.

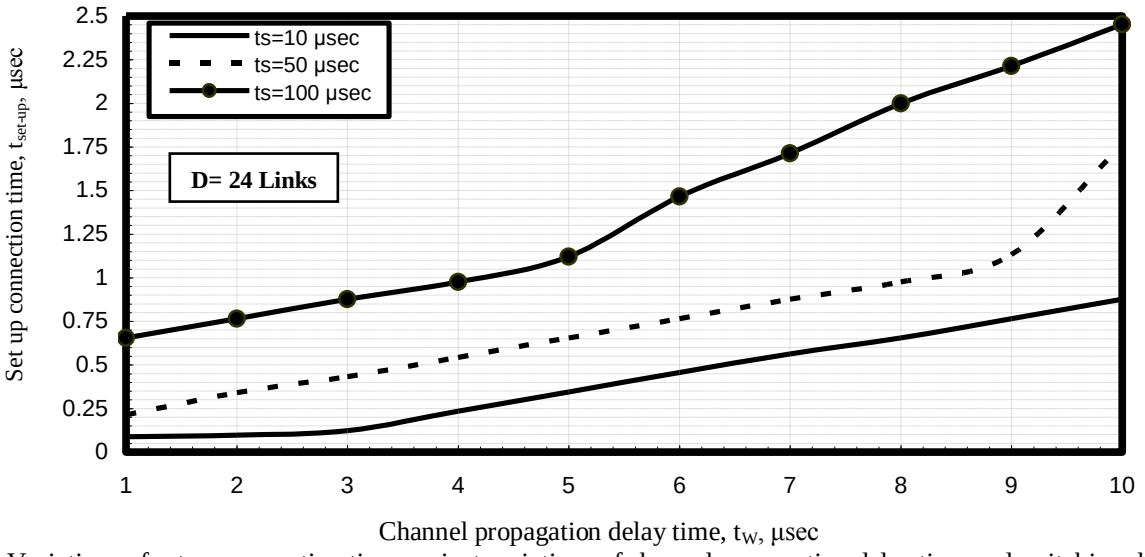

Fig. 4. Variations of set up connection time against variations of channel propagation delay time and switching delay time at the assumed set of the operating parameters.

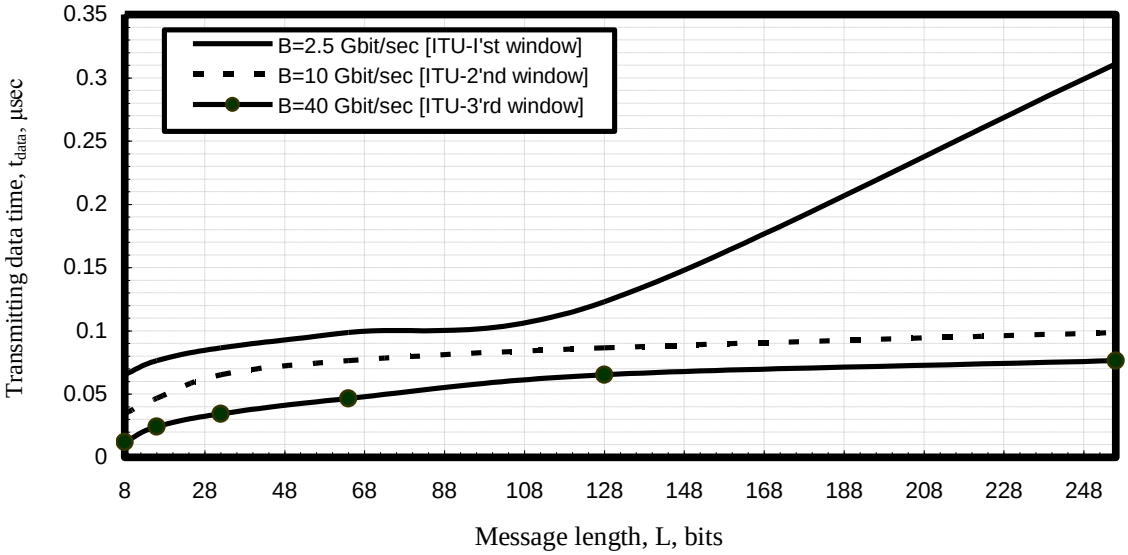

Fig. 5. Transmitting data time in relation to message length and channel bit rate at the assumed set of the operating parameters.

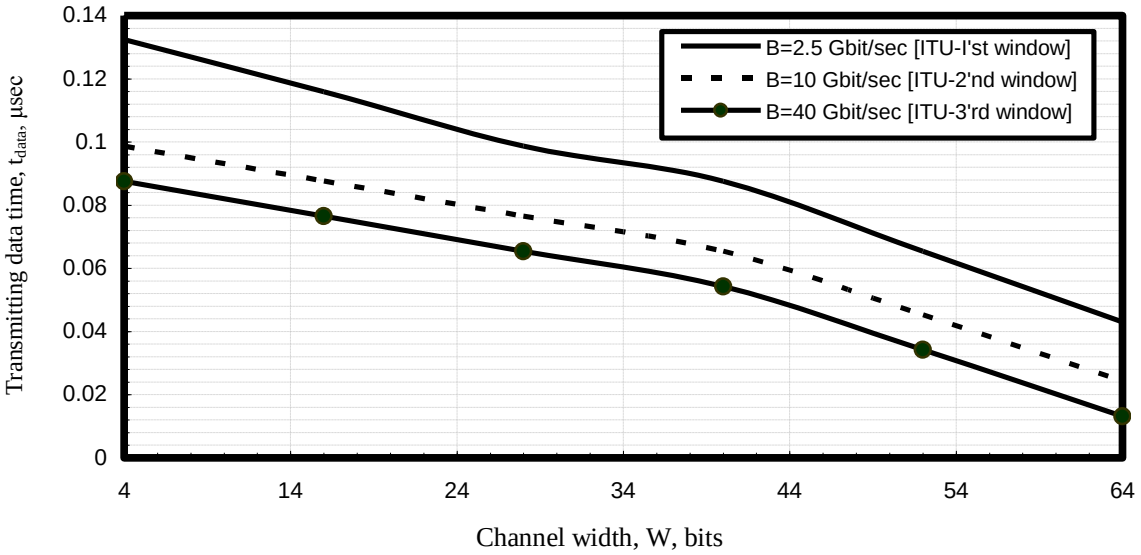

Fig. 6. Transmitting data time in relation to physical channel width and channel bit rate at the assumed set of the operating parameters.

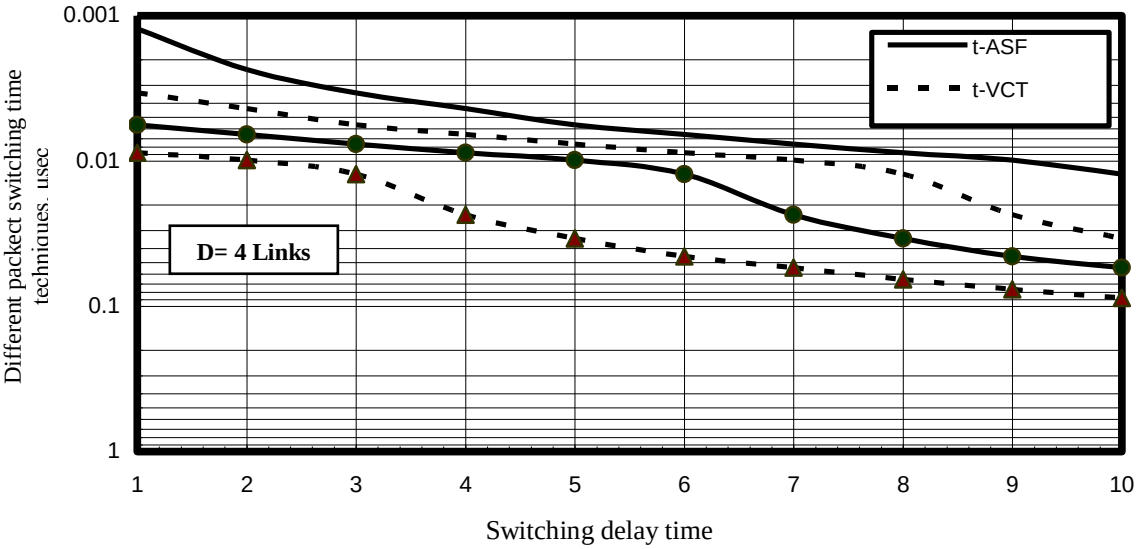

Fig. 7. Different packet switching time techniques versus switching delay time and number of links at the assumed set of the operating parameters.

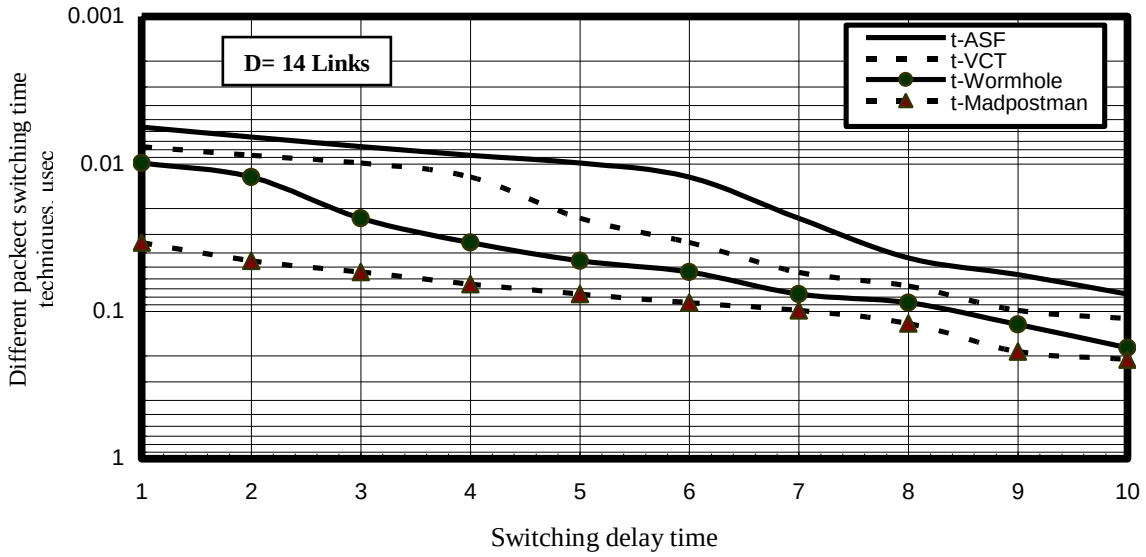

Fig. 8. Different packet switching time techniques versus switching delay time and number of links at the assumed set of the operating parameters.

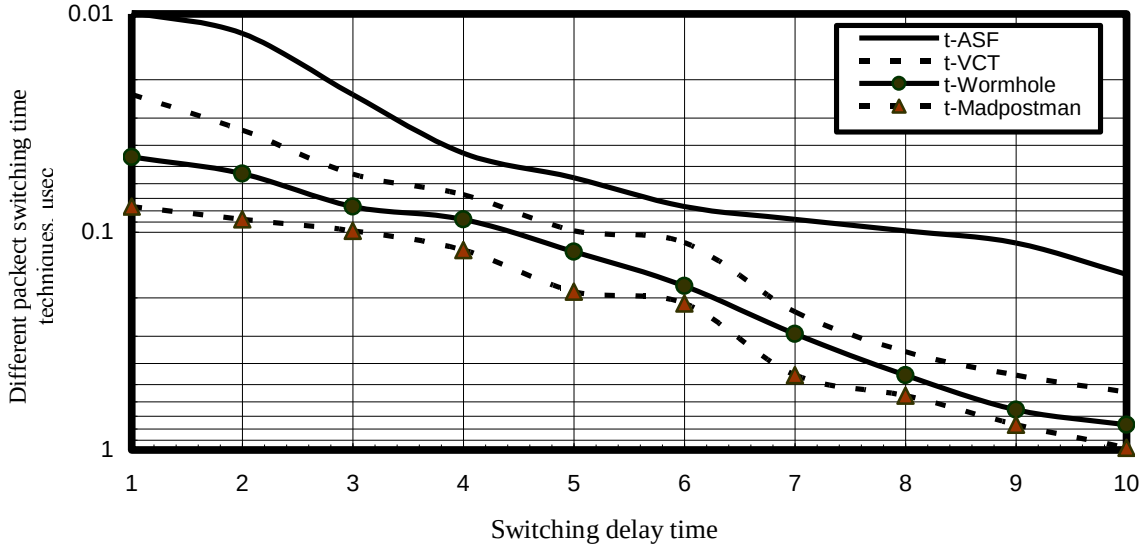

Fig. 9. Different packet switching time techniques versus switching delay time and number of links at the assumed set of the operating parameters.

v) Figs. (7-9) have proved that save and forward packet switching technique has presented the highest switching delay time, while mad postman switching packet technique has presented the lowest switching delay time at the same number of links between different messages.

IV. CONCLUSIONS

In a summary, we have deeply investigated different packet and circuit switching techniques to control different delay times. It is theoretically found that madpostman switching transmission technique has presented the lowest switching propagation delay time in comparison with other different switching transmission switching techniques under the same operating conditions.

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Author's Profile

Dr. Ahmed Nabih Zaki Rashed was born in Menouf city, Menoufia State, Egypt country in 23 July, 1976. Received the B.Sc., M.Sc., and Ph.D. scientific degrees in the Electronics and Electrical Communications Engineering Department from Faculty of Electronic Engineering, Menoufia University in 1999, 2005, and 2010 respectively. Currently, his job carrier is a scientific lecturer in Electronics and Electrical Communications Engineering Department, Faculty of Electronic Engineering, Menoufia university, Menouf. Postal Menouf city code: 32951, EGYPT. His scientific master science thesis has focused on polymer fibers in optical access communication systems. Moreover his scientific Ph. D. thesis has focused on recent applications in linear or nonlinear passive or active in optical networks. His interesting research mainly focuses on transmission capacity, a data rate product and long transmission distances of passive and active optical communication networks, wireless communication, radio over fiber communication systems, and optical network security and management. He has published many high scientific research papers in high quality and technical international journals in the field of advanced communication systems, optoelectronic devices, and passive optical access communication networks. His areas of interest and experience in optical communication systems, advanced optical communication networks, wireless optical access networks, analog communication systems, optical filters and Sensors. As well as he is editorial board member in high academic scientific International research Journals. Moreover he is a reviewer member in high impact scientific research international journals in the field of electronics, electrical communication systems, optoelectronics, information technology and advanced optical communication systems and networks. His personal electronic mail ID (E-mail:ahmed_733@yahoo.com). He has scored most download articles in optics and laser technology journal, Elsevier publisher in 2013.