ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2, Issue 7, July 2013

DESIGN AND PERFORMANCE ANALYSIS OF RING OSCILLATORS

(Derivation of frequency of an N staged inverter based ring oscillator)

ARYA TAH (*Author*)
Dept. name of organization: Electronics and communication engineering
Name of organization: NIT Durgapur
Durgapur, India

DEBASISH KUMAR RAKSHIT (*Author*)
Dept. name of organization: Electronics and communication engineering
Name of organization: NIT Durgapur
Durgapur, India

Dr. ASISH KUMAR MAL (*Author)*
Dept. name of organization: Electronics and communication engineering
Name of organization: NIT Durgapur
Durgapur, India

***Abstract*— This document emphasizes on deducing a technique to evaluate the frequency of a ring oscillator. The estimation of frequency of a ring oscillator in the absence of parameters like process transconductance, threshold voltage etc is quite a tedious job. Here we describe a technique and a formula thus has been deduced to precisely determine the frequency of a ring oscillator. The formula derived here has high precision rates, irrespective of the technology used, and the (W/L) ratio of the used transistors. In the underlying work, a comparison has also been made between the existent CMOS based Ring oscillators and DTMOS [1] based Ring oscillators based on performance. The advantage over other defined techniques is that it gives far better results, and is simple and lucid. Results have been obtained using LTspiceIV and BSIM 4.0 level 54 based MOSFET model using 50nm CMOS technology.**

Keywords*— *delay, ring oscillator, inverter, power dissipation, frequency, Elmore delay calculation.

I. INTRODUCTION

Ring Oscillators are of prime importance in the electronics industry. The importance is quite intense nowadays, given the developments in the domain of VLSI. ADCs, PLLs and VCOs have tremendous usage of ring oscillators.

Ring oscillators comprise of a ring of N-stages of inverters, where N is necessarily odd and the output oscillates between two limits, HIGH and LOW. We know that frequency of such oscillation can be increased by decreasing the number of stages or by altering device dimensions, which often end up disastrously increasing the power consumption.

Now, the big task is how to estimate the frequency of operation of the oscillator. The inverter based delay, t_d, can be found out, and hence by conventional methods we can find out the ring oscillator frequency, by the age old formula $f=1/2Nt_d$.

But, the evaluation of delay of each inverter stage remains a huge problem. This requires quite an amount of knowledge about internal device parameters. There have been methods, where the estimation formulae have been derived without much use of device parameters but, in those cases the efficiency of the formula is not appreciable. There have been a large number of works, but all of them have their own handicaps, in being applicable only to a particular device length or device (W/L) ratio. The proposed method largely oversees these deficits and is applicable not only at any (W/L) ratio, but also, even on changing device characteristics this formulation holds true.

The formula, prescribed here depends on only 3 parameters, namely the number of stages, the capacitance at each stage, and the resistance, which in turn is estimated by Barkhausen's criterion and power dissipation at a single stage.

II. DEVELOPMENT OF THE PROPOSED TECHNIQUE

A. *Study of existing formulae and making of a new estimation process*

The most basic ring oscillator is simply a chain of single ended digital inverters, with the output of the last stage fed back to the input of the first stage. Note that to provide the DC inversion, an odd number of stages must be used. To see why this circuit will oscillate, assume that the output of the first inverter is a '0'. Therefore, the output of the N-th inverter, where N is odd, must also be'0'.However, this output is also the input to the first inverter, so the first inverter's output must switch to a'1'.By the same logic, the output of the last inverter will eventually switch to a '1', switching the output of the first inverter back to '0'. This process will repeat indefinitely, resulting in the voltage at each node oscillating.

Let's assume that the delay each inverter gives is t_d. So, the net delay associated with N stages will be $N*t_d*2$. This is because t_d is nothing but the difference in time of the toggle points of the input and corresponding output.

We know the net phase shift should be of the order of 2π. But the net phase shift per oscillator must be of the order of π/N; as the remaining shift is obtained by the DC inversion. Now, this is one of the basic requirements that would come into play while we calculate the delay.

Now, our work involves studying of frequency response in case of an N-stage oscillator. We have seen already that frequency depends on t_d. We can say that every stage in the ring oscillator has a resistance and capacitance associated with it, which ultimately causes the delay. Now, to start with we use inverter stages using 50nm CMOS technology, with W_{pmos}=1000nm, and W_{nmos}=500nm

STUDYING THE EFFECTS OF ADDING IDENTICAL CAPACITIVE LOAD AT THE TERMINUS OF EACH STAGE

S.No.	DELAY TABLE		
	External load	*n*	*delay*
1.	0pf	5	0.22ns
2.	0.01pf	5	0.44ns
3.	0.02pf	5	0.67ns
4.	0pf	7	0.32ns
5.	0.01pf	7	0.64ns
6.	0.02pf	7	0.97ns
7.	0pf	9	0.42ns
8.	0.01pf	9	0.84ns

TABLE: 1

In the table above we have seen the effect of adding load capacitances at the terminal of each stage of the ring oscillator. Now, adding capacitance would increase delay, as we have seen t_d is proportional to Capacitance [3]. We have to analyze the dynamic operation of the inverter in this context.

Let us now analyze the results in the table. We know that, every ring oscillator has its characteristic capacitance. If we equal the load capacitance to the intrinsic capacitance that each stage of the oscillator provides, we find that the frequency halves. Thus, we may conclude, that when frequency halves, our estimated capacitance becomes equal to the intrinsic capacitance.

B. *Studying the effect of capacitance on frequency*

From [5] we get to know about Miller's effect and about replacing bridging capacitances with a single capacitance. In this way we bring about replacement in the transistors used in this context, and thus we get an equivalent load C_l across the inverter stage. Thus when we add another $C=C_l$ at the terminal of each stage, the equivalent load becomes $2C_l$.

Now, there are quite a number of ways to find C_l. Using the SPICE model files and hence device parameters for capacitance estimation is often tedious and time consuming. Also, the evaluation becomes a lot more difficult for advanced CMOS technology models.

So, a better way is experimental determination, by way of plots. The table below gives us the delay in relation to $(W/L)_p$,$(W/L)_n$ and $(W/L)_p+(W/L)_n$ ratio.

STUDY OF CAPACITANCE WITH RESPECT TO W/L RATIOS

S.No.	CAPACITANCE TABLE		
	$(W/L)_p$	$(W/L)_n$	*C*
1.	(1000/50)=20	(500/50)=10	0.010pf
2.	(1000/50)=20	(1000/50)=20	0.012pf
3.	(1250/50)=25	(500/50)=10	0.011pf
4.	(1000/50)=20	(3000/50)=60	0.023pf
5.	(4000/50)=80	(3000/50)=60	0.039pf

TABLE: 2

Capacitance can also be calculated analytically, by way of formulae given in [6]. Model manuals give us detailed description about how to calculate capacitance, and capacitance at the terminal of each stage can be calculated by Miller's effect.

However, as expected, the experimental results would vastly be equal to the results obtained by model files.

STUDY OF CAPACITANCE WITH $(W/L)_p+(W/L)_n$

S.No.	CAPACITANCE TABLE		
	$(W/L)_p,(W/L)_n$	$(W/L)_p+(W/L)_n$	C
1.	20,10	30	0.010pf
2.	25,10	35	0.011pf
3.	20,20	40	0.012pf
4.	20,60	80	0.023pf
5.	80,60	140	0.039pf

TABLE: 3

An observation can be accredited from the above table; capacitance is doubling with doubling (w/l) ratios. So, we can make a conclusion, by further close observation, that

C_1/C_2 is approximately equal to (sum of (W/L) ratios of p and n transistors)$_1$/ (sum of (W/L) ratios of p and n transistors)$_2$. This is a rough way of estimating the capacitance at each stage of the ring oscillator.

The delay is therefore proportional to N (number of stages) and C (capacitance).

Also, there must be a resistance term to equate the left and right sides. Hence, there must be a R. Our next objective is to determine the Resistance, R.

The gate drain overlap capacitance of Q_1, C_{gd1} is replaced by an equivalent capacitance between output node and ground of $2C_{gd1}$. Each of the drain body capacitances has a terminal at a constant voltage. Thus, these are replaced by equal capacitances between output node and ground. Since the second inverter does not switch states we will assume that the input capacitances of the upcoming stage remain constant and equal to gate capacitance.

$C=2C_{gd1}+2C_{gd2}+C_{db1}+C_{db2}+C_{g3}+C_{g4}+C_w$.

[7].

C. Study of resistance parameter and estimating resistance

Now, the important thing is estimating the resistance parameter. We have found out a new experimental way, of finding out resistance using power dissipation at a single stage. A point to be noted here is the power dissipation of a single stage is same as long as the device parameters remain the same. However, it does not depend on the length of the ring oscillator in any sense.

If the ring oscillator stages are replaced by their linear equivalents, then the whole loop can be reconstructed as shown in Fig.2.

The important thing that is done here is frequency domain analysis of the loop. The loop gain X(s) =A (s_1).A (s_2)…A (s_n).More often than not, A (s_1) = A (s_2) =…= A (s_n). [8,9]

First, let's start analyzing the Barkhausen's criterion. The Barkhausen's criterion states that the net phase of the loop gain should be zero. Given that should happen, the net phase shift needs to be $2k\pi$. However, π phase shift is obtained from DC inversion. Hence the phase shift of the rest of the loop has to be π. Hence, we find phase shift per stage of the oscillator is π/N.The general practice however remains, lessening the required phase shift, hence to minimize the number of required stages.

We can obviously state at this juncture that the total phase shift of RC delay $=\pm\pi$.

Thus if phase shift per stage is β then:

$\beta = \pm\pi/N$……..1.

The model proposed here, hence would have ,

$\tan^{-1}(RC\omega)=\beta$……..2. [8]

Hence, our oscillation frequency becomes:

$\omega = (\tan\beta)/RC$……..3.

We know that, for an inverter in operation, in each cycle, the energy dissipation in the Q_n and Q_p is $0.5CV_{DD}^2$ respectively. Hence the net energy dissipation is equal to CV_{DD}^2. Now, we would like to frame a possible evaluation of power.

$P= CV_{DD}^2/T$……4.

$P=f\ CV_{DD}^2$……..5.

$f=P/\ CV_{DD}^2$.....6.

$\omega= P.2\pi/\ CV_{DD}^2$……7.

Hence, now for finding a possible estimate of resistance we equate equation 3 and 7.

$(\tan\beta)/RC= P.2\pi/\ CV_{DD}^2$…8

$R= V_{DD}^2.(\tan\beta)/2\ \pi P$……..9.

For our case, V_{DD} has always been 1V, so our result would well be

$R= (\tan\beta)/2\ \pi P$……..10.

This is how we have developed an effective and efficient way of Resistance estimation.

However in reference [9] they have taken

$\beta = 2k\pi/N$, which is certainly not the case as the remaining phase shift is provided vy DC inversion

The advantages of using this method are many. Firstly we do not have to engage ourselves into tedious calculations. Nextly, by knowing power dissipation of a single stage, of a particular design of inverter, the resistance can be calculated for any length of ring oscillator, i.e. having any number of permissible stages.

With this, we approach the crucial juncture, where estimation of capacitances and resistances have been done.

So, we see, the 3 parameters on which the frequency depends, namely N,R,C have been sorted out to the best possible extent. The next task is to frame a relation between the parameters.

D. Framing a relation between number of stages ,frequency, resistance, capacitance

Frequency of operation is the parameter of interest for us. But, we know, f=1/T. We can say, T is proportional to N, R, and C as we can see. What we

are actually interested in is nothing but the propagation delay, that would ultimate give us the frequency. [4]

Quick delay estimation is the core basis of designing faster and critical paths. We may use the simulator based approach for our delay and hence frequency estimation purpose. But that does not help our understanding of paths in any case, hence faster; more efficient pathways cannot be developed. Novice designers, spend hours tweaking parameters to find out efficient model designs.

In this section we take up a lumped circuit RC model of transistors. Although transistors have complex, nonlinear current voltage characteristics, they can be well approximated as a switch in series with a resistor, where the *effective resistance* would depend on the average current delivered by the transistor. Transistor gate and diffusion nodes have capacitance.

So, we in this arena, devise a method, where the net delay measurement would be on the basis of driving resistance and load capacitance. Usually in the technology, we use devices of minimal length, and optimum power consumption.

We take up the Elmore delay model [10] for our purpose of synthesizing the delay of the ring oscillator.

Viewing ON transistors as resistors, a possible way of viewing the circuit is as shown in Figure 7. Elmore Delay states that the net delay over the whole Network is equivalent to the summation of the product of individual load capacitance at each node and the subsequent resistance between Node and Source.

$$T = \sum_{k=0}^{n} R_k C_k$$

Now, let's take up the case of investigating how to implement the technique of Elmore delay to Ring oscillator.

Ring oscillator does not contain any source as such, from where we would calculate the resistance per node. So, we take up an analogous method. We know, capacitors can act as voltage sources, when they are charged. Thus, for our sake, we take the ring oscillator to be composed of (N-1) +1 delay stages. So, for our analysis, there are N-1 stages of resistors and capacitors. The remaining stage is termed the 'Engine stage'. We, take up that it is this capacitor-resistor stage that acts as voltage source.

As ring oscillators have connected ends, we can take this 'Engine stage' anywhere in the ring.

A better representation would involve, cutting the ring at the K^{th} node. ($K \leq N$). So the $(K+1)^{th}$ node ((K+1) th stage of capacitance and resistance) is termed the engine node (engine stage). The remaining length of the ring is analyzed by Elmore delay analysis:

There would be (N-1) stages of identical capacitance and resistance

In case of added capacitive load, we take the capacitance as (C_p+C_l), where C_p is the intrinsic capacitance of the transistor and C_l is the added capacitive load at each level.

So our formula becomes:

$$T_{pd} = \sum_{k=0}^{n-1} R_k C_k \text{.....12.}$$

For no added capacitive load, for a N stage ring oscillator, this formula becomes:

$$T_{pd} = N(N-1)RC/2\text{.....13}$$

(It is because, T_{pd} becomes RC + 2RC+...+ (N-1)RC, and the driving or engine stage is excluded as it acts as the source).

So, a method has been devised to obtain both driving resistance and delay associated with a ring oscillator. Resistance has been calculated by the method given above. While delay estimation, is nothing but the summation of the product of estimated resistance and capacitance over (N-1) nodes. Now, it's time to check whether our proposal holds experimentally by simulation, and thus bring about a detailed study about accuracy of the proposed method

III. EXPERIMENTATIONS AND CHECKING OF THE PROPOSED METHOD

Now, we will check whether our proposed method holds by using simulation tool LTspiceIV and BSIM 4.0 model using 50nm CMOS technology.

First we have studied ring oscillators using 50nm CMOS technology with width of NMOS being 500nm and width of PMOS being 1000nm.

All the stages have a capacitance of 0.01pf as has been shown in a table above.

READINGS FOR A RING OSCILLATOR USING BSIM 4.0 MODEL WITH 50nm CMOS TECHNOLOGY.

S.No.	DELAY TABLE				
	n	***power***	***RC(in 10^{-11}s)***	***$T_d$spice***	***$T_d$calcu.***
1.	3	53.12 uW	5.161	0.13 ns	0.13 ns
2.	5	53.12 uW	2.167	0.21 ns	0.21 ns
3.	7	53.12 uW	1.661	0.30 ns	0.297 ns
4.	9	53.12 uW	1.090	0.41 ns	0.42 ns
5.	11	53.12 uW	0.876	0.46 ns	0.47 ns
6.	13	53.12 uW	0.73	0.56 ns	0.567 ns
7.	15	53.12 uW	0.63	0.69 ns	0.67 ns

TABLE: 4

So, we find that our formulation does predict results with great accuracy as far as working with a

W_p=1um, W_n=500nm, $L_{p,n}$=50nm based CMOS based ring oscillator.

Now, we find out, whether our proposed method holds true for any generalized case, i.e. for any $(W/L)_{p,n}$ ratio. The table below shows the results of simulation using transistors of different (W/L) ratio.

FREQUENCY RESPONSE WHEN THE (W/L) RATIOS ARE DIFFERENT

S.No.	DELAY TABLE					
	n	*power*	W_p	W_n	T_d*spice*	T_d*calcu.*
1.	5	67.12 uW	1u	1u	0.21ns	0.19ns
2.	5	60.14 uW	1.25 u	0.5u	0.24ns	0.22ns
3.	5	95.40 uW	1u	3u	0.31ns	0.28ns
4.	5	240.6 uW	4u	3u	0.22ns	0.19ns
5.	5	53.11 uW	1u	0.5u	0.21ns	0.21ns

TABLE: 5

Now, we see our formula operates with quite a high rate of precision for any value of (W/L) and N, for CMOS inverter stages.

Now, if we can show, that this formula can operate beyond CMOS technology, the formula would encompass a huge working domain. For our purpose we would use DTMOS [1].

IV. COMPARISION OF RESULTS FOR DTMOS AND CMOS BASED RING OSCILLATORS

So, we now begin our analysis of the formula, based on DTMOS technology. Using LTspiceIV simulator we have been able to get the following results. Model used is the same level 54 based BSIM 4.0 model. $L_n = L_p$ =50nm.

READINGS BASED ON DTMOS TECHNOLOGY BASED RING OSCILLATORS.

S.No.	DELAY TABLE					
	n	*C(pF)*	W_p	W_n	T_d*spice*	T_d*calcu.*
1.	5	0.065	4u	3u	0.18ns	0.18ns
2.	5	0.035	4u	0.5u	0.30ns	0.29ns
3.	7	0.013	1u	0.5u	0.26ns	0.25ns

TABLE: 6

So, we see our formula fits quite well for DTMOS based technology as well. So, there can't be much questionability regarding the domain of the proposed method.

Now, let's incorporate the fact that power dissipation in the first case of the above given table is a staggering 396.107uWatt per stage. In the next case its a 133.83uWatt, while for the last case its 80.5338uWatt.

What we can hence see, is that our formula works well for CMOS as well as DTMOS technologies. So, that generalizes the fact that this formula is well acceptable irrespective of the technology, irrespective of the device parameters. The above quoted technology further promises the fact of generalization because the ring oscillators can drive a higher frequency than CMOS based ones, although the power dissipation is a bit more than CMOS based ring oscillators.

V. CONCLUSION

Thus, the above study proves that the proposed method works well as far as single ended N stage ring oscillators are concerned irrespective of technology. Also, we get to bypass a number of parameters like Threshold voltage etc, and hence it comprehensively simplifies our work. This work is comparatively much better positioned than the previous works. It has all the abilities to find out frequency of operation irrespective of the technology being used.

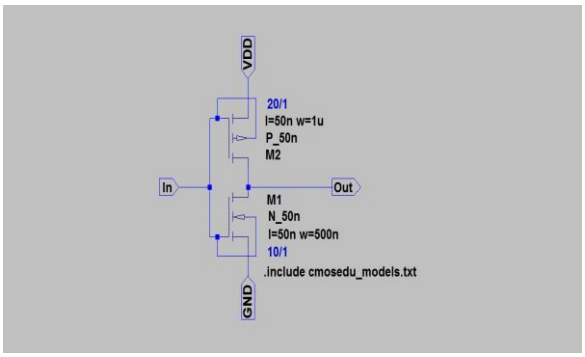

Figure1: DTMOS inverter

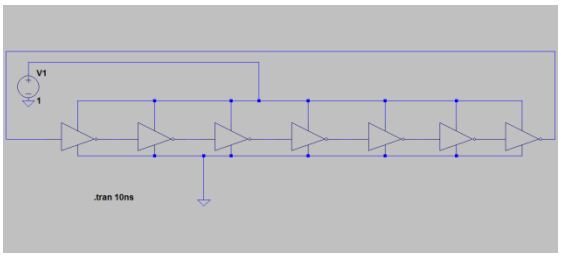

Figure2: Ring oscillator using above inverter

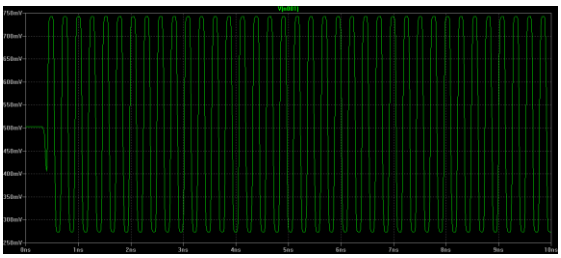

Figure3: Simulation results of above inverter

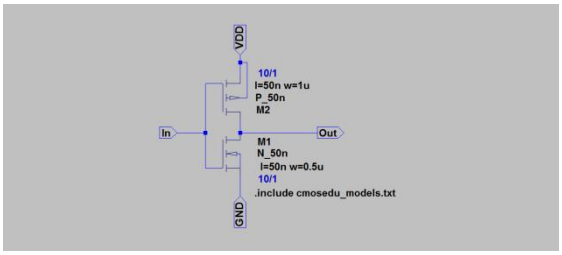

Figure4: CMOS inverter

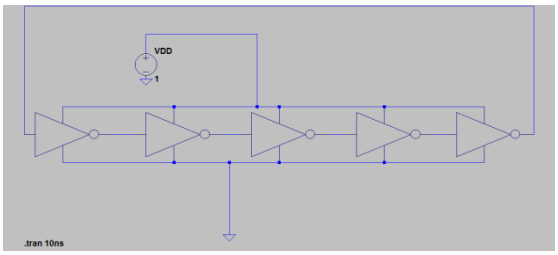

Figure5: Ring oscillator using the above CMOS Inverter

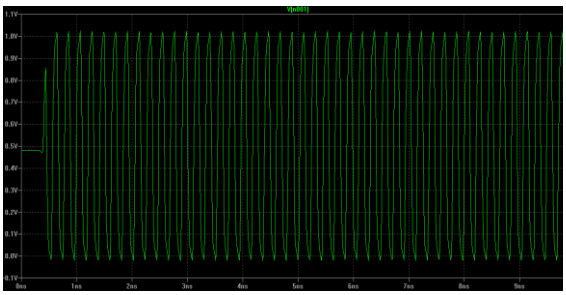

Figure6: Simulation results of the above ring oscillator

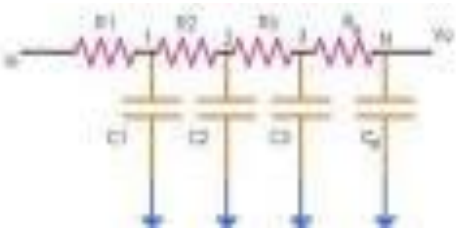

Figure7: RC ladder

ACKNOWLEDGMENT

I, Arya Tah want to thank my partner Debasish Kumar Rakshit who co-authored this work, and provided me with ample support. I want to thank our faculty mentor, Dr. Asish Kumar Mal of NIT Durgapur for all the support, suggestions and advice he has given us. Also, I want to thank my parents who have been by our side all throughout the span of this work.

REFERENCES

1. Nick Lindert, Toshihiro Sugii, Stephen Tang, and Chenming Hu, "Dynamic threshold pass transistor logic for improved delay at low power supply voltages," IEEE journal of solid state circuits, Vol.34, No.1, Jan 1999.
2. P.M.Faharabadi, H.Miar-Naimi and A.Ebrahimzadeh, "A New Solution to analysis of CMOS ring oscillators," Iranian Journal of Electrical & Electronic Engineering, Vol. 5, No. 1, March 2009.
3. Adel S. Sedra and Kenneth C. Smith, " Microelectronic Circuits," Pages 432 to 434, Fifth Edition.
4. Herbert Taub and Donald Schilling, "Digital Integrated Electronics",Pages 274 to 275.
5. Adel S. Sedra and Kenneth C. Smith, " Microelectronic Circuits," Pages 603 to 606, Fifth Edition.
6. Mohan V. Dunga, Xuemei (Jane)Xi, Jin He , Weidong Liu,Kanyu M. Cao, Xiaodong Jin, Jeff J. Ou, Mansun Chan, Ali M. Niknejad, Chenming Hu, "BSIM 4.6.0 MOSFET model," Department of electrical engineering and computer sciences, University of California, Berkeley.
7. Adel S. Sedra and Kenneth C. Smith, " Microelectronic Circuits," Pages 904 to 905, Fifth Edition.
8. Yalcin Alper Eken, " High frequency Voltage controlled oscillator in standard CMOS," School of Electrical and Computer Engineering, Georgia Institute of Technology
9. G. Jovanovic, M. Stojcev, Z. Stamenkovic, "A CMOS Voltage controlled oscillator with improved frequency stability", Scientific publications of the state university of Novi-Pazar, Ser.A, Applied Math. Inform. and Mech. Vol 2,1(2010), 1-9
10. Unknown, "Circuit Characterization and Performance Estimation." Weste04r4.fm,page-67, Monday, January 5,2004.Link::http://www.aw-bc.com/info/weste/assets/downloads/ch4.pdf