ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2, Issue 7, July 2013

Performance Investigation of Two-Stage Operational Amplifier

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Abstract: As CMOS technology scaling down transistor channel lengths to satisfy the thrust of low power consumption in modern electronics system . There is need to investigate the performance of the upcoming scaled channel length CMOS devices. At lower technology nodes mixed signal issues increases significantly this limits the performance of devices. In this paper two stage op-amp at different technology nodes of CMOS is designed and its performance has been investigated .CMOS technology nodes 16nm , 22nm ,32nm are used for evaluating the performance of two stage op-amp. Effect of temperature variations has been observed on two stage op-amp at 32nm CMOS technology.

***Index Terms*: Two stage op-amp , differential amplifier, common mode gain , slew rate**

I INTRODUCTION

As technology is scaling down the transistor lengths to reduce power consumption , the variability issues increases. Also static power dissipation and subthreshold leakage current becomes dominant at lower technology[1] .Sacaling of CMOS in deca nanometer results in degradation of gmb/gm ratio to from 0.38 to 0.12 between representative 0.25 lm and 65 nm technologies[5]. A common-mode adapter with a folded cascaded op-amp is used to reduce the common-mode voltage , circuitry and save power[6].In this paper the performance of CMOS devices at different technology for analog and mixed signal processing has been investigated .Op-amp ideally have infinite differential gain, infinite bandwidth ,infinite CMRR ,infinite slew rate in practical op-amp approaches to these values [3].Two stage op-amp is designed for different technology nodes of CMOS. Electrical characteristics of two stage op-amp at different technology nodes of CMOS are compared to study the technology scaling effects on the conventional CMOS .The effect of temperature variation on two stage op-amp at 32nm CMOS technology has been observed as temperature is also considered to be important factor for affecting the performance of circuit .

II TWO STAGE OP-AMP

Operational Amplifier is an elementary building block of the many electronics system. They are integral part of many analog and mixed signal systems.

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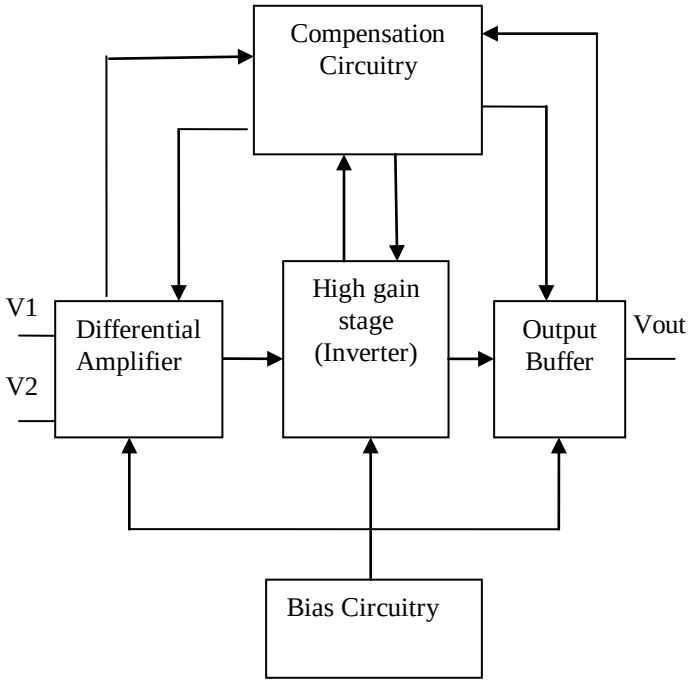

Figure.1 Block diagram of Op-amp

The block diagram of an op-amp is as shown in figure1 it consists of mainly four stages. The differential amplifier act as an input stage of the op-amp and sometimes provides the differential to single ended conversion normally, a most of the portion of the overall gain is provided by the differential input stage and the second stage is typically an inverter [3]. If the differential input stage does not perform the differential to single ended conversion, then it is accomplished in the second stage inverter. If the op-amp must drive a low resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing .Bias circuits are provided to establish the proper operating point for each transistor in its quiescent state[3]. Ideal op-amp has infinite differential voltage gain, infinite input resistance and zero output resistance. In reality op-amp only approaches these values. .The output voltage Vout can be expressed as

$$Vout = A_V (V1 - V2) \quad (1)$$

Where A_V is used to designate the open-loop differential-voltage gain.V1 and V2 Are the input voltages applied to the non-inverting and inverting terminals, respectively [3].

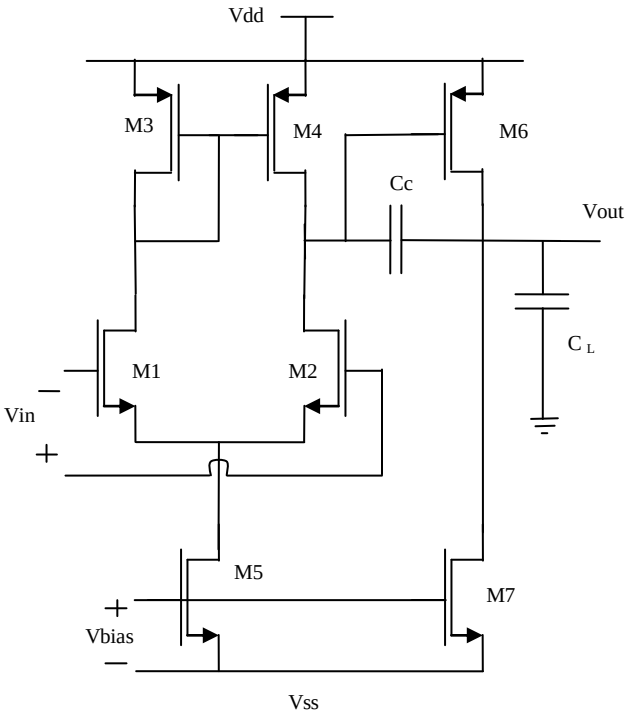

Figure 2.The circuit diagram of two stage Op-amp

The circuit diagram consist of M1 and M2 are acting as a differential amplifier for converting the input differential voltage to differential current. Figure.2 shows the single ended. Confugaration of two stage Op-amp here M1 is connected at ground and input signal applied to M2 .Differential current is then converted to voltage by load formed using MOSFETs M3 and M4. In the second stage voltage is converted to current by using MOSFET M6.The common current sink inverter by using MOSFET M7 [3]. Formulae's for designing op-amp .Assuming that $g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$ and $gds_2 + gds_4 = GI$, $gds_6 + gds_7 = GII$

1) Slew rate $SR = I_5 / C_c$ (2)

2) First stage gain $A_{v1} = -gm_1/(gds_2+gds_4)$ (3)

3) Second stage gain $A_{v2} = -gm_6/(gds_6+gds_7)$ (4)

4) Gain bandwidth $GB = gm_1/C_c$ (5)

MOSFETS	(W/L)
M1	2
M2	2
M3	10
M4	10
M5	3
M6	60
M7	10

Table1.Aspect Ratios

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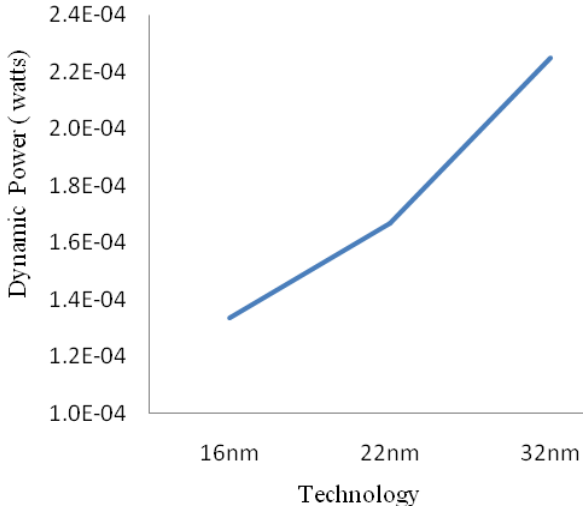

Figure 3. Variation in Dynamic power for different CMOS technologies

III SIMULATION AND RESULTS

Synopsys Hspice 2005.09 simulator is used for circuit simulation. Performance of the two stage op-amps electrical characteristics differential gain, bandwidth , slew rate, common mode rejection ratio , dynamic power dissipation for different technology nodes of CMOS are shown in graphs from figure 3 to figure 7 .The supply voltage and other circuit parameters except technology are kept constant for comparison .The temperature variation effects at 32 nm CMOS technology are shown in figure 8 to figure 15 are

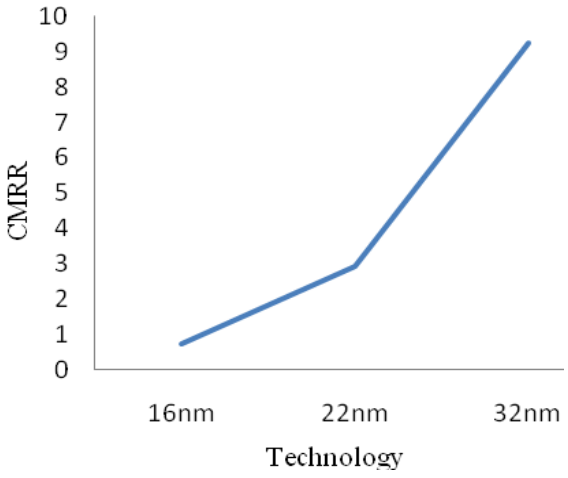

Figure 4. Variation in Common mode rejection ratio (CMRR) for the different CMOS technologies

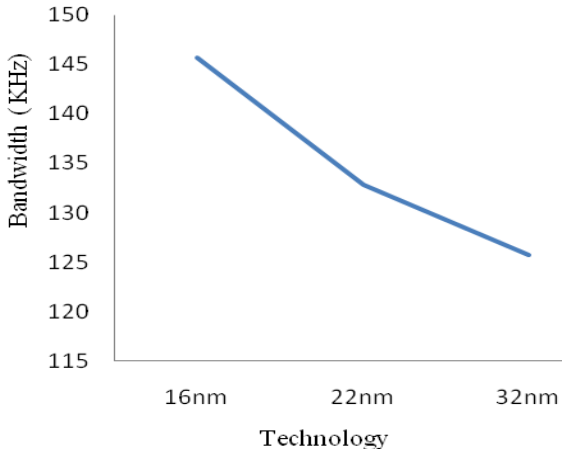

Figure 5 . Variation in Bandwidth for the different CMOS technologies

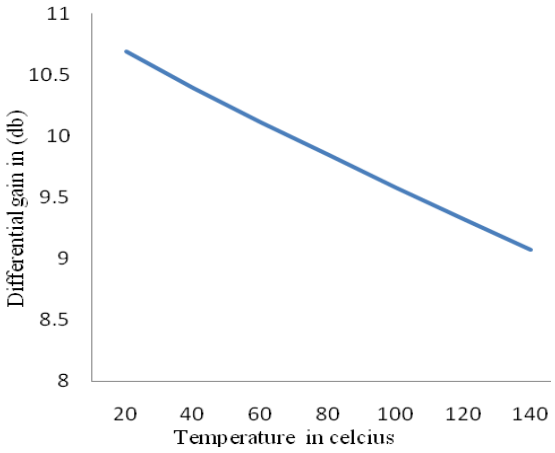

Figure 8.Effect of temperature variation on differential gain at 32nm technology

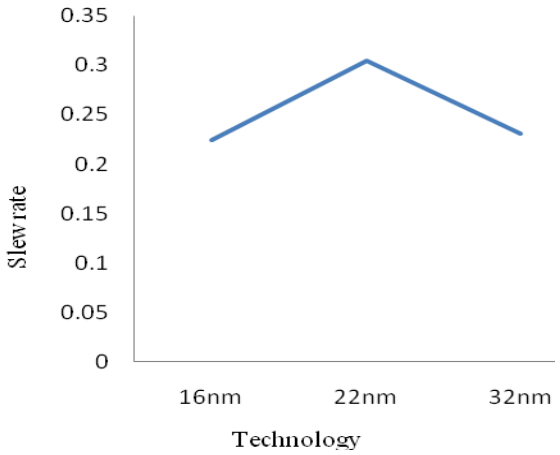

Figure6.Variation in slew rate for the different CMOS technologies

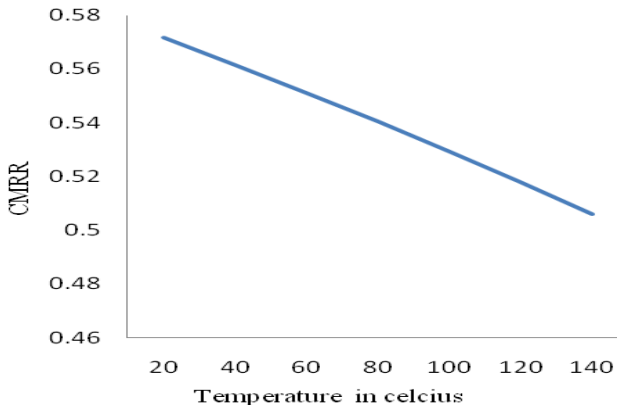

Figure 9.Effect of temperature variation on common mode rejection ratio(CMRR)

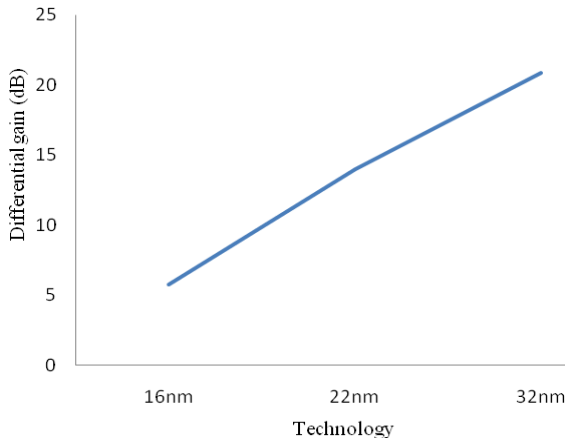

Figure7.Variation in differential gain for the different CMOS technologies

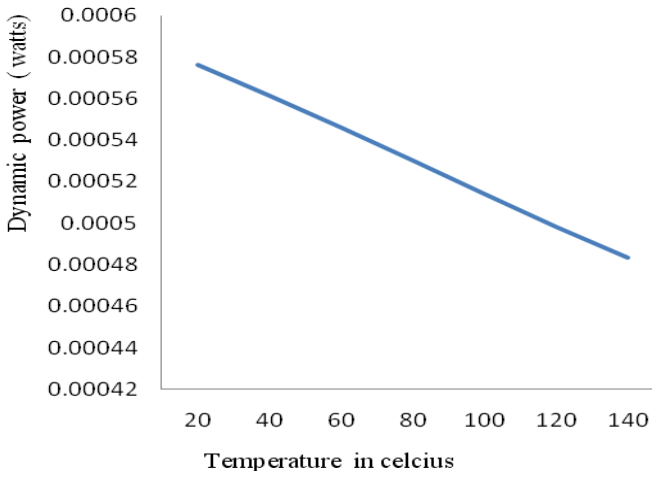

Figure10. Figure 7.Effect of temperature variation on dynamic power

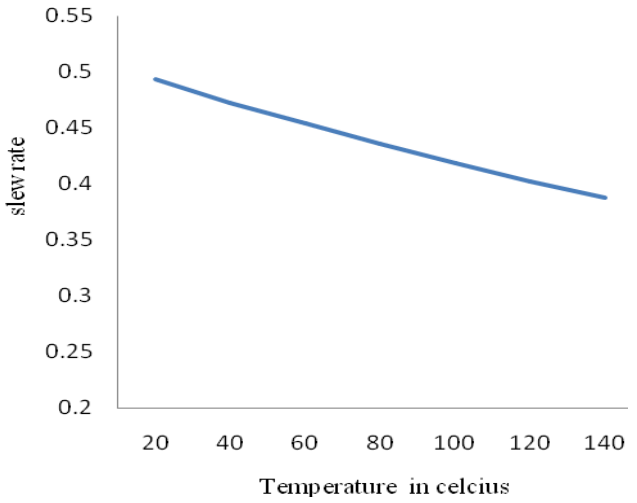

Figure 11.Effect of temperature variation on slew rate

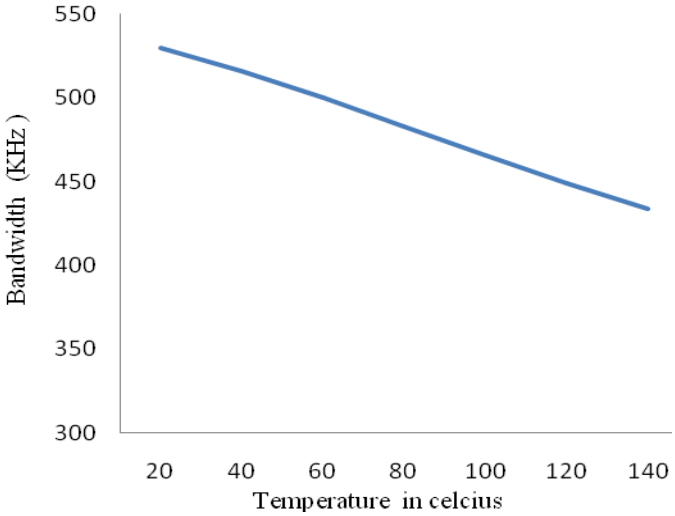

Figure 12..Effect of temperature variation on Bandwidth

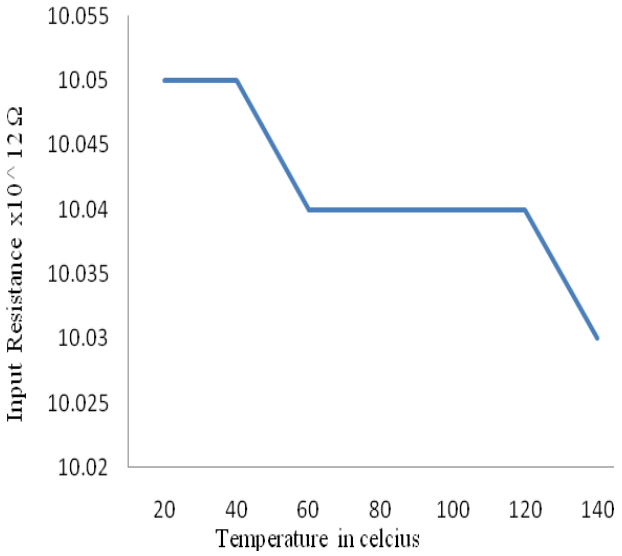

Figure 12..Effect of temperature variation on input resistance

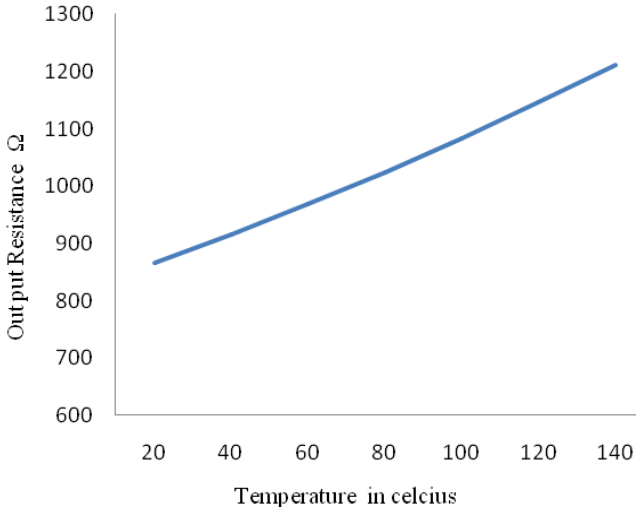

Figure 13..Effect of temperature variation on output resistance

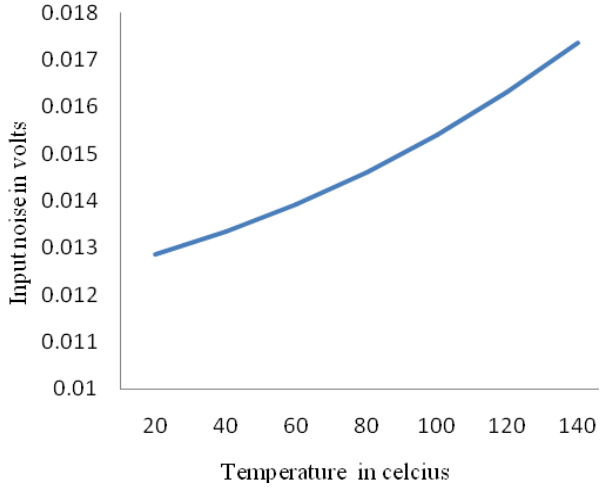

Figure 14.Effect of temperature variation on input noise

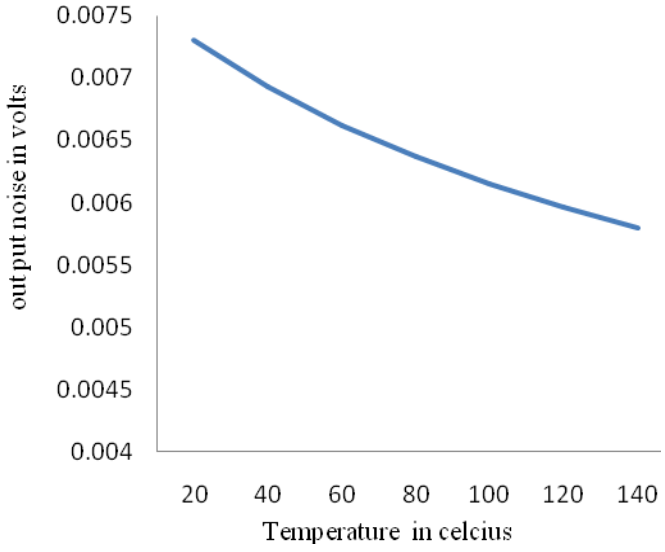

Figure 15.Effect of temperature variation on output noise

IV CONCLUSION

Performance of the two stage amplifier's electrical characteristics at different technology node has been analyzed. It shows that as technology is scaled down the transistor channel lengths dynamic power ,differential gain ,CMRR, slew rate reduces and bandwidth increases. From the result it can be observed that performance decreases as technology scales down but power dynamic dissipation is also reduces. Temperature variation for 32nmtechnology CMOS two stage amplifier has been analyzed. It shows that with temperature rise dynamic power ,differential gain ,CMRR, slew rate, bandwidth ,input resistance and output noise reduces and input noise and output resistance increases.

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