

Design of low power SAR ADC in Biomedical Applications

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Abstract— Power consumption is one of the main design constraints in today ICs. For systems that are powered by small non rechargeable batteries over the entire life time, such as medical implant devices ultra low power consumption is important. In these systems ADCs are key components to interface between analog world and digital domain. This project is going to address the design challenges and strategies of low power ADCs for biomedical implant devices.

Index Terms— DAC, Low Power, SAR ADC, Biomedical applications

I. INTRODUCTION

Analog to Digital Converters are important building blocks in lots of applications. In past few years, more and more applications are built with very stringent requirements on power consumption. For electronic systems, such as wireless systems or implantable devices, the power consumption is becoming one of the most critical factors. The stringent requirements on the energy consumption increase the need for the development of low voltage and low power circuit techniques and system building blocks.

Analog-to-Digital Converters (ADCs) translate the analog quantities into digital language, used in information processing, computing, data transmission and control systems. ADCs are key components for the design of power limited systems, in order to keep the power consumption as low as possible. Implantable Medical electronics, such as Pacemakers and cardiac defibrillators are typical examples of devices where ultra-low-power consumption is paramount. The implanted units rely on a small non rechargeable battery to sustain a lifespan of upto 10 years.

The life time of the artificial pacemakers should last up to 10 years which mandate low power consumption per operation. The analog to digital converter is the crucial part of an implantable pacemaker since it consumes a large amount of power as the interface between sensed analog signal and digital signal processor block.

Low power ADCs with moderate resolution and low sampling frequency is suited for biomedical application. These specifications make SAR ADC the suitable choice. It consumes low power due to its simple structure. Moreover, SAR ADC is scalable with the technology scaling since most parts of the architecture apart from the comparator are digital.

The rest of the paper is organized as follows; one biomedical device Pace Maker operation is explained in Section II. The SAR ADC architecture operation is explained in Section III....

II. PACEMAKER OPERATION

Pacemakers directly control the pattern and speed of the heartbeat. When the heart stops beating or it beats too slowly, pacemaker provides weak electrical signals with approximately 70 beats per minute to correct the timing of the heart beat. This medical device contains a battery, a generator and pacing leads. The leads connect the pacemaker to the heart and stimulate the heart with the pulses generated in pacemaker. Battery and generator are inside a titanium container which is placed inside the body.

Figure shows the block diagram of a pacemaker. The main blocks fall into four parts

1) At the input, there are sensing system, amplifier, filter, and analog to digital converter.

2) The digital output of the ADC is fed to the logic block.

This consists of a programmable logic, timing control system and therapy algorithms.

3) Current and voltage reference generator and battery power management.

4) At the output of the pacemaker, high voltage pulse generator and multiplier exist.

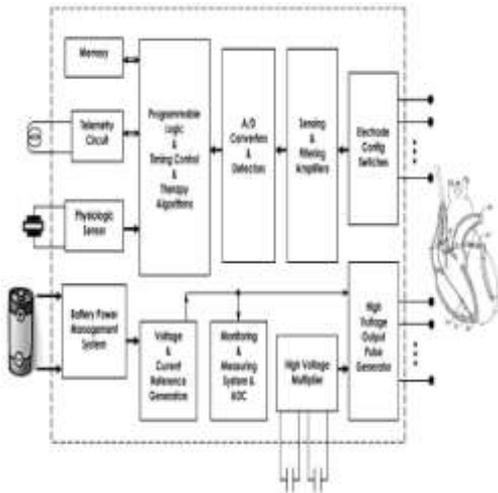


Fig 1: Functional Blocks of Peace Maker

III. SUCCESSIVE APPROXIMATION ADC

This section describes different components of SAR ADC architecture. The main components of SAR ADC are a Sample and Hold, a Digital to Analog Converter (DAC), a Comparator and a SAR Logic.

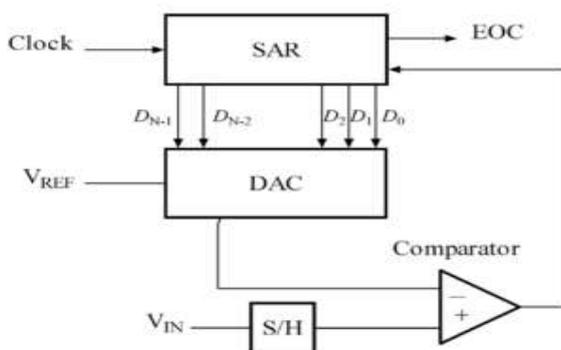


Fig 2: Sample & Hold

A. Sample & Hold

The Sample & Hold uses a capacitor and an analog switch to connect or isolate the capacitor from the input. An operational amplifier connected as follower avoids the effects of the load. The amplifier can be powered down in order to reduce the power consumption when the circuit is in the standby mode.

The most basic form of the sample and hold circuit combines a switch and a capacitor, the operation of the circuit as

follows. In sampling mode the switch is “on”, creating the signal path that allows the capacitor to track an input voltage. When the switch is “off” an open circuit is created that isolates the capacitor from the input, hence changing the circuit from sampling mode into holding mode.

B) Digital to Analog Converter

The Digital to Analog Converter has a resolution of 8 bits. The converter has been divided into two 4 bits D/A converters to reduce the total area. Each block can be powered down independently to reduce the power consumption.

In this architecture we are using R-2R ladder network DAC. The advantage of the R-2R ladder method is only two values of resistors are used greatly simplifying the task of matching or trimming and temperature tracking. Since the output of the R-2R DAC is the product of the reference voltage & digital input word, the R-2R ladder DAC is often called as MDAC.

C) Comparator

The comparator is an essential part in the SAR ADC to perform the binary search algorithm. Comparator in the SAR ADC takes more power consumption than the other blocks. A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage.

In an ideal comparator, with infinite gain, for input voltages higher than the reference voltage, the comparator outputs logical one and for the input voltages lower than the reference voltage it produces zero at the output.

D) SAR LOGIC

Successive Approximation Register (SAR) control logic determines each bit successively. The SA register contains N bit for an N-bit ADC. There are 3 possibilities for each bit, it can be set to ‘1’, reset to ‘0’ or keeps its value. In the first step, MSB is set to ‘1’ and other bits are reset to ‘0’, the digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared to the sampled input.

Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC, the MSB remains at ‘1’, otherwise it is reset to ‘0’. The rest of bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion.

Successive approximation register ADC implements the binary search algorithm using SAR control logic.

In general, there are mainly two fundamentally different approaches to designing the SAR logic. The first one which is proposed by Anderson consists of a ring counter and a shift register. At least 2N flip flops are employed in this kind of SAR. The other, which is proposed by Rossi, contains N flip flops and some combinational logic.

IV. EXPERIMENTAL RESULTS

A) Sample & Hold

In below figure voltage follower is placed after the capacitor in order to avoid the loading effect on the capacitor. The S/H operation is conceptually illustrated by the circuit shown. The opening and closing of the switch or sampler is controlled by a sample command (i.e., clock).

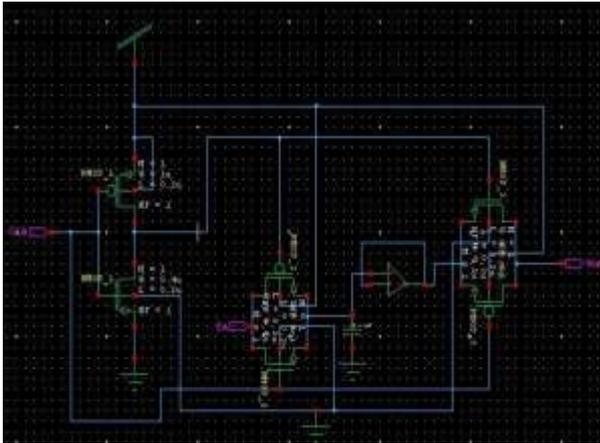


Fig 3: Design Of Sample & Hold

When the switch is closed (clk='1'), the capacitor C charges that is samples and tracks the input signal. When the switch opened (clk='0'), the output is held at the voltage that the capacitor is charged to at V_o , until the next sampling pulse arrives (clk='1'). The time interval during which the sampler is closed is called the sampling duration period P.

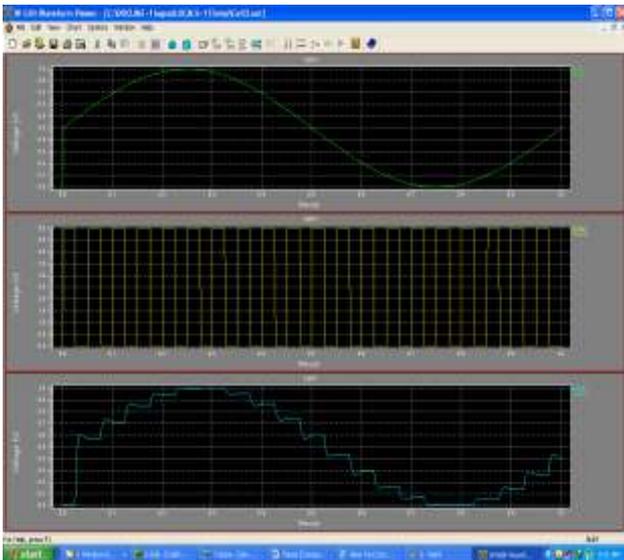


Fig 4: Sample & Hold Waveforms

B) Comparator

A comparator generates a logic output high or low based on the comparison of the analog input with a reference voltage.

The comparator in the SAR ADC takes more power consumption than other blocks. In SAR ADC we must design comparator such that it consumes very less power.

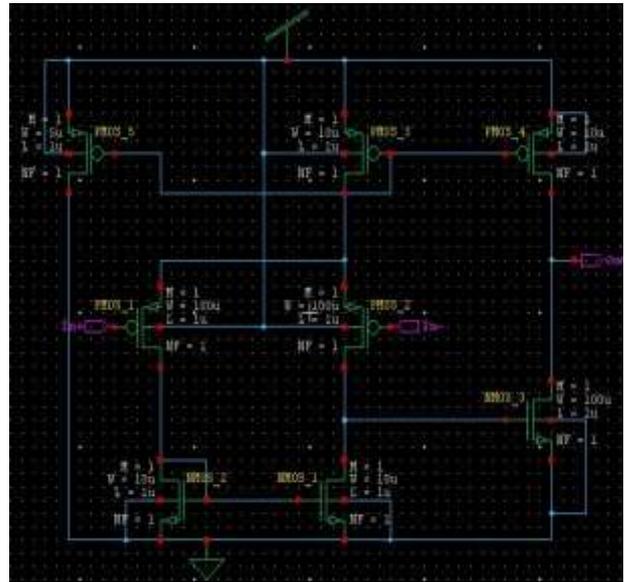


Fig 5: Design of Comparator

In the below Figure 'In-' given to the -ve terminal and the In+ given to the +ve terminal of comparator, when $In+ > In-$ the output is Out (5 volts) and 0 volts when $In+ < In-$.

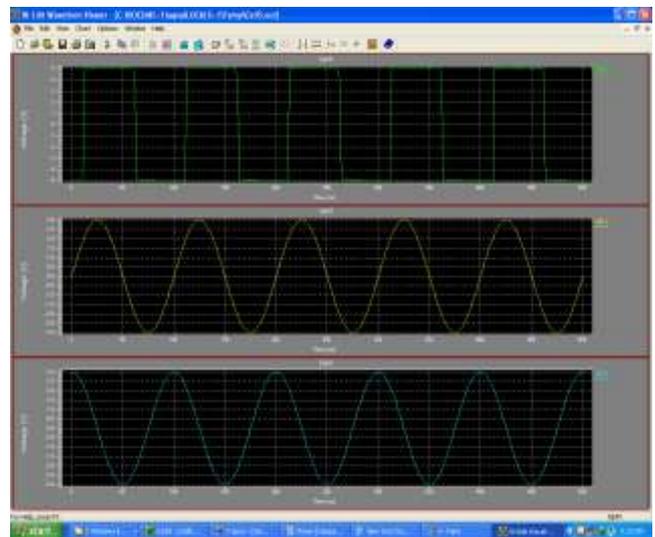


Fig 6: Waveforms of Comparator

C) SAR Logic

This control logic encompasses a ring counter and a code register. The ring counter is in fact a shift register. In each clock cycle, one of the outputs in the ring counter sets a Flip Flop in the code register. The output of this Flip Flop which is set by the ring counter is used as the clock signal for the

previous Flip Flop. At rising edge of the clock, this Flip Flop loads the result from the comparator.

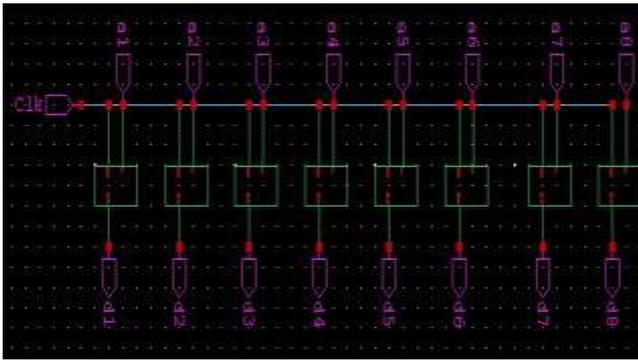


Fig 7: SAR logic

The Flip Flops which are employed in this structure are set-reset D-FFs. For low power purpose, transmission gate based Flip Flops are used. Minimum size transistors with double length are chosen for improving the power performance.

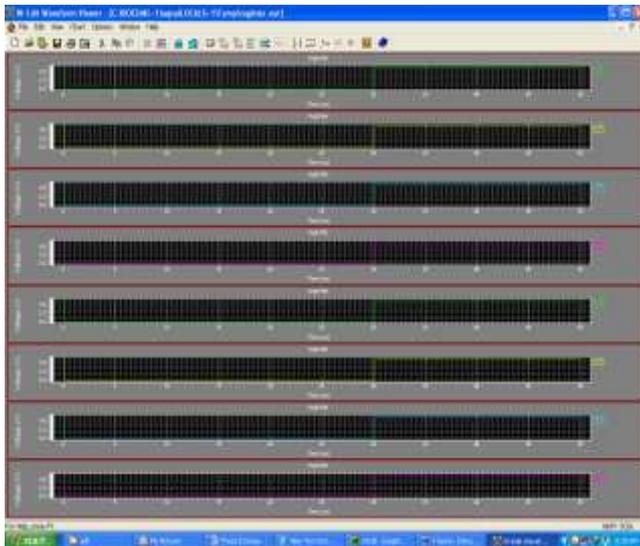


Fig 8: Waveforms of SAR logic

D) SAR ADC

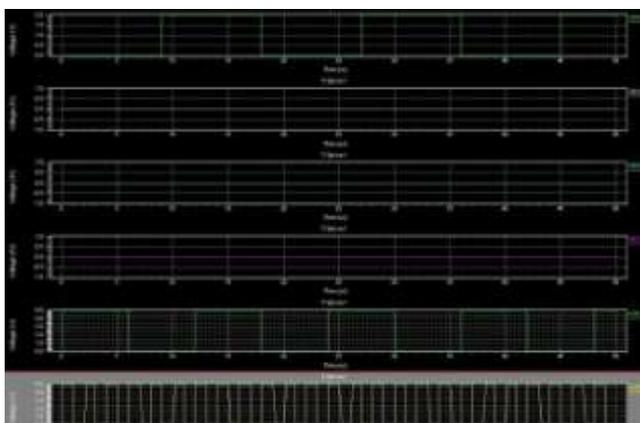


Fig 9: Waveforms of SAR ADC

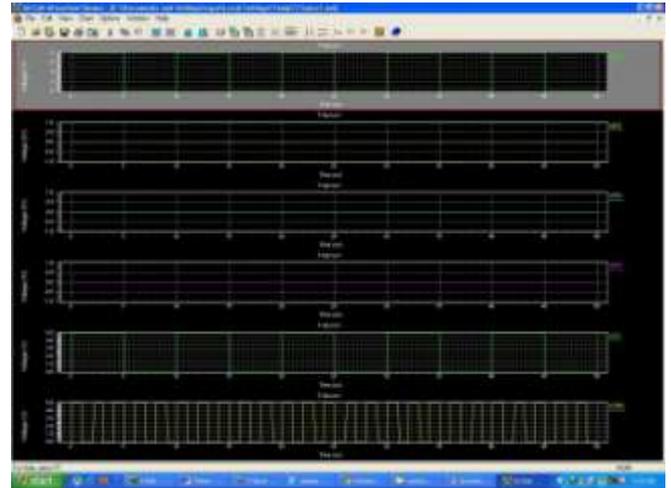


Fig 10: Waveforms of SAR ADC

The power consumption of this ADC mainly depends upon the performance of the comparator. The power consumption of the other components such as SAR LOGIC, DAC and D- Flip Flops are negligible.

As the D-Flip Flops and SAR logic are the digital components they consume less power compared to analog ones. Also R-2R DAC consumes less power compared to comparator during the process

V. CONCLUSION

A successive approximation ADC is suitable for operation at ultra low supply voltage is realized in a 0.13um CMOS technology using standard threshold CMOS devices and avoiding the bootstrapping techniques. This SAR ADC is well suited for biomedical applications such as Pacemaker, MRI and EEGs.

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