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Transformation of Graph Partitions into Problem Domain in Digital Circuit Layout

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***Abstract*—The digital circuit layout problem is a constrained optimization problem in the combinatorial sense. It is accomplished in several stages such as partitioning, floorplanning, placement and routing with each step being a constrained optimization problem. Partitioning is one of the first steps in VLSI circuit design. The technique is applied recursively until the complexity in each subdesign is reduced to the extent that it can be handled efficiently by existing tools. This technique is of great importance since it directly affects the rest of the steps in the process. The paper presents three encoding techniques for representation of circuit in the form graph for solving the circuit partitioning problem in context with Digital circuit Layout.**

***Index Terms*—Circuit Partitioning, Evolutionary approach, Hypergraph.**

I. INTRODUCTION

Practically, all aspects of the layout problem as a whole are intractable; that is, they are NP-hard. The alternate is to exploit the heuristic methods to solve very large problems. One of these methods is to break up the problem into sub problems, which are then solved one after the other. Almost always, these sub problems are NP-hard too, but they are more amenable to heuristic solutions than is the entire layout problem itself [1]. Each one of the layout sub problems is decomposed in an analogous fashion. In this way, the procedure is repeated to break up the optimization problems until reaching primitive sub problems. These sub problems are not decomposed further, but rather solved directly, either optimally if an efficient polynomial-time optimization algorithm exists or approximately if the sub problem is itself NP-hard or intractable

The circuit-partitioning problem consists of finding a decomposition of the target circuit into non-overlapping sub circuits with at least one logical gate in each sub circuit. With hypergraph representation of digital circuit, modern hypergraph partitioning algorithms based on evolutionary approach are used as a divide-and-conquer tool to achieve the objectives [2]. These partitioning algorithms implemented based on evolutionary approach possess many desirable properties in terms of run time, quality of partitions generated, cut size, and scalability. Various solution encoding schemes are used in literature for partitioning the circuit using evolutionary approach [3, 4, 5, 6]. The encoding method affects the quality of solution. The work presents three ways to map the graph partitions into problem domain and investigate their performance.

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II. TRANSFORMATION OF GRAPH PARTITIONS INTO PROBLEM DOMAIN

The work presents three ways to transform the graph partitions to represent the partitions of circuit for circuit partitioning problem. The ways are:

- A solution of length n on a binary alphabet is an n-tuple $< c_1, c_2, : : : , c_n >$ where $c_i = \{0,1\}$ for $i = 1, 2, \ldots . , n$ with n representing number of cells. Each solution represents one of the feasible partitions. Each cell is represented by 1 bit in the solution, the value of which determines the partition to which the cell is assigned. The total number of cells reflects the length of solution.
- The graph G= (V, E) (|v| = n) is represented with 2n identical single stranded SCA memory strands each with (2n) bit regions. The first n bit region represents the presence/absence of vertex in the first partition and the rest n bit region represents the presence/absence of an edge crossing the partition emanating from that i^{th} vertex.
- The graph G= (V, E) (|V| = n, |E|=m) is represented with 2n identical single stranded DNA memory strands each with (n+m) bit regions. The first n bit region represents the presence/absence of vertex in the first partition and the rest m bit region represents the presence/absence of an edge crossing the partition.

III. NET CUT EVALUATION

Let P represents an n-tuple < c1, c2, : : : , cn > where ci ={0,1} for i = 1, 2, , n., a feasible solution to the circuit partitioning problem with n number of gates and m hyperedges. Let $\bar{P}$ is the bitwise compliment of solution bit string P. Given M_{ij} representing the mask for N_i net and is the j^{th} bit position of M_i. The net cut evaluation is performed using bit-mask operations as shown below:

Step 1: Calculate X_i and Y_i for each net i = 1, 2, …….,n such that

X_i = P *bitwise AND* M_i *and*
Y_i = $\bar{P}$ *bitwise AND* M_i *for* i = 1, 2, …….,n

Step 2: If both X_i *=1 and* Y_i *=1* then net M_i is present in both partitions, hence a cut. Otherwise no cut.

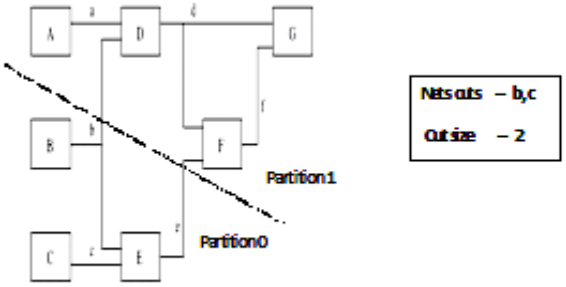

Fig 1: Nets labeled 'b'and 'e'are present in both partitions, contributing to net cut.

For the circuit shown in Figure 1 the partitioning solution, P is represented by 7 bit tuple as follows

BFS ordering of vertices	A	D	B	C	F	G	E
P, the partition solution	1	1	0	0	1	1	0
$\bar{P}$the bitwise compliment of P	0	0	1	1	0	0	1

Calculate X_i and Y_i for each net $i \in (a,b,c,d,e,f)$

	ADBCFGE	**Partition, P**	$\bar{P}$	X_i	Y_i	**Net Cut**
a	1100000	1100110	0011001	1	0	No
b	0110001			1	1	Yes
c	0001001			0	1	No
d	0100110			1	0	No
e	0000101			1	1	Yes
f	0000110			1	0	No

IV. STUDY OF THE ENCODING METHOD FOR SOLUTION REPRESENTATION

The first way(Fig. 2) to transform the graph partition to represent the partitions of circuit for circuit partitioning problem is the most common way for representation of circuit as graph partition [2, 3].

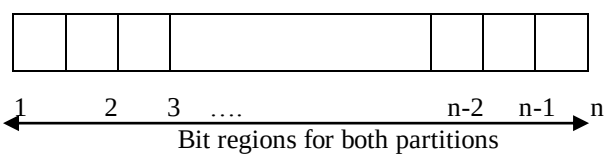

Fig 2: 1st way to encode solution

Although this solution representation is commonly used for the circuit partitioning using evolutionary approach, but it is not the most suitable because of the high redundancy. The encoding technique may further require repair operator in case of evolutionary operations.

The second way (Fig. 3) to transform the graph uses 2n bit strand to represent the solution.

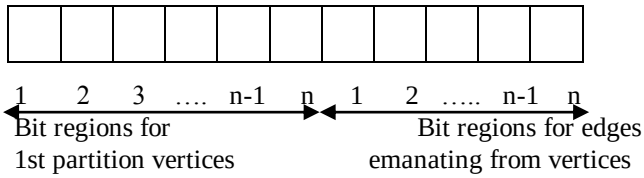

Fig 3: 2nd way to encode solution

The third way (Fig. 4) to transform the graph uses (n+m) bit strand to represent the solution.

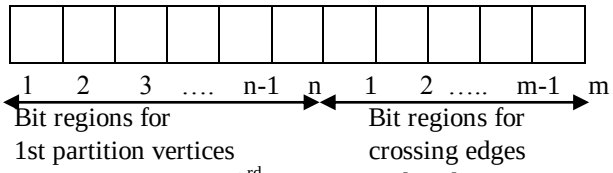

Fig 4: 3rd way to encode solution

The second encoding technique is suitable when the circuit is a dense circuit i.e having more connections.

V. CONCLUSION

The paper describes 3 ways to map the graph partitions into problem domain with each encoding scheme having its own advantages and disadvantages. The first encoding technique is most commonly used technique for solving circuit partitioning problem using evolutionary approach. Rest of the encoding techniques can be of great use in soft computing and DNA computing approach for solving the problem of partitioning in context with Digital circuit layout.

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