ISSN: 2278 – 1323
*International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)*
*Volume 2, Issue 4, April 2013*

# Leakage Power Reduction Through Hybrid Multi-Threshold CMOS Stack Technique In Power Gating Switch

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**Abstract**

**In this paper Two Hybrid digital circuit design techniques are produced as Hybrid Multi-Threshold CMOS complete stack technique and Hybrid Multi-Threshold CMOS partial stack technique for reducing the leakage power dissipation in mode transistion.Tri-modal switch are performance depends on these two techniques reduce the leakage power dissipation. These technique are implemented in the CADENCE virtuoso tool to find the leakage power dissipation and propagation delay. This proposed Hybrid techniques are proved better leakage power reduction than the MTCMOS techniques**.

**Keywords-MTCMOS,leakagepower,sleep transistor.**

## I.Introduction

### 1.1 Motivation of this Project

Low power designs are desirable for various reasons including competent energy and temperature characteristics, higher battery time for portable devices, and lower packaging and maintenance costs. MTCMOS technology provides a simple and effective power gating structure by utilizing high speed, low Vt (LVT) transistors for logic cells and low leakage, high Vt (HVT) devices as sleep transistors [7].

MTCMOS circuits suffer from some drawbacks such as long wakeup latency, large amount of rush-through current, and wasteful energy usage during mode transition. MTCMOS technology perform the PMOS and NMOS sleep transistor are connected as a high threshold voltage and logic circuit connects the low threshold voltage. some testing circuits are used as to analysis the MTCMOS technology.

Threshold voltage of transistors used in design of digital circuits should be adjusted for maximum saving in the leakage power dissipation. Circuit techniques play a very important role to control the subthreshold leakage power dissipation in the mode transistion.such as Multi-threshold CMOS(MTCMOS) technique are available in literature to control the subthreshold leakage power dissipation in deep submicron and nano scale technologies. The major components of leakage power dissipation are subthreshold leakage, gate leakage, gate induced drain leakage, and forward biased diode leakage.

### 1.2 Aim of this project

Subthreshold leakage dominates the other leakage components in deep submicron and nanoscale technologies. Tri-modal MTCMOS switch design, in the form of header or footer, which can operate in three different modes: active, drowsy, and sleep.That the drowsy mode, an intermediate power saving mode, reduces the leakage current while preserving the content of the cell[1]. To reduce the leakage power during mode transisition in the various modes at the same circuit.

### 1.3 Previous Work

The Tri-modal switch has two input signals called SLEEP and DROWSY. This switch enables three different circuit operation modes: sleep, drowsy, or active, depending on the value of the two control signals (Table I).

**TABLE I**

**TRIMODE SWITCH FUNCTIONALITY**

| SLEEP | DROWSY | SWITCH FUNCTION |
|---|---|---|
| 0 | X | ACTIVE |
| 1 | 0 | SLEEP |
| 1 | 1 | DROWSY |

When SLEEP is “0”, MS1 is ON and the voltage level at GS is VDD. Thus, independent of the value of the DROWSY input, the MS transistor is ON and the circuit is in the active mode.

When SLEEP is "1", the tri-modal switch operates in the sleep or drowsy mode depending on the value of the DROWSY signal. In particular, if DROWSY is "0", MS2 and MD2 will both be ON, MS is OFF, and the Tri-modal switch cell will operate in sleep mode.If SLEEP and DROWSY is "1", MS2 and MD1 will be ON, creating a negative feedback between VVSS and GS nodes which puts the circuit block into the drowsy mode (see Table I).
Tri-modal switch has two input signals called SLEEP and DROWSY. This switch enables three different circuit operation modes: sleep, drowsy, or active, depending on the value of the two control signals (Table I).The Fig 1 shows the Tri-modal footer type of MTCMOS switch.same as like the header type also connected with the PMOS and logic circuits in the switch. We use thick lines to draw the gate plate of HVT transistors.

since the drowsy signal changes only during sleep to drowsy or drowsy to sleep transitions, it need not be fast. Therefore, the always-on inverter that receives the DROWSY input in Fig. 1 may be implemented with HVT devices for leakage saving.The transistor count overhead of the tri-modal switch is only four (MD1, MD2, and the two transistors inside the inverter that feeds into gate terminal of MD2) compared to a regular bimodal MTCMOS switch.

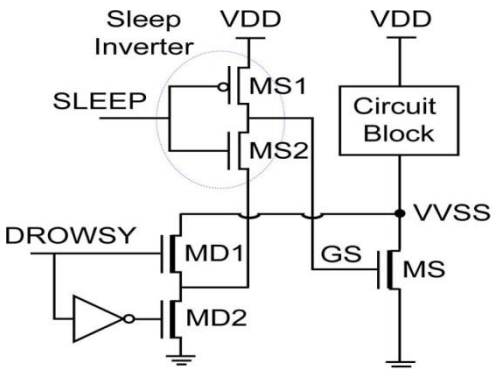


**Fig 1. Implementation of the trimode footer cell.**

The paper is organized as follows. In section II. Proposed work. In section III. Proposed work circuit discription. In section IV. Results and discussion is presented. Followed by conclusions in section

## II Hybrid MTCMOS Stack Technique Used In Tri-Modal Switch

### A. Introduction

The proposed technique combines the advantages of both MTCMOS and Stack techniques. This hybrid technique is further classified into two types depending on the stacking of transistors.

1. Hybrid MTCMOS Complete Stack Technique

2 .Hybrid MTCMOS Partial Stack Technique

These Hybrid techniques provide the improved performance in terms of Leakage power compared with the other techniques. In this technique, a high threshold voltage PMOS transistor (sleep PMOS transistor) is inserted between *VDD* and the pull up network and a high threshold voltage NMOS transistor (sleep NMOS transistor) is inserted between the pull down network and GND.

## III. Circuit Description

### A.Hybrid Multi-Threshold CMOS Complete Stack Technique

The proposed logic circuit for hybrid MTCMOS complete stack technique is shown in Fig 2 In this technique, a high threshold voltage PMOS transistor (sleep PMOS transistor) is inserted between *VDD* and the pull up network and a high threshold voltage NMOS transistor (sleep NMOS transistor) is inserted between the pull down network and GND. Then stacking of all transistors (high *VTH* sleep PMOS, high *VTH* sleep NMOS and low *VTH* transistors of the logic circuit) are done by replacing each transistor of width *W* with two series connected transistors of width W/2.

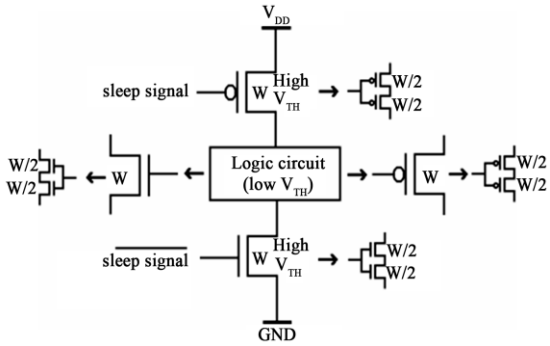


**FiG 2 Logic circuit using hybrid MTCMOS complete stack technique**

During standby mode, the sleep signal is active high, making the stacked sleep transistors in cut off state. So, the logic circuit is disconnected from *VDD* and GND. This reduces the sub threshold leakage power dissipation significantly by utilizing stacking effect in both high *VTH* sleep NMOS and sleep PMOS transistors during their cut off states.

The high *VTH* NMOS and PMOS stacked sleep transistors are turned on during normal or active circuit operation, when the sleep signal is active low.

**B.Hybrid MTCMOS Partial Stack Technique**

The proposed logic circuit for hybrid MTCMOS partial stack technique is shown in Fig 3 In this technique, a high *VTH* PMOS transistor (sleep PMOS transistor) is inserted between VDD and the pull up network and a high *VTH* NMOS transistor (sleep NMOS transistor) is inserted between the pull down network and GND. Then stacking of only high *VTH* sleep PMOS and high *VTH* sleep NMOS transistors are done. In this technique, stacking of low *VTH* NMOS and PMOS transistors of the logic circuit is not performed. Here, only partial stacking of high *VTH* sleep PMOS and sleep NMOS transistors are done to reduce the overall circuit propagation delay in active mode.

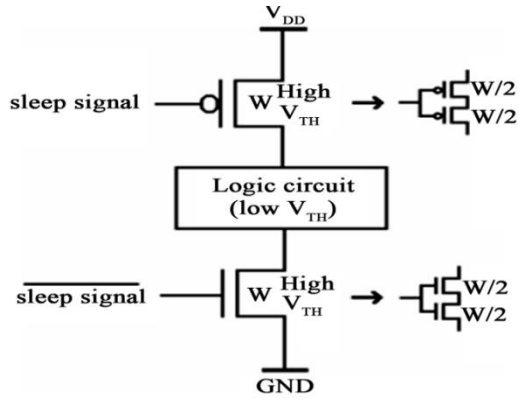


**Fig 3 Logic circuit using hybrid MTCMOS partial stack technique**

During standby mode (when sleep signal is active high), the stacked high *VTH* sleep PMOS and sleep NMOS transistors are turned off, thereby, reducing significant sub threshold leakage power dissipation. In active mode, the stacked sleep transistors are turned on. The circuit propagation delay using this technique in active mode is slightly reduced as compared to the previous technique because of partial stacking of transistors (stacking of only sleep PMOS and sleep NMOS transistors).

## IV. RESULTS AND DISCUSSION

The hybrid MTCMOS stack techniques are used in the tri-modal switch to applying input to the sleep and drowsy the logic circuit to under go anyone mode.

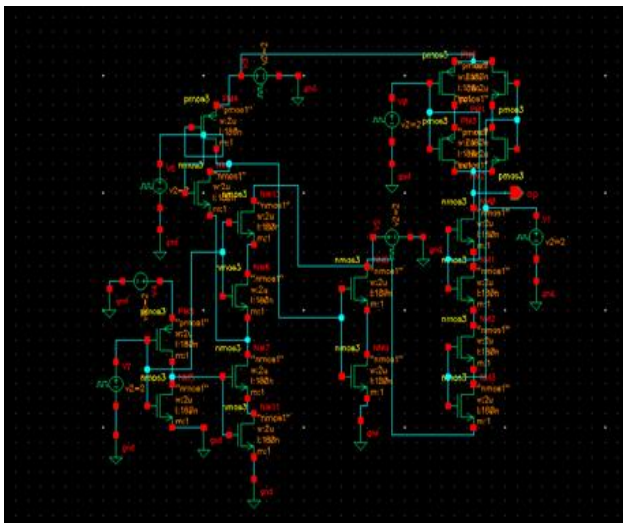

**Fig 4 Schematic Design of Hybrid MTCMOS Complete Stack Technique using tri-modal switch**

Any testing circuit used to the logic circuit analysis the performance in the tool. CADENCE virtuoso tool used to analysis the performance in the 180nm technology. The leakage power reduced the Hybrid techniques to compare the MTCMOS technique.

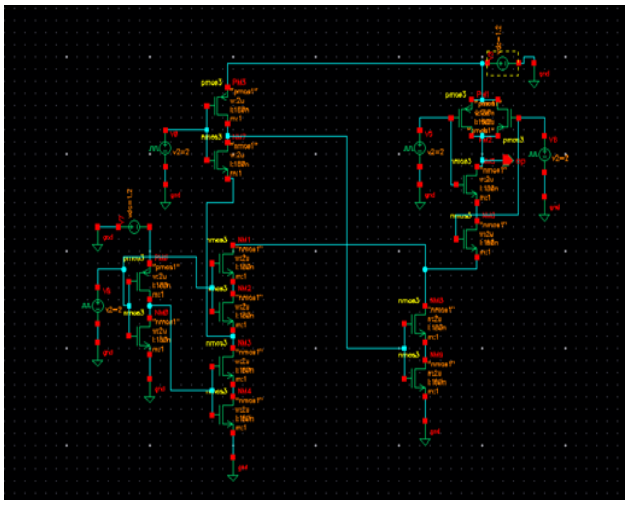

**Fig 5 Schematic Design of Hybrid MTCMOS Partial Stack Technique using tri-modal switch**

The Fig 4 and 5 shows the complete and partial stack technique in the switch. The leakage power and propagation delay to calculate the both these technique to compare with the MTCMOS.

**TABLE II**

**LEAKAGE POWER COMPARISONS FOR TRI-MODAL SWITCH USING 180NM TECHNOLOGY**

| Techniques | Leakage Power(W) | | |
|---|---|---|---|
| | Active | Drowsy | Sleep |
| MTCMOS | 114.54m | 95.28m | 38.97m |
| Hybrid MTCMOS complete stack | 388.67µ | 338.1µ | 66.41µ |
| Hybrid MTCMOS partial stack | 375.81µ | 295.62µ | 54.85µ |

The threshold voltage of high *VTH* transistor was taken as two times of *VTH* of normal transistor of the logic circuit. The threshold voltage of normal NMOS and PMOS transistors (low *VTH*) were taken as 0.20 V and −0.20 V respectively. The VDD is to be 1.2 V in the switch while performance

From the Table II Hybrid MTCMOS partial stack circuit has the lowest leakage power among all configurations, making it the most appropriate choice than others. The drowsy mode of the Hybrid MTCMOS partial stack circuit is prefer than the others. Therefore the hybrid techniques provides a reasonably Low-Leakage solution than others.

Subthreshold leakage power dissipation was measured by combining all possible input vectors. The voltage magnitude of input vector should always be less than the threshold voltage of the normal transistor of the logic circuit.

Sleep NMOS and sleep PMOS transistors were turned off during measurement of subthreshold leakage power dissipation in standby mode while for its measurement in active mode, all sleep NMOS and sleep PMOS transistors were turned on.The output will be simulated in the 50ns time interval.

The propagation delay to be calculated in the CADENCE tool for the hybrid techniques is higher than the conventional MTCMOS technique.

**TABLE III**

**PROPAGATION DELAY COMPARISONS USING 180NM TECHNOLOGY**

| Techniques | Propagation delay(ps) |
|---|---|
| MTCMOS | 4.02 |
| Hybrid MTCMOS partial stack | 9.93 |
| Hybrid MTCMOS complete stack | 15.86 |

From the Table III Hybrid MTCMOS complete stack technique has the higher propagation delay among all configurations, making it the most appropriate choice than others. The propagation delay to be calculated in the CADENCE tool for the hybrid techniques is higher than the conventional MTCMOS technique. Hybrid MTCMOS partial stack delay is lower than the complete technique. The table III shows the result for the propagation delay for 50ns time interval in the cadence virtuoso tool used.

## V CONCLUSION

This paper presented a Hybrid technique combines the advantages of both MTCMOS and Stack techniques. Thus the stack techniques are used in the Tri-modal MTCMOS switch design enabling three different modes: active, drowsy, and sleep. Leakage power reduction in the mode transistion is reducing to comparing with MTCMOS. The propagation delay of the hybrid technique is higher than the MTCMOS technique. The Hybrid MTCMOS partial stack is lower leakage power dissipation than the complete technique. From the results drowsy mode is the intermediate mode in the tri-modal switch.

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