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A Wide Range All Digital Feedback Duty Cycle Corrector

K. Sindhuja, **PG** *scholar, Karpagam University, Coimbatore, India.*
C. Pandiarajan M.E, *Assistant Professor, Karpagam University, Coimbatore, India.*

Abstract **- This concise presents a Modified Successive Approximation Register (MSAR)-based duty cycle corrector (DCC), which achieves low jitter, fast lock time with an accurate 50% duty cycle correction. This Modified SAR adopts a binary search method to condense lock time while maintaining tight synchronization between effort and production clocks. The projected DCC consists of a duty-cycle detector, a duty-cycle adjuster, MSAR controller. In order to obtain fast duty-correction with a tiny die region, a MSAR-controller is demoralized as a duty-correction controller. A modified successive approximation register-controller reduces the locking time and allows the DCC to follow the process, voltage, temperature, and load variations (PVDL). The MSARDCC circuit has been implemented in a 0.18- µm CMOS process which corrects the duty rate within 5 cycles which has a closed loop characteristic. The measurement power dissipation and area occupation are 5581nW and 0.033mm^2 respectively.**

Keywords **— Duty Cycle, Duty cycle corrector (DCC), Double data rate (DDR), Modified Successive Approximation Register (MSAR), PVTL.**

I. INTRODUCTION

1.1 Motivation of this Project

The majority frequent clock signal is in the form of a square wave with a 50% duty cycle, typically with a preset, stable frequency. Circuits using the clock signal for synchronization may become dynamic at either the growing edge, declining edge, or, in the case of double data rate, together in the growing and in the declining limits of the clock cycle.

A clock with 50% duty cycle is very important in many applications such as DDR-SDRAMs and double sampling analog-to-digital converters. To twice the data rate, mutually positive and negative transition edges of a clock are used. However, the duty-cycle alteration of a clock occurs owing to the unmatched rising time and falling time in the clocking paths. Therefore, the duty cycle of clock signal is complex to fix at 50%. Since improving the speed of computer systems demands low-power high-speed memory such as DDR3 and promising DDR4 DRAMs, it has become more important to develop a low-power high-performance DCC.

1.2 Aim of this project

The main objective of this project is to achieve 50% duty cycle in order to avoid corrupt data transmission caused by inappropriate data windows, leading to data rate reduction. Many duty cycle alignment circuits have been developed to solve the duty cycle distortion (DCD) of the clock, such as a duty cycle corrector (DCC).

1.3 Previous Work

There are two categories to realize the DCC in literature: the feedback type and non feedback one. The non-feedback digital DCCs have the advantage of fast duty-correction and low-power operation. However, the DCCs utilizing interruption have speed restrictions on the maximum operation frequency and the open-loop characteristic cannot follow the process, voltage and temperature (PVT) variations. The analog-feedback DCCs usually implement the negative feedback scheme which achieves higher duty cycle accuracy but it leads to long duty-correction time.

The non-feedback digital DCCs have the benefits of fast duty-correction and low-power operation and its open-loop characteristic cannot follow the process, voltage and temperature (PVT) variations. To compensate this PVT variation, it needs complex calibration and trimming circuitry, which increases the area over- head.

All digital-feedback DCCs can correct the 50% duty-cycle within the very short duty-correction time. However, DCCs uses convoluted duty-cycle detector structures such as a time-to-digital converter (TDC)-based detector, which increases the expenditure of hardware implementation and the performance of

TDC such as the linearity can degrade the complete DCC performance.

Before this work DCC has been implemented by using predictable SAR. In that, this predictable SAR stops their operation when its binary search operation has been completed. Thus the SARDCC becomes open loop and heavily affected by PVTL variations. To overcome this drawback, conventional SAR has been replaced by modified SAR, which automatically enters into a counter mode after its binary search operation has been completed.

This brief is organized as follows. In Section II, the architecture and operation of the proposed MSAR-DCC circuit are described. Also, the effectiveness of first exploiting the MSAR controller in the DCC circuit is discussed. Section III describes details of the implemented circuit. Section IV shows the results and discussions of the proposed circuit. Finally, the brief is concluded in Section V.

II. Proposed MSAR-DCC

The block diagram of proposed MSAR-DCC circuit is shown in Fig. 2.1.which includes a duty-cycle detector, a duty-cycle adjuster, and modified SAR controller. The MSAR controller, which adopts the binary search algorithm, controls the duty-cycle adjuster to correct the clock duty-cycle by 50%. When the *Start* signal goes to HIGH, the duty-cycle correction begins with initializing the control signals of the duty-cycle adjuster.

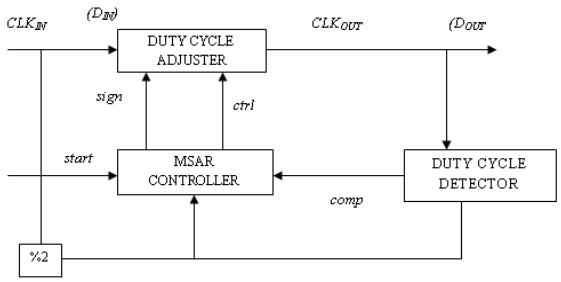

Fig.2.1. Block Diagram of the Proposed MSAR-DCC

Initially the duty cycle adjuster does not execute any operation. It passes input as output. Duty cycle detector detects the duty rate of an output clock and checks whether the duty rate is greater or lesser than 50%. Based on that it will produce output signal as *comp*. When the MSAR controller completes their binary search algorithm it will automatically enters into a counter mode. Therefore, closed loop operation has been maintained. Finally, the signal *End* goes to HIGH, which provides the end information of the duty-cycle correction to the delay locked-loop (DLL) in DDR DRAMs. The *Sign* bit is to decrease the chip area of the duty-cycle adjuster.

III Circuit Description

A. Duty-Cycle Adjuster

The DDR DRAMs need wide operation frequency range with digitally controllable duty-cycle adjuster for the power-down mode. The block diagram of the duty-cycle adjuster is shown in Fig. 3.1. This duty cycle adjuster consists of a changeable falling edge generator with 6-bit programmable delay lines, fixed rising edge generator with imitation delay lines, latch, and MULTIPLEXER. The falling edge generator performs the duty-rate adjustment with the non-inverted or reversed signal CLK_{IN} of the input clock CLK_{IN} by MUX selection and 6-bit control signals Ctrl [5:0] of the programmable delay line.

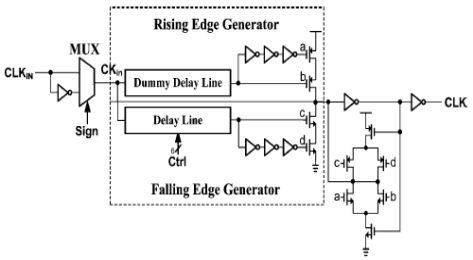

Fig.3.1. Duty cycle adjuster

The earlier delay-line based duty-cycle adjuster circuit uses falling edge generators or both rising and falling edge generators for the duty-rate adjustment. In order to decrease delay lines, here we use only a falling edge generator with the input inversion MUX for duty-rate adjustment. The main downside of this adjuster is that the DLL requires a specially planned phase detector, which consequences in a difficult DLL design.

B. Duty-Cycle Detector

The duty-cycle detector of the duty-rate comparator includes analog amplifier, latch and inverter buffers as revealed in Fig. 3.2.

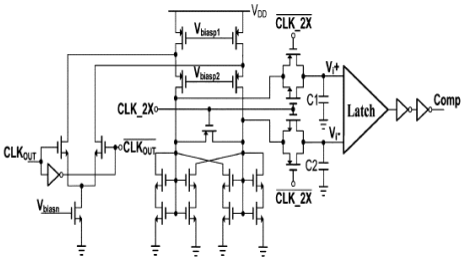

Fig.3.2. Duty cycle detector

First the folded preamplifier converts the differential clock signals into differential current signals and amplifies the current variation, which is incorporated into the capacitors C1 and C2. Then the latch amplifies the incorporated voltage variation to a digital signal. Since the duty-rate comparator operates at high speed, the first stage of the preamplifier requires ample bandwidth. Finally, bias voltages are externally calibrated in order to decrease the variance of the incorporated current and balance of the latch over the process deviation.

C.MSAR-Controller

The operation of the predictable SAR circuit stops when the binary search is completed. So, the DCC becomes open-loop and cannot follow the PVT variations. To accomplish the closed-loop operation, we need an additional counter. For a 6-bit predictable SAR controller, a 6-bit UP/DOWN counter is desirable. The hardware transparency is double. To accomplish the closed-loop operation after the binary search, the MSAR circuit is proposed in this paper. The closed-loop operation can be accomplished by entering the MSAR controller into a counter after its binary search operation has been completed. The hardware cost for the MSAR control system is only 50% of the predictable SAR with extra counter control scheme. The MSAR unit is identical to a predictable SAR unit when the signal Enable is logic 0 and becomes a counter unit when the signal Enable is logic 1. Fig. 3.4 reveals the realization of the MSAR unit.

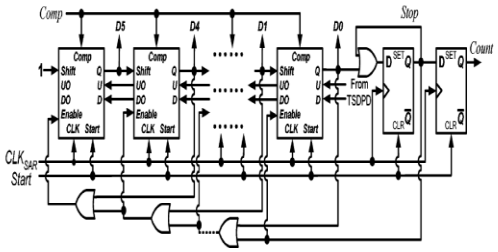

Fig.3.3. 6-bit MSAR circuit

The 6-bit Modified SAR circuit comprises of six MSAR units, two DFFs, and six OR gates, which is shown in Fig. 3.3. Later than the signal arises, the Modified SAR circuit is in the binary searching mode when the signal is logic 0. The signal decides the output of every SAR unit from the MSB to the LSB. Whereas the next MSAR unit performs the binary searching, the output throughout the OR gate arises and becomes the signal of the earlier MSAR unit to latch the determined value. At the same time, the preceding SAR unit is converted into a counter unit and starts to receive the outputs generated by the logic gates. The carry-out signals and for the counter mode are fashioned by the logic gates as fine. After the six-digit binary searching is finished, the signal arises to make sure that each MSAR unit is changed into a counter unit and the MSAR circuit enters the counter mode. Thus the closed-loop operation is accomplished.

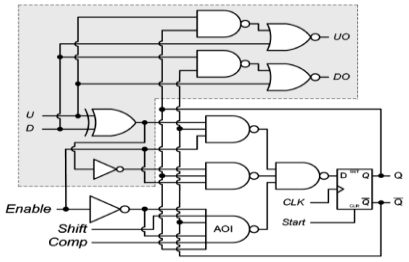

Fig.3.4.The implementation of MSAR unit

IV. RESULTS AND DISCUESSIONS

The model of the proposed MSAR-DCC has been implemented in a standard 0.18µm CMOS technology, by using CADENCE software. The active area is 0.033mm^2. Fig. 4.1 shows the calculated output clock waveform of the MSAR-DCC. The output of the DCC is corrected to 50% only within 5 cycles and Power consumption is calculated as 5581nW. Among the usual feedback type DCCs, this digital-feedback DCC has the smallest duty-correction time with the highest duty rate accuracy.

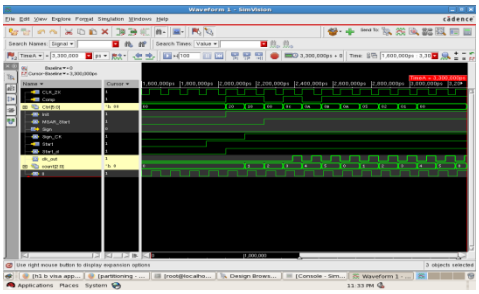

Fig 4.1 Output of MSAR – DCC

The Fig 4.1 shows the output of MSAR – DCC was obtained using Cadence digital lab tool nclaunch.

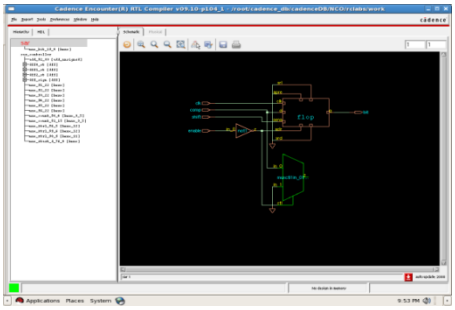

Fig 4.2 RTL Schematic of MSAR - DCC

The Fig 4.2 shows the RTL representation of MSAR – DCC was obtained using Cadence digital lab tool nclaunch.

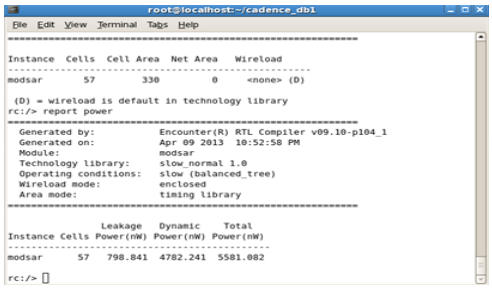

Fig 4.3 Power Report of MSAR - DCC

The Fig 4.3 shows the Power Report of MSAR – DCC was obtained using Cadence digital lab tool nclaunch.

TABLE I

PERFORMANCE SUMMARY OF MSAR – DCC

	MSAR – DCC
CMOS Technology	0.18µm
Architecture	Digital Feedback
Correction Time	5 cycles
Power Consumption	5581nW
Area	0.033mm^2

V. CONCLUSION

In this concise, a MSAR-DCC is obtainable. In order to accomplish the fastest duty-correction with small die area and to sustain the power-down mode, a MSAR-controller is proposed as a duty-correction controller. Within 5 cycles, the proposed DCC corrects the duty-cycle to 50%. The proposed MSAR-DCC achieves the fastest duty-correction time among feedback type DCCs.

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K.Sindhuja received B.E degree in Electronics and Communication Engineering from Maharaja Institute of Technology, Coimbatore under Anna University in 2011. Currently she is pursuing her PG VLSI Design in Department of Electronics and Communication Engineering, Karpagam University, Coimbatore-21, Tamil Nadu, India. She attended many International and National Conferences. Her research interests are in Duty cycle corrector circuit and mixed mode clock generator.

C.Pandiarajan working as an Assistant Professor in the Department of Electronics and Communication Engineering in Karpagam University, Coimbatore-21, Tamil Nadu, India. He received his B.E degree in Electronics and Communication Engineering from Mohamed Sathak Engineering College, in Chennai under Anna University in 2006. He got his M.E Degree in Anna University Coimbatore, India. He has one years of industrial experience and two years of institutional experience. His area of interest is RFIC design.