ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2, Issue 4, April 2013

Design of Differential LC and Voltage Controlled Oscillator for ISM Band Applications

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Abstract— **Oscillators are integral part of many electronic systems. An oscillator is an electronic device used for the purpose of generating a signal. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillators topologies and performance parameters. Robust, high performance oscillator design in CMOS technology continues to pose interesting challenges. CMOS circuitry in VLSI dissipates less power during static, and is denser than any other implementations having the similar functionality. As this advantage has grown and become more important, CMOS processes and variants for VLSI have come to dominate the others, so that the large number of modern integrated circuit manufacturing is on VLSI technology processes. In this paper differential LC oscillator and Voltage controlled oscillator are designed that generate the ISM band using VLSI technology with the help of EDA tool microwind3.1. Oscillators are designed in 120nm and 90nm VLSI technology to produce ISM band and compared for different parameters such as area, power, frequency etc**.

Index Terms—**Differential LC oscillator, voltage controlled oscillator, ISM band.**

I. INTRODUCTION

The 2.4 GHz industrial, scientific, and medical (ISM) Band is poised for strong growth [1]. The Bluetooth, ZigBee, Wi-Fi operate in 2.4GHz frequency [2]. This band can be obtained with the help of oscillator. Oscillatory behavior is appearing in all physical systems, especially in electronic and optical systems. In radio frequency and lightwave communication systems, oscillators are used for frequency translation and channel selection. Oscillators are also present in all digital electronic systems which require a time reference i.e. Clock signal in order to synchronies operations. An ideal oscillator would provide a perfect time reference i.e. a periodic signal. However all physical oscillators are corrupted by undesired perturbation/noise. Hence signal generated by practical oscillators are not perfectly periodic. Since oscillators is a noisy physical system and it makes them unique in their response to perturbation/noise. A variety of oscillators is Available but the principal of operation; the frequency band of oscillation and the performance in noisy environment are different from one class of oscillators to the other. Recently Communication transceiver design in single IC demands monolithic oscillator with low cost a low power dissipation. CMOS technology becomes widely used in RFIC and the CMOS one-chip solutions integrated both of digital and RF circuits start to be provided. In these one-chip solutions, the differential LC oscillator is commonly adopted as local oscillator because of the better phase noise performance [3]. The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO is commonly used for clock generation in phase lock loop circuits. The clock may vary typically by +/-50% of its central frequency [4]. The Software microwind3.1 used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain or access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately. The rest of this paper is organized as follows. Section II briefly introduces the differential LC oscillator; next, a voltage controlled oscillator is described briefly in section III. Section IV gives simulation setup. Then section V present results obtain in the paper. Finally, Section VI. Conclude this paper.

Manuscript received April, 2013.
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II. DIFFERENTIAL LC OSCILLATOR AND ITS OSCILLATION FREQUENCY

LC oscillators are commonly used in CMOS radio-frequency integrated circuits (RF-ICs) because of their good phase noise characteristics and their ease of implementation. However, no systematic design methodology exists to account for the many specifications (phase noise, power dissipation, voltage swing, tuning range . . .). Typical design strategies have tried to achieve a low phase noise by using the largest possible inductance value or by using inductors with the lowest possible series resistance. However, an optimal design requires the simultaneous consideration of both active and passive devices [5]. Due to their relatively good phase noise, ease of implementation, and differential operation, cross-coupled inductance–capacitance (LC) oscillators play an important role in high-frequency circuit design [6]. The LC oscillator used in this paper is not based on the logic delay, but on the resonant effect of a passive inductor and capacitor circuit. The schematic diagram of differential LC oscillator shown in fig 1 [3], the inductor L1 resonates with the capacitor C1 connected to S2, combined with C2 connected to S1.

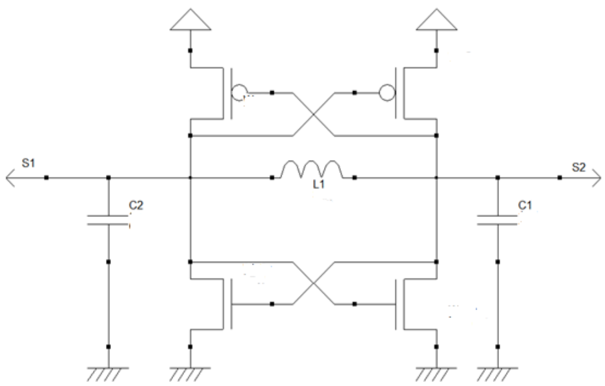

Fig.1 A differential LC oscillator

The layout implementation is performed using a virtual inductor L1 and two capacitors C1 and C2. Notice the large width of active devices to ensure a sufficient current to charge and discharge the huge capacitance of the output node at the desired frequency. Using virtual capacitors instead of on-chip physical coils is recommended during the development phase. It allows an easy tuning of the inductor and capacitor elements in order to achieve the correct behavior. Once the circuit has been validated, the L and C symbols can be replaced by physical components. The time-domain simulation shows a warm-up period around 1ns where the DC supply rises to its nominal value, and where the oscillator effect reaches a permanent state after some nano-seconds. The measured frequency approaches around 2.4GHz with a L1=400nH inductor and C1=C2=0.01pF in 120nm technologies, L1=380nH and C1=C2=0.01pF in 90nm technology shown in following figures.

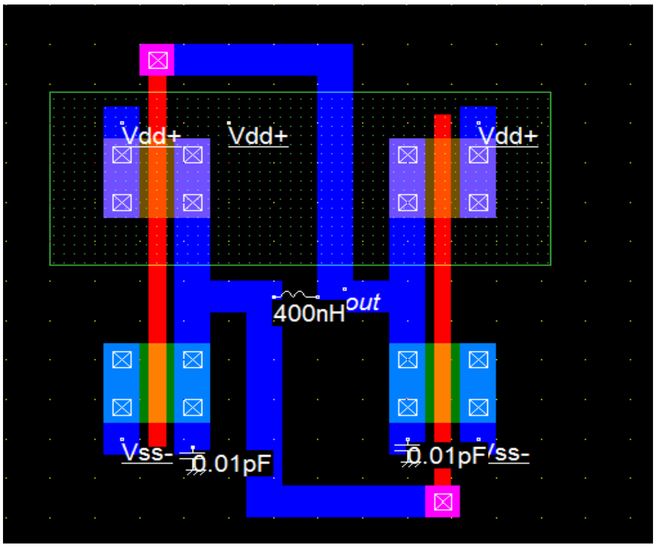

Fig.2 The layout implementation of a differential LC oscillator in 120nm technology

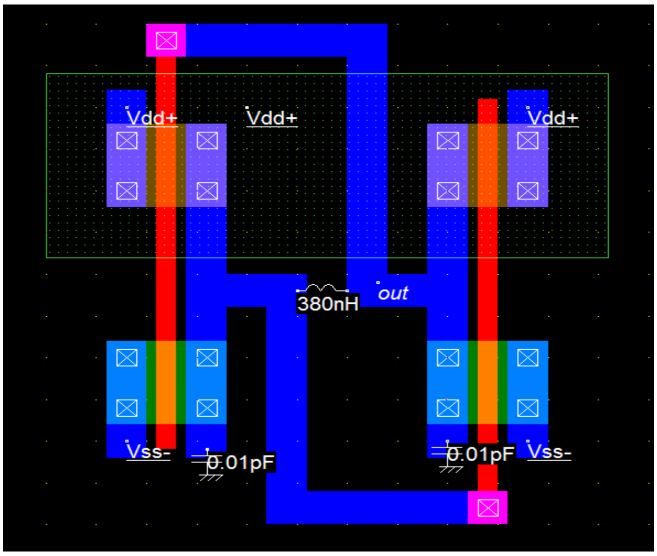

Fig.3 The layout implementation of a differential LC oscillator in 90nm technology

III. VOLTAGE CONTROLLED OSCILLATOR AND ITS OSCILLATION FREQUENCY

The most popular type of the VCO circuit is the current starved voltage controlled oscillator. In this circuit the numbers of inverter stages are used. The simplified view of a three stage current starved oscillator is shown in the fig 4. The voltage controlled oscillator (VCO) generates a clock with a controllable frequency. The VCO shown in fig.4 is commonly used for clock generation in phase lock loop circuits. The clock may vary typically by +/-50% of its central frequency. The current starved Inverter chain uses a voltage control Vcontrol to modify the current that flows in the N1, P1 branch. The current through N1 is mirrored by N2, N3 and N4. The same current flows in P1. The current through P1 is mirrored by P2, P2 and P4. Consequently, the change in Vcontrol induces a global change in the inverter currents, and acts directly on the delay. Usually more than 3 inverters are in the loop. A higher odd number of stages are commonly implemented, depending on the target oscillating frequency and consumption constraints [4].

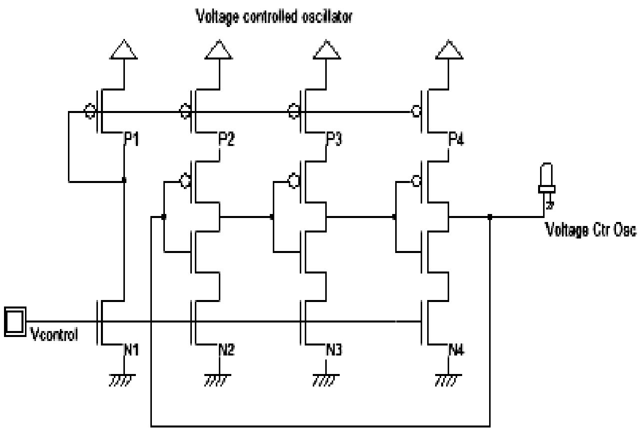

Fig.4 A voltage controlled oscillator

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International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2, Issue 4, April 2013

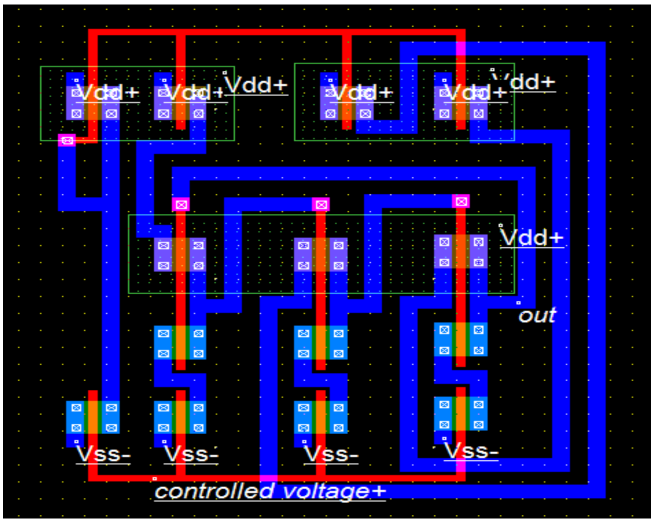

Fig.5 The layout implementation of a voltage controlled oscillator

The measured frequency reaches around 2.4GHz when the controlled voltage is 0.412v in 120nm technology and in 90nm technology it requires controlled voltage equal 0.241v

IV. SIMULATION SETUP

This paper describes the semi custom design of oscillators related to the CMOS 120 nm, 90nm technology and the implementation of this technology in Microwind3.1 There may exist several variants of the 120nm and 90nm process technology. One corresponds to the highest possible speed, at the price of a very high leakage current [4]. This technology is called “High speed” as it is dedicated to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc. The Software Microwind3.1 used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately.

V. EXPERIMENTAL RESULTS

The simulation of differential LC oscillator and VCO is given in following figures it shows frequency verses time. The power, area, current consumption is observed for frequency around 2.4GHz. Differential LC oscillator in 120nm technology require L1=400nH and C1=C2=0.01pF to generate frequency around 2.4GHz where as in 90nm technology it require L1=380nH and C1=C2=0.01pF. For VCO the measured frequency reaches around 2.4GHz when the controlled voltage is 0.412v in 120nm technology and in 90nm technology it requires controlled voltage equal to 0.241v. If we change the temperature, the device current changes, and consequently the oscillation frequency are modified. Such oscillators are rarely used for high stability frequency generators.

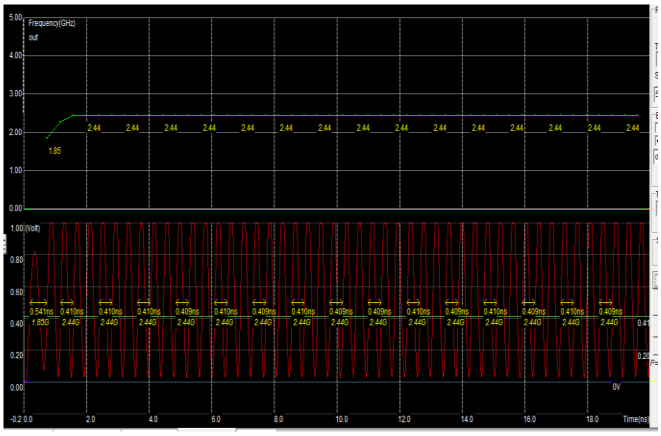

Fig.6 Layout simulation of VCO in 120nm technology.

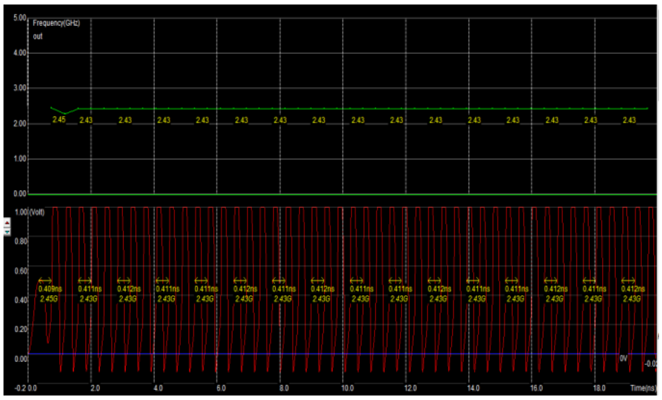

Fig.7 Layout simulation of differential LC oscillator in 120nm technology.

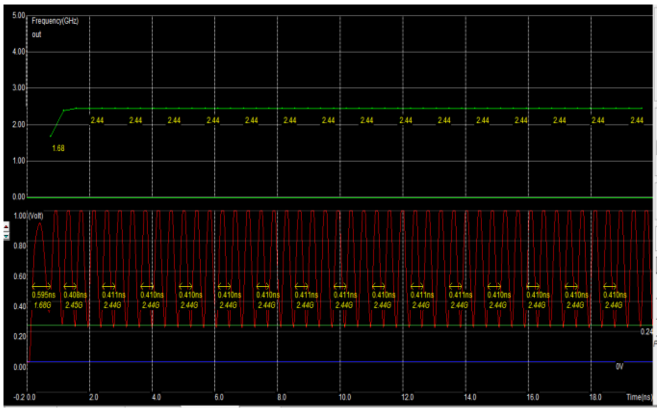

Fig.8 Layout simulation of VCO in 90nm technology

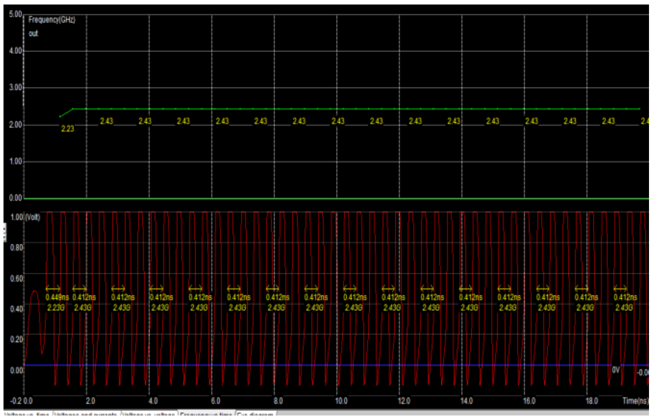

Fig.9 Layout simulation of differential LC oscillator in 90nm technology

Table I: Design parameter

MOS	120NM	90NM
PMOS width	0.600 µm	0.500 µm
PMOS Length	0.120 µm	0.100 µm
NMOS Width	0.600 µm	0.500 µm
NMOS Length	0.120 µm	0.100 µm

Table II: Comparison for 120nm technology

Parameter	Differential LC oscillator	Voltage controlled oscillator
Area estimation	Width =4.8 µm height =3.6 µm	Width = 7.7 µm height = 8.3 µm
Power estimation	P = 0.109 mW	P = 59.547 µW
Current estimation	Iddmax = 0.142 mA iddAvr = 0.091 mA	Iddmax = 0.055 mA iddAvr = 0.050 mA
Frequency estimation	2.43 GHz	2.44 GHz

Table III: Comparison for 90nm technology

parameter	Differential LC oscillator	Voltage controlled oscillator
Area estimation	Width =4.0 µm height =3.0 µm	Width = 6.5 µm height = 7.0 µm
Power estimation	P = 0.149 mW	P = 63.654 µW
Current estimation	Iddmax =0.280 mA iddAvr =0.124 mA	Iddmax =0.057 mA iddAvr =0.053 mA
Frequency estimation	2.43 GHz	2.44 GHz

VI. CONCLUSION

The Software used in paper allows us to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. It also includes all the commands for a mask editor as well as original tools never gathered before in a single module such as 2D and 3D process view, Verilog compiler, tutorial on MOS devices. You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately. In this paper oscillators are designed in 120nm and 90 nanotechnologies and compared on the basis of simulation result. In the estimated design more emphases given on generation of ISM band, power consumption, layout design and many more. This report is a brief study of differential LC oscillator and VCO on 120 and 90 nanometer VLSI technologies to achieve some objectives as mention above.

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