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A Novel BIST based Diagnosis Technique to Detect Faults in FPGA

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***Abstract*- Testing is considered as the major factor for many applications because of the high level fault detection and the fast hardware and software implementations, many of which are power and resource constrained and requires reliable and efficient hardware implementations. In this paper, Output response analyzer(ORA) based fault detection architecture of the Interconnect and Logic block for designing high performance fault detection structure of the FPGA is presented .The proposed output response analyzer based fault detection approach detects faults in both interconnect and logic block . This ORA-based fault detection scheme reaches the maximum fault coverage when compared to other methods of fault detection. The proposed fault detection of the Output response analyzer in this paper have the least area and power consumption compared to their counterparts with similar fault detection capabilities.**

***Index Terms*—Built in self test(BIST), LFSR, field programmable gate array.**

I. INTRODUCTION

Field-Programmable Gate array formally known as FPGA. It is an alternative for implementation of digital logic systems. The first static memory-based FPGA(commonly called as SRAM-based FPGA)allowed for both Logic and interconnect configuration using a stream of configuration bits. It contains the low classic array of configurable logic blocks(CLB) and inputs/ outputs. FPGAs are so called because they are structured very much like the now-obsolete "gate array form of ASIC". FPGAs can be programmed in minutes while ASICs require weeks to fabricate a new design.

Test and diagnosis of FPGAs can be categorized into application-independent and application-dependent methods. Application-independent approaches target faults in the entire FPGA to ensure functionality of the device for any possible user configurations. Here faults cannot be detected accurately. For the drawback of this fault detection we have been proposed the Application dependent method whereas, Application dependent techniques test and diagnose the FPGA resources with respect to a particular application mapped into the FPGA device. In these applications, the existence of Faults in the system are first identified and faulty resources are precisely diagnosed afterwards. Then, the design is remapped to avoid faulty resources. Because test and diagnosis procedures are performed during system operation (online), the number of test vectors and configurations must be minimized. Here in this paper a conventional BIST approach is presented where we can test and identify the faults. Due to this test time can be minimised. The rest of this paper is organized as follows. In Section II, the diagnosis technique for interconnect faults is described. In Section III, the diagnosis method for logic block faults is presented. Finally, Section V concludes this paper.

II. FPGA ARCHITECTURE

Each FPGA vendor possess their own FPGA architecture, but in general terms they are all a variation of that shown in fig.1.The architecture consists of configurable Logic blocks(CLB),configurable I/O blocks and programmable interconnects. Also, there will be clock circuitry for deriving the clock signals to each logic block. Configurable logic blocks(CLBs) contain the logic for the FPGA. The block contains Random access memory(RAM) for creating arbitrary combinatorial logic functions, also known as LUTs. It also contains Flip-flops for clocked Storage elements, along with multiplexer in order to route the logic within the block and to and from external resources.

A. Interconnect Testing Using Walsh Code:

Normally, an interconnect resources in FPGAs can be categorized as *inter-CLB* and *intra-CLB* resources. Inter-CLB routing resources provide interconnections among CLBs. Inter-CLB resources include programmable switch blocks and wiring channels connecting switch blocks and CLBs. Intra-CLB resources are located inside each CLB. Intra-CLB interconnects include programmable multiplexers and wires inside CLBs. For inter-CLB interconnect test and diagnosis, the configuration of routing resources remains unchanged while the configuration of logic resources is modified. The interconnects may be defined as a set of lines which can be connected by a set of programmable interconnect points(PIP) which act as switches. These interconnects

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can be classified as Local interconnect and Global interconnect. The local interconnects are associated with CLBs, including wire segments and connecting blocks.

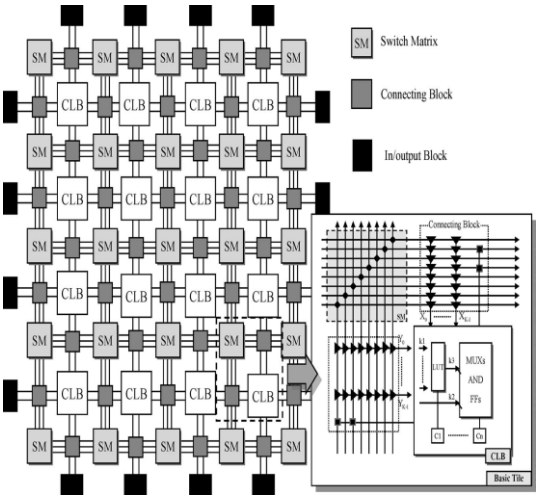

Fig. 1. SRAM-based FPGA architecture.

On the other hand, wire segments and programmable cross-point PSs (PCP-PSs) within the switch matrix (SM) in global interconnects form horizontal and verticalrouting channels that connect signals between CLBs. The input–output signals can be transmitted in-out of the FPGA using the input–output blocks (IOBs). In walsh code technique, the vectors can be converted to the activating inputs of LUTs implementing single-term functions. . The *activating* value of each net in a test configuration is the corresponding bit position of that Walsh code. The test vector in each test configuration is the activating values of primary input nets.. Since the test configurations target faults in inter-CLB interconnect, all additional logic resources in CLBs, if used, will be bypassed. Hence, CLBs are configured as LUTs followed by flip-flops (if those flip-flops are originally used in the user configuration).using this walsh code technique, interconnect faults can be detected easily and time also consumed less.

B. Logic Block testing using LFSR :

In Logic block diagnosis, the configuration of the original used logic blocks is preserved while the configuration of interconnects and unused logic blocks are changed to exhaustively test and diagnose all used logic blocks. In this BIST scheme, each used logic block will be exhaustively tested while all these logic blocks are tested concurrently. A linear feedback shift register (LFSR) technique is used in input of Logic block so that test time can be minimised more. The outputs of used blocks along with the parity predictor block are connected to the response compactor, which is also implemented in the available unused resources.

Fault dictionary is used to check the detection of faults. The overall faults can be detected in fault dictionary and can be arranged in order. Thus obtained faults can be compared with the fault dictionary and the exact faults can be detected. Thus, for logic block diagnosis an xor operation is implemented inside the used logic blocks along with compactor.

III. PROPOSED BISD METHOD AND ITS POWER OPTIMIZATION

Logical BIST is a design for testability technique in which a portion of a circuit on a chip ,board or system is used to test the digital logic circuit itself It is increasingly being adopted to improve test quality and reduce test costs for rapidly growing designs.

A BIST approach able to detect and accurately diagnose all multiple faulty programmable logic blocks(PLBs) in field programmable gate array(FPGA) with maximum diagnostic resolution.

A. Detection Of Various Faults:

1.*wire-open fault*:

A disconnection occurs on any wires in the global interconnect. An open fault is a fault that can be detected when the break is occurred on a single wire on a net. Since an open fault can behave either as stuck-at-1 or stuck-at-0 faults, it is required to test for both stuck-at faults to guarantee the detection of open faults.

2.*wire Stuck-at-fault*:

A stuck-at-fault is a particular fault model used by fault simulators and automatic test pattern Generation(ATPG) tools to mimic a manufacturing defect within a integrated circuit.

3.*wire-Short fault*:

A bridge occurs between two wires in the global interconnect. This fault can be detected in BISD using Output response analyzer(ORA) technique.

4. *Wire Stuck-On Fault*:

PIP-PS stuck-on fault*:* The pass transistor of a non-connectable PIP-PS is turned on in the local interconnect..

MUX-PS stuck-on fault: One of the pass transistors of a non selective MUX-PS is turned on in the local interconnect.

5.*Wire Stuck-Off Fault:*

PIP-PS stuck-off fault: The pass transistor of a connectable PIP-PS is turned off in the local interconnect..

MUX-PS stuck-off fault: One of the pass transistors of a selective MUX-PS is turned off in the local

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interconnect. Wire stuck on and stuck off faults can be detected in interconnect diagnosis.

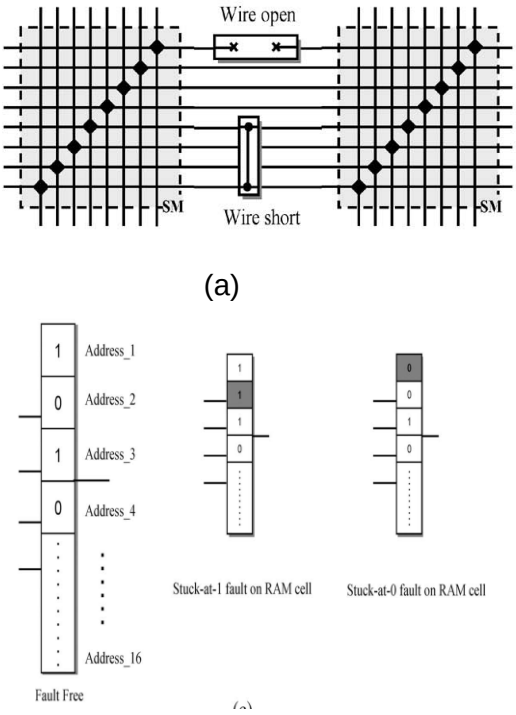

Fig.2.a) Open/short faults in the global interconnects.
b) Stuck-at-0/1 faults on a RAM cell in an LUT.

B.LFSR Technique in BIST:

LFSRs are more popular because of their compact and simple design. Different structure of LFSR (Linear feedback shift Register) will generate different sequence of test pattern. It means that if the BIST time is limited, structure of LFSR will affect the BIST time and fault coverage of CUT(circuit under test).

Here ,LFSR technique is implemented in Logic block diagnosis where it is given as inputs, and the output can be obtained using pass/fail checker and it is compared with the fault dictionary to detect faults.

IV.OUTPUT RESPONSE ANALYZER

A Comparator which sets the pass/fail flip-flop to '1' if the output of both sets do not agree(XOR). In FPGA, testing can be done for both interconnect and logic blocks. By testing them separately, area and power reduction is more. So, to reduce the test timing and also the area, output response analyzer (ORA) is used. In this output response analyzer(ORA) the interconnect and logic blocks can be put together under built in self test(BIST).

Inputs are given under built under test(BUT),using that open fault, short fault, stuck fault can be diagnosed. short, open and stuck on and off fault can be diagnosed using pass/fail checker.

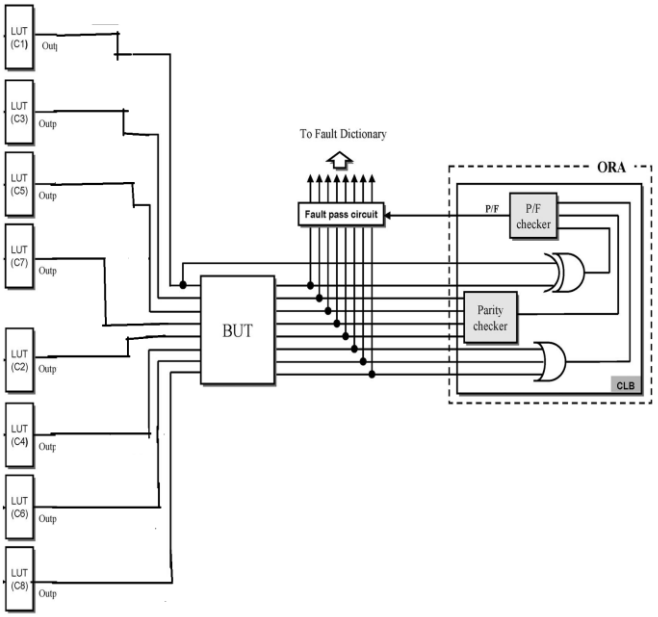

Fig. 3. Schematic of a BIST structure in a test block.

Stuck-at-0 and Stuck at-1 fault can be diagnosed using parity checker. An LFSR technique is implemented in logic block diagnosis(i.e., XOR tree).This all together can be done in the output response analyzer(ORA) and finally combined with the fault dictionary to accurately detect the faults.

A. Error indication:

In order to develop a fault detection structure, the predicted pass/fail checker can be compared with the actual fault in the fault dictionary in order to obtain the error indication in output response analyzer(ORA). By analyzing both the interconnect and logic blocks using LFSR technique, the error indication of the Output response analyzer(ORA) is obtained.

V. RESULTS AND DISCUSSION

A. Interconnect diagnosis results

First the results for interconnect diagnosis is shown where open fault is injected in LUT 1 then ,next shows the logic block diagnosis where stuck at 1 and stuck at 0 fault can be tested. ISIM from Xilinx is used as the simulation tool.. The target device used is Spartan 3E.In interconnect diagnosis, the configuration of used logic blocks is modified, and the configuration of the interconnects remains unchanged. Finally, the Parameter Analysis report and the error coverage has been calculated from the obtained results.

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B. *Logic Block Results*:

Fig.5.a)Simulation Results for Interconnect Diagnosis

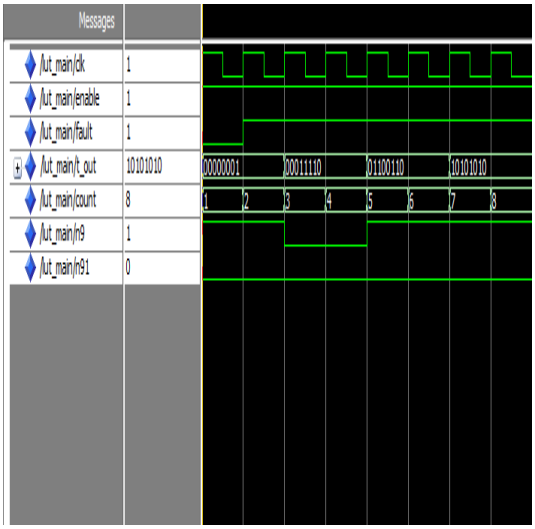
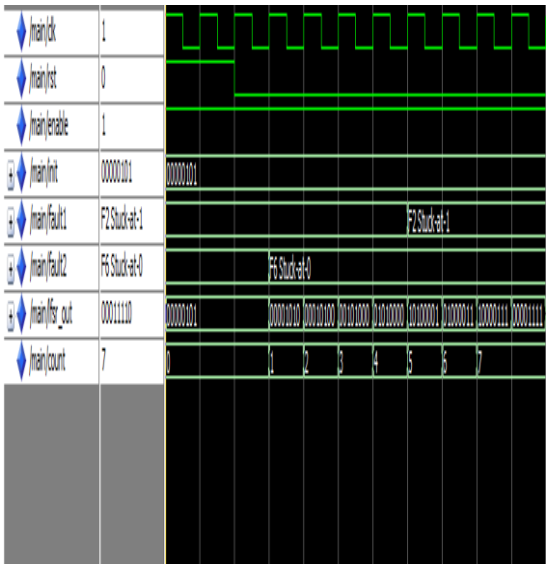


Fig.5.b) Simulation Results for Logic Block Diagnosis



In logic block diagnosis, LFSR is used to generate the test patterns .Fault dictionary is created by activating test patterns of entire FPGA. Then, the initial LFSR value is given as 00000101 and this LFSR initial undergoes ex-or operation at the next stage and produces 4 bit output. This output is compared with the fault dictionary that is assumed and produces the fault.

Here in this simulation, stuck-at-fault is detected at 6th and 2nd pattern. Thus, multiple faults can be detected in Logic block using Application dependent method.

C.Output Response Analyzer Results

Using output response analyzer, both the Interconnect and logic block can be put together in a BIST and the output response can be obtained. The interconnect faults can be detected using pass/fail checker and the logic faults can be detected using parity predictor. The results that are obtained can be combined with the Fault dictionary to detect the accurate faults.

Fig.5.c)Simulation Results for Response analyzer output Diagnosis

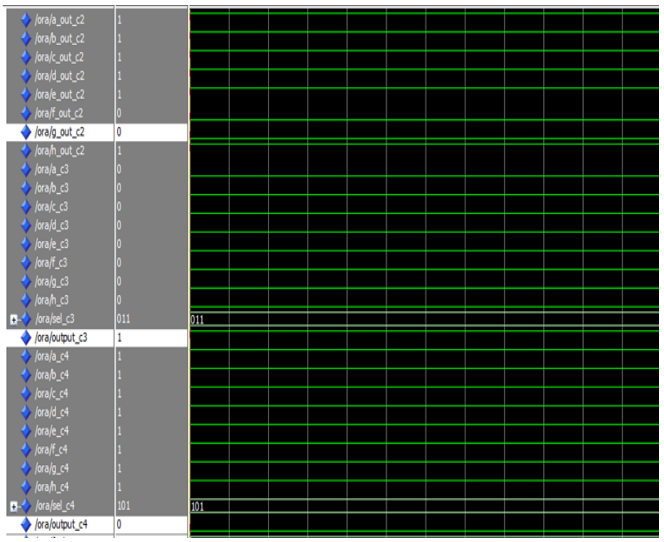


TABLE I

PARAMETER ANALYSIS REPORT

LOGIC UTILIZATION	INTERCONNECT DIAGNOSIS	LOGIC DIAGNOSIS
No .of Gate counts	68	43
Delay	4.86ns	1.82ns
Power	1.007mw	0.030mw

D. Fault Detection

The proposed architecture for the Interconnect and Logic block is able to find all the single Struck-At faults as well as multiple faults. Faults are injected randomly on the input and output nodes of the output response analyser. In the case of multiple Struck-At faults in output response analyser (ORA), 50 multiple SA faults have been injected and 49 faults have been identified. So, the total error coverage faults in the output response analyser has been identified in interconnect and Logic block is identified as 98% and 96%. Thus the error coverage can be detected at the maximum and faults can be detected

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easily in FPGA to improve its precision and quality. The error coverage is given in table V.

TABLE II

ERROR COVERAGE

Faults	Error Coverage
Single SA fault in Interconnect	100%
Multiple SA fault in Interconnect	98%
Single SA fault in Logic block	100%
Multiple SA fault in the Logic block	96%

From the above simulation results, it has been found that the error coverage is approximately 97%. The total area cost of the proposed fault detection scheme in the Output response analyzer (ORA) is much less than the scheme based on interconnect and logic block in separate manner . Also, low power is achieved in the proposed method and also the test time can be minimised more.

V. CONCLUSION

In the proposed method, faults are detected using output response analyser(ORA).i.e., interconnect fault and Logic block fault in FPGA can be obtained together using Output response analyser(ORA).Thus, high fault coverage can be obtained as 98% through this proposed method. Also Low power and less area can be achieved through this Output Response Analyser(ORA) technique.

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