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Radix-4 Encoder & PPG Block for Multiplier Architecture using GDI Technique

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***Abstract*— A radix-4 encoder & partial product generator circuit is implemented that demand high speed and low energy operation. It is a good approach if we implement the multiplier as a hybrid architecture of the radix-4/-8 because the radix-8 mode has low power consumption capability, occupying less area and number of partial products obtained in this mode are less(N/3). But the detection of the 3B term while computing the partial products is very difficult and it is difficult to implement it on the FPGA board. So by comparing the performances of the two multipliers we suggest to go with the radix-4 multiplier. Compared to a conventional CMOS radix-4 encoder & PPG, the proposed circuit consumes 2.23% less power, 17.51% less average delay time with the use of only 74 transistors in comparison to conventional CMOS circuit which uses 204 transistors.**

Index Terms - encoder, multiplier,* gate-diffusion input (GDI), *power consumption, PPG

I. INTRODUCTION

Multipliers are essential components in signal-processing for multimedia applications. While many previous works focused on implementing high-speed multipliers, recently there have been many attempts to reduce power consumption [1]. This is due to the increased demand for portable multimedia applications which require low power consumption as well as high speed operation.

However low-power multipliers without any consideration for high-speed are not the appropriate solutions of low-energy embedded signal processing for multimedia applications [2] [4].
Previously, a hybrid radix-4/-8 modified Booth encoded (MBE) multiplier was proposed for low-power and high-speed operation [2] [10]. It is a good approach if we implement the multiplier as a hybrid architecture of the radix-4/-8 because the radix-8 mode has low power consumption capability, occupying less area and number of partial products obtained in this mode are less(N/3) compared to the partial products of the radix-4 mode(N/2). But the detection of the 3B term while computing the partial products is very difficult and it is difficult to implement it on the FPGA board.

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So by comparing the performances of the two multipliers we suggest to go with the radix-4 multiplier and the Radix-4 encoder with the partial product generation block is implemented here.

The paper is organized as follows. Section II introduces radix-4 encoder. Section III introduces radix-4 partial product generation block. In section IV we can see radix-4 encoder & PPG architecture. Section V introduces GDI circuit methodology. In Section VI, introduces proposed radix-4 encoder & PPG architecture. Implementation results are summarized in Section VII. Finally, conclusion of this paper is made in Section VIII.

II. RADIX-4 ENCODER BLOCK

Radix-4 multiplication obtains an improvement in the multiplication algorithm due to the less number of partial products entering the Wallace tree to be reduced. This can be achieved by the application of the multiplier recoding, changing from a 2's complement format to a signed-digit representation from the set {0, ±1, ±2}.
Now let us assume that we are giving a triplet of multiplier one at a time in the form of xi-1, xi, xi+1 and gets the encoded output in the form of x, x_2, m_i. In which 'x' means that the multiplicand is not to be doubled, 'x_2' means multiplicand is to be doubled and 'm_i' means neither to be doubled nor to be inverted. Figure 1 shows the block diagram of the radix-4 encoder.

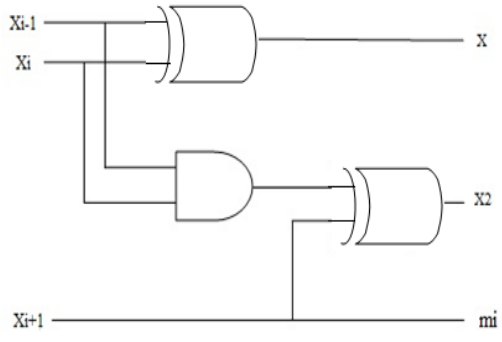

Figure 1. Block diagram of Radix-4 Encoder

III. RADIX-4 PARTIAL PRODUCT GENERATOR BLOCK

In this block, multiplier bits encoded from the encoder and the multiplicand bits get multiplied and the partial products are generated. Figure 2 shows the block diagram

of the partial product generator block where the input x, x_2, m_i are the encoded multiplier bits from the encoder and Y_j and Y_{j-1} are the multiplicand bits which are to be multiplied by the multiplier bits coming from the encoder [11].

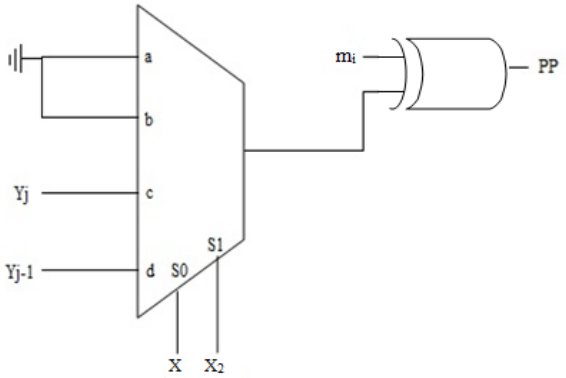

Figure 2. Block diagram of Radix-4 Partial Product Generator

IV. Radix-4 Encoder & PPG Block

In this block, multiplier bits first goes into the encoder, get encoded multiplied be and the multiplicand bits and the partial products are generated. Figure 3 shows the block diagram of the encoder & partial product generator block where the input to the encoder is x_{i-1}, x_i, x_{i+1} and the encoded multiplier bits are x, x_2, m_i. These multiplier bits from the encoder get multiplied by the multiplicand bits Y_i and Y_{i-1} and the partial products are obtained.

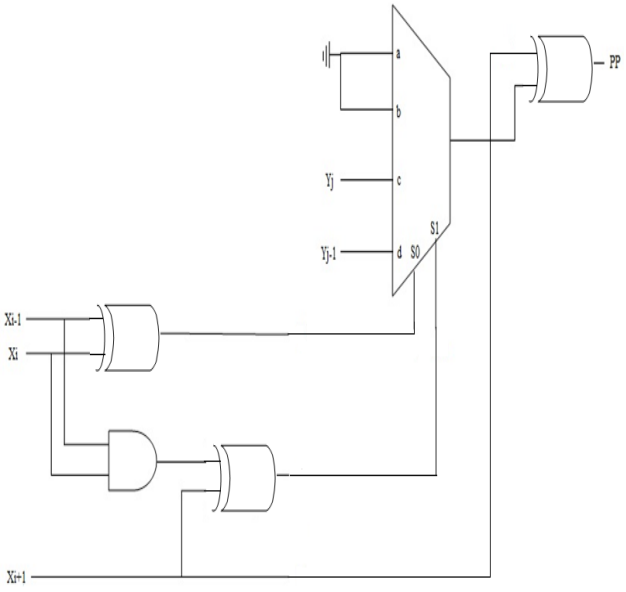

Figure 3. Block diagram of Radix-4 Encoder & PPG

V. GDI Circuit Methodology

The GDI method [6]–[7] is based on the simple cell shown in Figure 4. At a first glance the basic cell resembles the standard CMOS inverter, but there are some important differences. The GDI cell contains four terminals – G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N, and D may be used as either input or output ports, depending on the circuit structure.

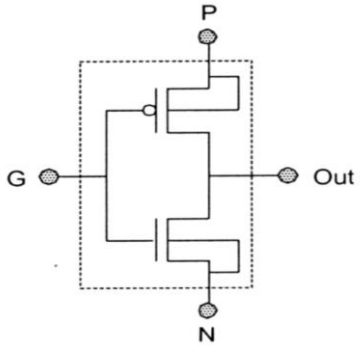

Figure 4. GDI basic cell

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics. Multiple-input gates can be implemented by combining several GDI cells.

TABLE 1
Logic functions that can be implemented with a single GDI cell

N	P	G	D	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table I shows an example of how simple configuration changes of the inputs P, N, and G in the basic GDI cell correspond to very different Boolean functions at the output D.

Most of these functions require a complex (6- 12 transistors) gate in CMOS (as well as in standard PTL implementations [8]), but are very simple (only two transistors per function) in the GDI design methodology.

VI. Pooposed Radix-4 Encoder & PPG Architecture

All the used sub-circuits used to make the radix-4 encoder are being implemented using CMOS style & GDI technique. The transistor count for the conventional CMOS encoder is 34 whereas with GDI technique it is 10 transistors. Schematic of encoder is shown in Figure 5.

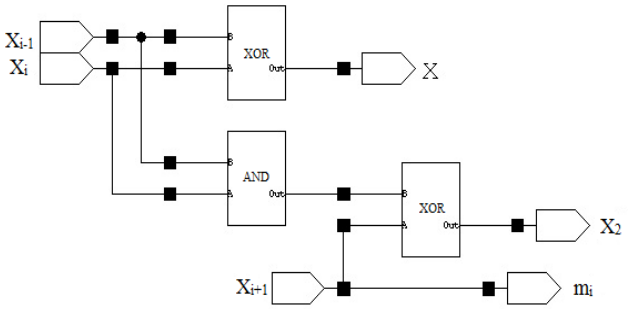

Figure 5. Schematic of Radix-4 Encoder

All the used sub-circuits used to make the radix-4 PPG are being implemented using CMOS style & GDI technique. The transistor count for the conventional CMOS PPG is 50 whereas with GDI technique it is 10 transistors. Schematic of PPG is shown in Figure 6.

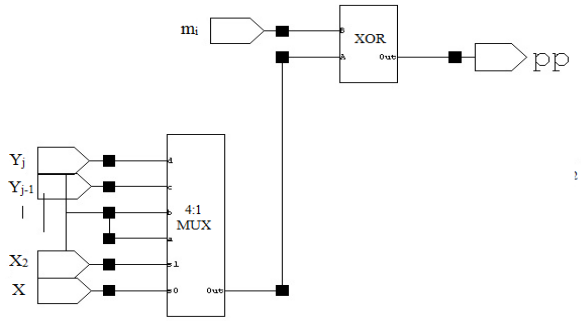

Figure 6. Schematic of Radix-4 PPG

The circuit as shown in Figure 7(a) is a Radix-4 encoder & partial product generator schematic.. All the used sub-circuits used to make the radix-4 encoder & partial product generator architecture are being implemented using CMOS style and GDI technique.

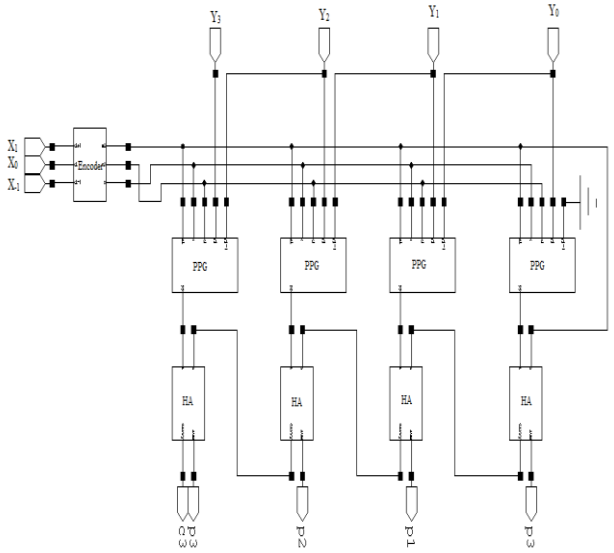

Figure 7 (a) Schematic of encoder & PPG

The transistor count for the conventional CMOS encoder & partial product generator is 204. Its area is large as a result it is more complicated, consumes more power and has slow speed. Whereas, transistors count for the GDI encoder & partial product generator is 74. Schematic and output waveform of encoder & partial product generator is shown in Figure 7(a) & Figure 7(b) respectively.

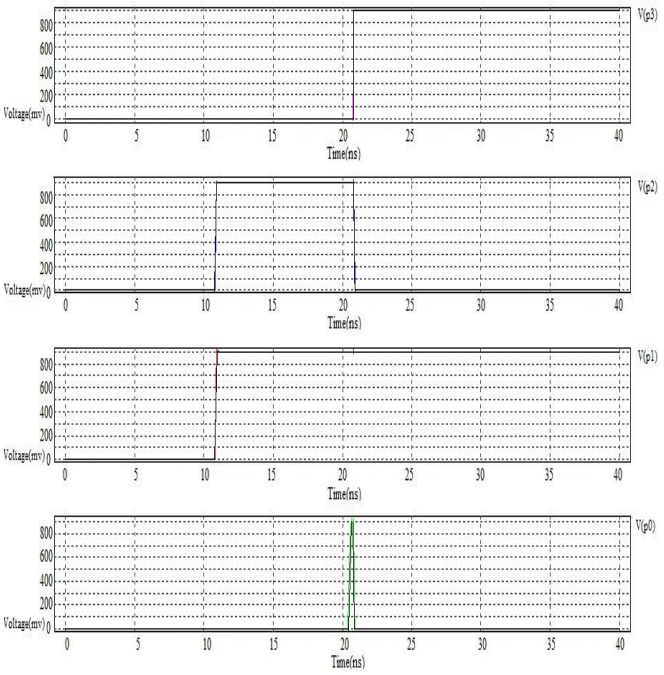

Figure 7 (b) Waveforms of CMOS dual encoder

VII. Experimental Result

Table II & III shows implementation results including the proposed encoder's hardware area, critical path delay, and power consumption compared to previous work. The multiplication of power and propagation delay means energy. [1] [3] [5]. It has been observed that Power consumption is higher at 1.2v with less speed and lower at 0.9v with higher speed. The proposed GDI radix-4 encoder & PPG architecture consumes less power and less delay time compared to previous work [2] [10].

Table II and Table III show comparison between CMOS & GDI encoder & PPG at 0.9v & 1.2v respectively.

TABLE II Power, Delay & Transistor count of CMOS & GDI Encoder & PP generator

At 0.9 v	CMOS Encoder & PPG	GDI Encoder & PPG
Power(watt)	6.4210×10^{-6}	4.2435×10^{-6}
Delay(sec)	1.2354×10^{-9}	1.1255×10^{-9}
Transistor Count	204	74

TABLE III Power, Delay & Transistor count of CMOS & GDI Encoder & PP generator

At 1.2 v	CMOS Encoder & PPG	GDI Encoder & PPG
Power(watt)	1.4140×10^{-5}	1.3824×10^{-5}
Delay(sec)	8.3247×10^{-10}	6.8655×10^{-10}
Transistor Count	204	74

VIII. CONCLUSION

Simulation of this circuit is being done on Tanner EDA 13.0v Tool at 90nm technology and find out the following results.

A GDI radix-4 encoder & PPG architecture which is proposed in this paper is an appropriate solution for multiplier because it is both low-power and high-speed and less area. Compared to a conventional CMOS radix-4 encoder & PPG, the proposed circuit consumes 2.23% less power, 17.51% less average delay time with the use of only 74 transistors in comparison to conventional CMOS circuit which uses 204 transistors.

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