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# ARCHITECTURE OF 4-BIT PIPELINE ADC IN CMOS TECHNOLOGY

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*Abstract*- **Analog-to-digital converters (ADCs) are key design blocks and are currently adopted in many application fields to improve digital systems, which achieve superior performances with respect to analog solutions. With the fast advancement of CMOS fabrication technology, more and more signal-processing functions are implemented in the digital domain for a lower cost, lower power consumption, higher yield, and higher re-configurability. Wide spread usage confers great importance to the design activities, which nowadays largely contributes to the production cost in integrated circuit devices (ICs). This has recently generated a great demand for low-power, low-voltage ADCs that can be realized in a mainstream deep-submicron CMOS technology. Various examples of ADC applications can be found in data acquisition systems, measurement systems and digital communication systems also imaging, instrumentation systems. Hence, we have to considered all the parameters and improving the associated performance may significantly reduce the industrial cost of an ADC manufacturing process and improved the resolution and design specially power consumption . This paper presents a 4 bit Pipeline ADC with low power dissipation implemented in <0.18µm CMOS technology with a power supply of 1V.**

## I. INTRODUCTION

As IC fabrication technology has advanced, more analog signal processing functions have been replaced by digital blocks ,analog-to-digital converters (ADCs) retain an important role in most modern electronic systems because most signals of interest are analog in nature and must to be converted to digital signals for further signal processing in the digital domain.

There is wide variety of different ADC architectures available depending on the requirements of the application. Pipeline ADCs are one of the best examples. Pipeline analog–to-digital converters (Pipeline ADC) have recently become very attractive in energy efficient moderate-resolution/moderate-speed applications due to their minimal active analog circuit requirements. It typically generate one bit per clock cycle, the benefits are the low area needed for the implementation. ADCs of this type have good resolutions and quite wide ranges. By combining the merits of the successive approximation and flash ADCs this type is fast, has a high resolution, and only requires a small die size.

The pipeline analog-to-digital converter (ADC) is a promising topology for high-speed data conversion with compact area and efficient power dissipation. Its speed of operation far surpasses that of serial-based structures, such as successive approximation or cyclic converters, while its die area and power dissipation favorably compare to that of flash and other more parallelized architectures. Pipelined ADCs are widely used in the areas of wireless communications, digital subscriber line analog front ends, CCD imaging digitizers, studio cameras, ultrasound monitors, and many other high speed applications.

Pipeline analog-to-digital converters ($ADC_S$) represent the majority of the ADC market for medium-to high-resolution $ADC_S$. Pipeline $ADC_S$ provide up to 5Msps sampling rates with resolutions from 8 to 18 bits. The Pipeline ADC architecture allows for high performance, low power $ADC_S$ to be packaged in small form factors for today's applications. With ADC we have designed 4 bit low power high speed Pipeline ADC with 0.18µm technology.

## II. REWIEW OF WORK

The first documented example of an ADC was a 5-bit, electro-optical and mechanical flash-type converter patented by Paul Rainey in 1921, used to transmit facsimile over telegraph lines with 5-bit pulse-coded modulation (PCM). The first all-electrical implementation came in 1937 by Alec Harvey Reeves, this also had a 5-bit resolution and the ADC was implemented by converting the input signal to a train of pulses which was counted to generate the binary output at a sample rate of 6 kS/s. Following this the successive approximation ADC was developed in 1948 by Black, Edson Goodall to digitize voice to 5-bits at 8 kS/s. Also in 1948, a 96 kS/s, 7-bit ADC was developed and it was developed and it was implemented using an electron beam with a sensor placed on the other side of a mask. The mask had holes patterned according to the binary weights so that all bits were simultaneously detected, the pattern also employed Gray coding of the output in order to reduce the effect of errors in the most significant bit (MSB) transition, much as is done in modern high-speed flash $ADC_S$[12].

Following the development of the transistor in 1947 and the integrated circuit in1947 and the integrated circuit in 1958, the ADC development continued in the 1960's with for example an 8-bit, 10 MS/s converter that was used in missile-

defence programs in the United States. During the same decade, all the currently used high-speed architectures were developed including Pipeline $ADC_S$ with error correction. Commercial flash converters appeared in instruments and modules of the $1960_S$ and $1970_S$ and quickly migrated to integrated circuits during the $1980_S$. The monolithic 8-bit flash ADC became an industry standard in digital video applications of the $1980_S$. Today, the flash converter is primarily used as a building block within subranging "pipeline"[9]. Using Partial amplifier sharing topology, a 6-bit pipeline ADC, developed in 0.35µm CMOS process. A 6-bit, 2.5 V flash ADC design has been reported new flash topology and this new topology has only 2(N-2) + 2 comparators required. Here area of the chip is large and it's required to minimize it [10]. The AD7880 is a high speed, low power, 12-bit A/D converter which operates from a single +5V supply.

First commercial converter, 1954 "DATRAC" 11-Bit, 50-kSPS SAR ADC Designed by Bernard M. Gordon at EPSCO. In the recent years there has been a trend in ADC research to use low accuracy analog components which are compensated for through the use of digital error correction. Because of their popularity, successive approximation ADCs are available in a wide variety of resolutions, sampling rates, input and output options, package styles, and costs. Many SAR ADCs now offer on-chip input multiplexers, making them the ideal choice for multichannel data acquisition system. An example of modern charge redistribution successive approximation ADCs is Analog Devices' PulSAR® series. TheAD7641 is a 18-bit, 2-MSPS, fully differential, ADC that operates from a single 2.5 V power supply. The part contains a high-speed 18-bit sampling ADC, an internal conversion clock, error correction circuits, internal reference, and both serial and parallel system interface ports. The AD7641 is hardware factory calibrated and comprehensively tested to ensure such ac parameters as signal-to-noise ratio (SNR) and total harmonic distortion (THD), in addition to the more traditional dc parameters of gain, offset, and linearity.

The motivation behind this is that analog design have not been able to benefit from process scaling in the same way as digital logic and therefore the relatively area-cheap digital logic is used to compensate for the shortcomings of expensive analog circuits. For device reliability reasons, the supply voltage needs to be reduced to ensure gate oxide integrity over time and prevent p-n junction from breakdown. Present-day CMOS processes are making the transition from 3.3 V to 1.8 V supplies. The converter should operate with high sampling rate from an operating supply as low as possible, to facilitate integration with low-voltage, power efficient digital circuits.

## III. PIPELINE ADC DESIGN

The pipeline ADC architecture combines the benefits of high throughput and an input capacitance bound by noise constraints. Typical pipeline architecture is illustrated in Figure 3.1.

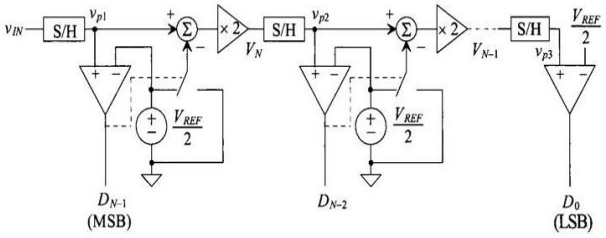


Fig 3.1 Pipeline A/D converter

The pipeline ADC is an N-step converter, with 1 bit being converted per stage. Able to achieve high resolution (10-13 bits) at relatively fast speeds, the pipeline ADC consists of N stages connected in series (Fig.). Each stage contains a 1-bit ADC (a comparator), a summer, multiplier, mux, buffer and a Transmission Gate (S/H).Each stage of the converter performs the following operation:

1. After the input signal has been sampled, compare it to vref/2. The output of each comparator is the bit conversion for that stage.

2. If vm > vref/2 (comparator output is 1), vref/2 is subtracted from the held signal and pass the result to the amplifier. If vIN < vref/2 (comparator output is 0), then pass the original input signal to the amplifier. The output of each stage in the converter is referred to as the residue.

3. Multiply the result of the summation by 2 and pass the result to the sample and- hold of the next stage.

A main advantage of the pipeline converter is its high throughput. After an initial latency of N clock cycles, one conversion will be completed per clock cycle. While the residue of the first stage is being operated on by the second stage, the first stage is free to operate on the next samples. Each stage operates on the residue passed down from the previous stage, thereby allowing for fast conversions. The disadvantage is having the initial N clock cycle delay before the first digital output appears. The severity of this disadvantage depends, of course, on the application. One interesting aspect of this converter is its dependency on the most significant stages for accuracy. A slight error in the first stage propagates through the converter and results in a much larger error at the end of the conversion. Each succeeding stage requires less accuracy than the one before, so special care must be taken when considering the first several stages.

The Pipelined ADC can be thought of as an amplitude-interleaved topology where errors from one stage are correlated with errors from previous stage. The basic block diagram implementation of an N-bit Pipelined ADC using the cyclic stages is as shown in Figure 3.2.

Instead of cycling the analog output of the 1 bit/stage section back to its input, we feed the output into next stage. The stages are clocked with opposite phases of the master clock signal. The comparator outputs are labelled digital in figure.

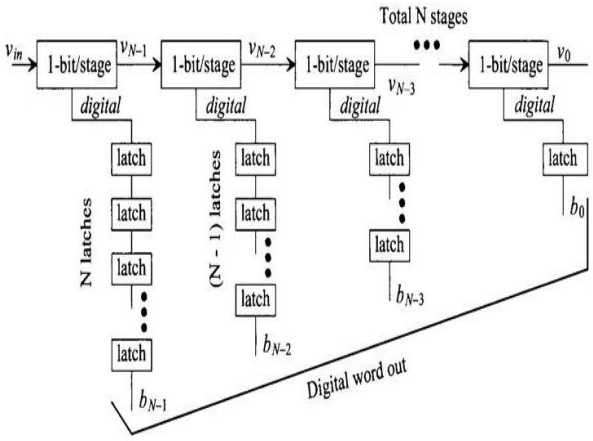


Fig 3.2. Pipeline ADC based on cyclic stages

The digital comparator outputs are delayed through latches so that the final digital output word corresponds to the input signal sampled N clock cycles earlier. The first stage in figure must be N-bit accurate. It must amplify its analog output voltage, VN-1 to within 1 LSB of the ideal value. The second stage output, VN-2 must be an analog voltage within 2 LSB of its ideal value. The third stage output, VN-3 must be an analog voltage within 4 LSB of its ideal value.

Each stage of the 4-bit Pipeline ADC has the following elements i.e.

- Comparator
- Transmission gate.
- multiplexer
- A summer
- Multiplier

### A. Comparator

An operational amplifier (op-amp) has a well balanced difference input and very high gain. This parallels the characteristics of comparators and can be substituted in applications with low- performance requirements.

In theory, a standard op-amp operating in open- loop configuration (without negative feedback) may be used as a low–performance comparator. When the non-inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage. When the non-inverting input (V+) drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split-voltage power supply, (powered by ± Vs) its transfer function is typically written as: $V_{out} = A_0 (V1 - V2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open-loop (no negative feedback).

If there is a fixed voltage source from, for example, a DC adjustable device in the signal path, a comparator is just the equivalent of a cascade of amplifiers. When the voltages are nearly equal, the output voltage will not fall into one of the logic levels, thus analog signals will enter the digital domain with unpredictable results. To make this range as small as possible, the amplifier cascade is high gain. The circuit consists of mainly bipolar transistor except perhaps in the beginning stage which will likely to field effect transistor. For very high frequencies, the input impedance of the stage is low. This reduces the saturation of the slow, large P-N junction bipolar transistors that would otherwise lead to long recovery times. Fast small schotkey diode, like those found in binary logic designs, improve the performance significantly though the performance still lags that of circuits with amplifiers using analog signals.

In order to precisely slice input data, a reference voltage may be transmitted, on a different signal path, along with the data. Alternatively, the data may be transmitted differentially (an input and its complement). In either case a differential amplifier is needed. A differential amplifier input buffer (which we will supply call an input buffer from this point on) amplifies the difference between the two inputs. In a simplest case one input to the input buffer is a DC voltage, say 0.5 V (Vinm) in fig 5.11. When the other input (Vinp) goes above 0.5V, the input of the buffer changes states (goes from low to a high) or

Vinp > Vinm =.> 1
Vinp < Vinm = > 0

**Design of Comparator**

We have designed comparator to design the Pipeline architecture shown in fig 3.3 where the core plot of the block named as comparator is shown in fig 3.4. For different ranges of voltages we have used both N and P type comparator and output is common for high speed cascading of two stages is used in comparator. Due to mismatch of MOS device there is offset voltage present and to avoid it we have used Vdc offset voltage of 40 mv in our design so we got the accurate simulation results shown in fig 3.5.

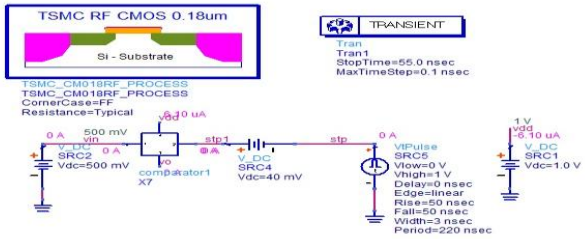


Fig 3.3 Design of Comparator

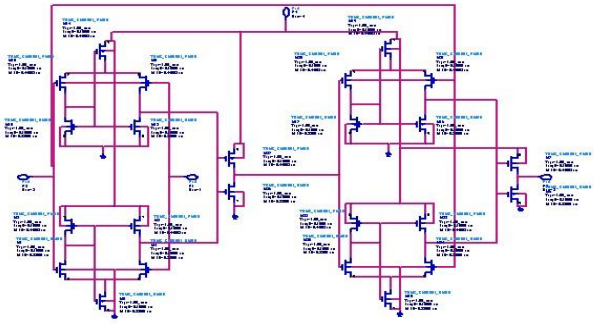

Fig 3.4 Comparator's Circuit

**Simulation Results**

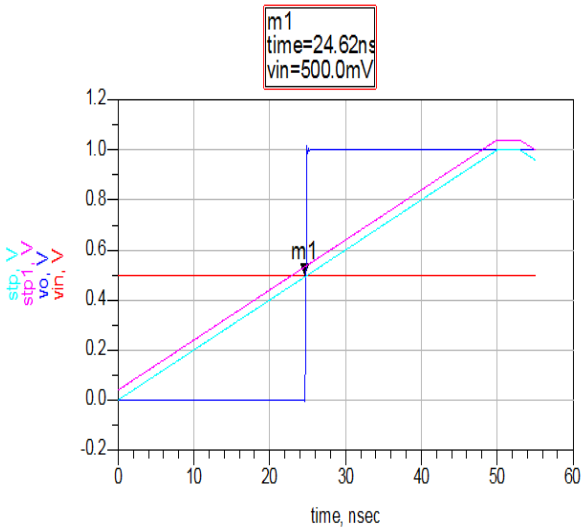


Fig 3.5 Simulation Results for Comparator

## B. Transmission Gate

The transmission gate (TG) is used in digital CMOS circuit design to pass or not pass a signal. Transmission Gate acts as sample and hold circuit. The gate is made up of parallel connection of an NMOS and a PMOS device. Referring to the figure 3.6. When S is high, transmission gate passes the signal on the input to the output (nothing the nodes we define as the input or output are interchangeable) [1]. The resistance between the input and the output can be estimated as Rn || Rp. Since the NMOS pass gate (PG) passes logic lows well and the PMOS PG passes logic highs well, putting the two complementary MOSFETs in parallel, produces a TG that passes both logic level well. Propagation delay- times of the CMOS TG are estimated as, $t_{PHL} = t_{PLH} = 0.7$ (Rn || Rp).C load

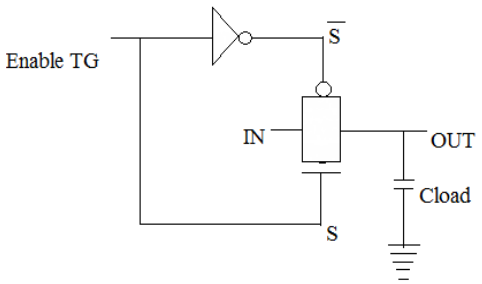


Fig 3.6 Transmission Gate

The capacitance on the S input of the TG is the input capacitance of the NMOS device. The capacitance on the input of the TG is the input of the TG is the input capacitance of the PMOS device. Increasing the widths of the MOSFETs used in the TG reduces the propagation delay times from the input to the output of the TG when driving specific load capacitance.

We have designed transmission gate shown in fig 3.7and we got the simulation results shown in fig 3.8. As transmission gate pass or not pass the signal depend on control input, in simulation results when clock (control input) is high, input is transferred and when clock is low input is not transferred.

**Design of Transmission Gate**

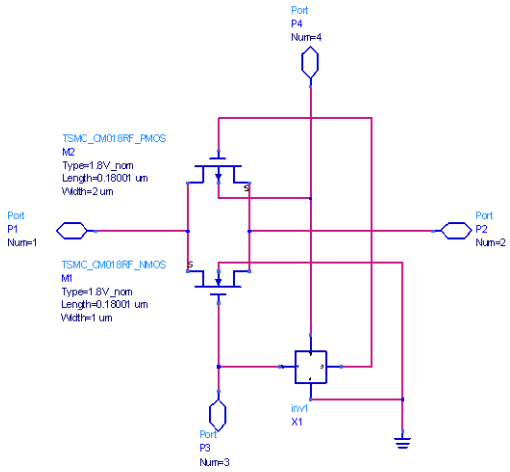


Fig 3.7 Design of Transmission Gate

**Simulation Results**

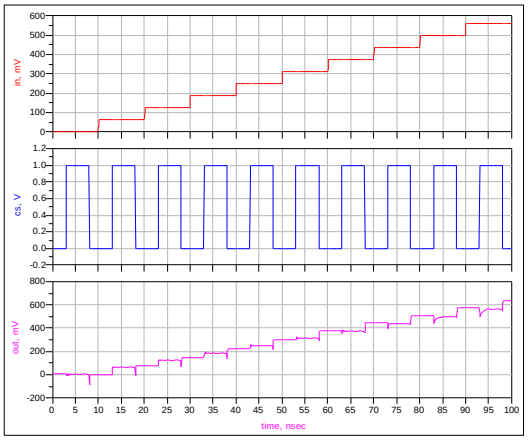


Fig 3.8 Simulation Results of Transmission Gate

Application of the Transmission Gate

Path Selector

Circuit shown in figure 3.9 is a two – input path selector. Logically, the output of the circuit can be written as

Z=AS+BS

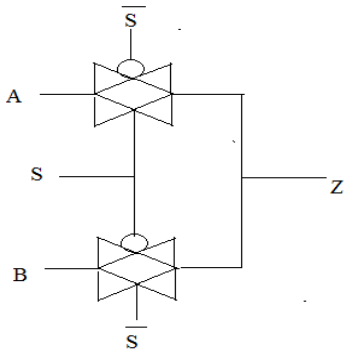


Fig 3.9 Path Selector

When the selector signal S is high, A is passed to the output while a low on S passes B to the output.

### C. MULTIPLEXER

This same idea can be used to implement multiplexer / demultiplexers. Block diagram is shown in Fig 3.10. The number of control lines is related to the number of input lines by

$$2^m = n$$

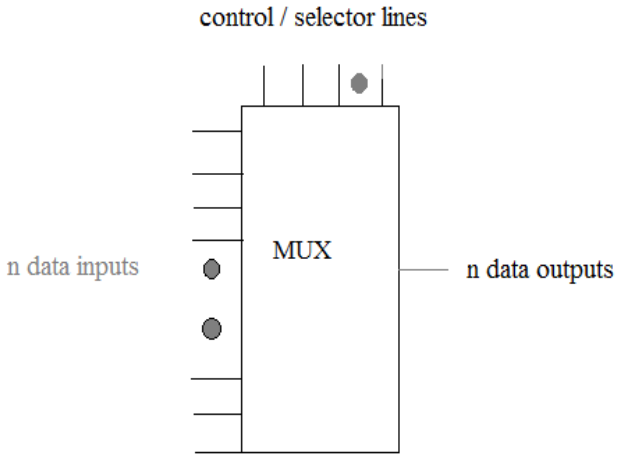


Fig 3.10 MUX

Where n is the number of inputs (outputs) to the MUX (DEMUX) and m is the number of control lines. A 4 to 1 MUX is shown in Fig 3.10. Note that Mux is Bidirectional that is it can be used as MUX or DEMUX [1]. We have designed Analog MUX shown in fig 3.11 where two transmission gates are connected in parallel and we got Simulation Results shown in Fig 3.12. Where when clock is high first signal get transferred and when it is low second signal get transferred.

**Design of Analog MUX**

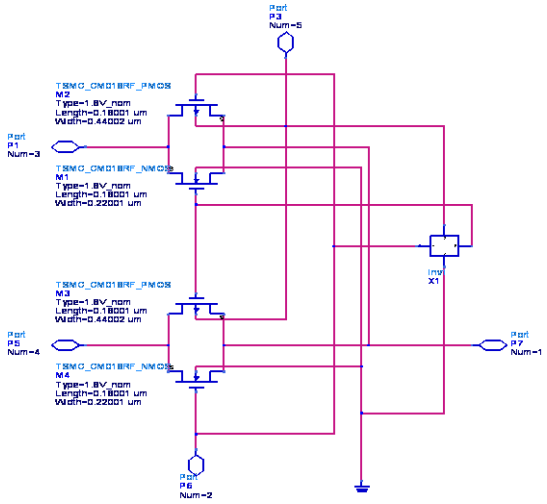

Fig 3.11 Design of Analog MUX

**Simulation Results**

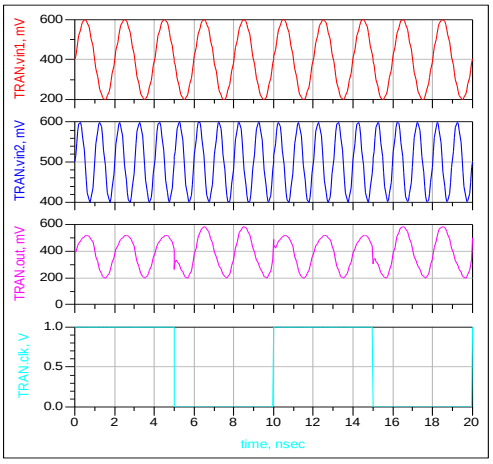


Fig 3.12 Simulation Results of Analog MUX

**Power dissipation in ADC**

Power dissipation in CMOS logic arises from following

1) Switching current from charging and discharging parasitic capacitance.
2) Short circuit current when both N & P channel transistors are momentarily on at the same time.
3) Leakage current & subthreshold current.

Average dynamic power dissipated is given by :-

$$Pavg = Ctot * VDD^2 * Fclk$$

Notice that power dissipation is a function of clock frequency. A great deal of effort is put into reducing the Power dissipation in CMOS circuits.

Together with the scaling of process geometry, the supply voltage (squared term) is reduced in order to both reduce the digital Power dissipation and the rate of device

degradation. Also we have to reduce short circuit current, sub threshold current, leakage current.

The basic problems coupled to SC, such as clock feed through from digital part through the switches, capacitor mismatch and op-amp non-idealities, have been taken into account during the design of the ADC. AS we are using 0.18µm technology, supply voltage is 1V. Also due to clock redundancy Power dissipation is reduced.

## IV. CIRCUIT IMPLEMENTATION

With ADS and various designed components we have designed complete Pipeline Architecture shown in fig 4. And we got the simulation results shown in fig 5.

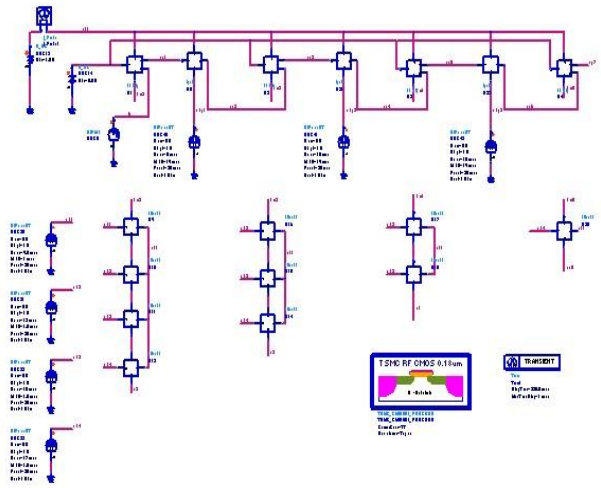

Fig 4 Pipeline Architecture

## V. SIMULATION RESULT

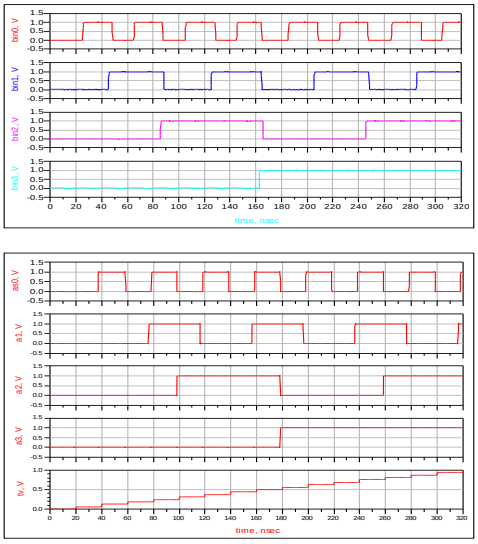

Fig 5 Simulation Results for Pipeline ADC

The ADC is fabricated in 0.18µm standard CMOS process with 4 bit resolution. The value of the unit capacitor is 100fF. The static performance of the ADC is shown in Figure. ADC operates at 1V. The DNL and INL of the ADC are a measurement factor of linearity.

**.Pipeline ADC vs. other ADCs**

Power dissipation of Pipeline ADCs varies with the sampling rate unlike Flash and SAR architectures. Hence find applications in PDAs.

The SAR ADC's are low power consumption, high resolution, and accuracy. In a SAR ADC, increased resolution comes with the increased cost of more-accurate internal components.

Flash ADC is much faster, less accurate and takes more silicon area due to the number of comparators 2N for N bit Resolution.

Oversampled/Σ-J ADCs have low conversion rates, high precision, averaging noise and no requirement for trimming or calibration even up to 16 bits of resolution.

## VI. CONCLUSION

ADC is the key design Block in modern microelectronics digital communication system. With the fast advancement of CMOS fabrication technology and continued proliferation of mixed analog and digital VLSI systems, the need for small sized, low-power and high-speed analog-to-digital converters has increased.

With an increasing trend to a system-on-chip, an ADC has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other digital circuits. So we have proposed low power ADC. The Pipeline ADC is best suitable for low power application. The designed Pipeline ADC is ideal because there are no missing codes, INL is zero and for DNL there is slight difference between Actual step width & Ideal step width.

For designing purpose we have used Advanced Designing System. The Pipeline ADC core is composed by 4 stages. Each stage includes comparator, Transmission Gate, and pipeline control logic; these components have been designed targeting to fulfil several constraints on requirements such as low power dissipation, the offsets due to mismatch. From the results presented we could conclude that conversion is performed without missing codes and a low-power high speed 4-bit Pipeline ADC in a 0.18µm CMOS process with a 1V supply voltage is designed.

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