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A Design of Ultra Low Power and High Speed 64 Bit Error Tolerant Adder for MAC

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***Abstract*— High speed and Low power design of VLSI circuits has been identified as a critical technological need in recent years due to the high demand for portable consumer electronics products. Error-Tolerance is a novel method to enhance the effective yield of IC products.A large, extremely fast digital adder with some control block and carry free addition block is described. Without depending on the conventional design methods, a new method of addition is used.In this method the power dissipation due to carry propagation is greatly reduced unlike other conventional adders. Therefore, it is important to develop computational structures that fit well into the execution model of the processor and are optimized for the current technology. Optimization of the algorithms is performed globally across the critical path of its implementation.In this methodology, 64 bit design of Error Tolerant Adder is implemented and is verified from simulation outputs using CADENCE ENCOUNTER COMPILER. The results show that proposed 64 bit architecture fair better in terms of power and delay compared to previous approaches.**

***Index Terms*—Power Delay Product(PDP),Multiply and Accumulate(MAC),Least Significant Bit(LSB),Most Significant Bit(MSB), Digital Signal Processing (DSP).**

I. INTRODUCTION

To increase the speed of a digital computer, a designer can either develop faster electronic components and circuitry or organize slower components into faster, for more efficient systems. In recent methods, increased speed is obtained by combining available electronic components into more complex logic structures [1,2]. But these structures are rarely used with more subtle algorithms for executing basic operations, often require large amounts of additional equipment.In digital adders, the delay in addition is mainly by the durationneed to propagate a carry through the adder. The each bit position sum in a conventional adder is generated serially only after the previous bit position has been summed and a carry propagated into the next position. Improved adders generate carries simultaneously [3,4]. However, becauseof the inherent limitations in available components, the construction of simultaneous carry-generation adders is not always practical. This paper describes fast and low power digital adders that abruptly reduce the need for carry propagation, without requiring an excessive of additional hardware.

The design of 64 bit ETA is synthesized and compiled to the layout design to get accurate leakage power and dynamic power analysis results.

II. KEY DEFINITIONS

The most commonly used terminologies in ETA are given as follows

A. Overall Error (OE):

The difference between the correct result (R_c) and the result obtained by the adder (R_e). OE=|Rc-R_e|.

B. Accuracy (ACC):

In this ETA design accuracy of adder is used to indicate how "correct" the output for an particular input.
ACC=(1-(OE/R_c))×100% .

C. Minimum Acceptable Accuracy (MAA):

In this ET adder even though some errors are allowed to exist at the output, the accuracy of an acceptable output should be "high enough" to meet the requirement of the particular system. MAA is just a threshold value.

D. Acceptance Probability (AP):

The probability of the accuracy of an adder should be greater than the acceptable accuracy. AP=(ACC>MAA), ranging from 0 to 1.

III. NECESSITY OF ERROR TOLERANT ADDER.

In the modern VLSI design, due to increase in input data sets and the requirement of large and low power needs the adder architecture to be large and high speed response.The conventional ripple-carry adder (RCA), no longer suitable for large addition operation, because of its low speed performance. Other conventional types of fast adders, such as the carry-skip adder (CSK) [10], carry-select adder (CSL) [11], and carry-look-ahead (CLA) [12], are developed.However, they are also consuming more power due to complex structure. The ETA design will be the efficient way to reduce the power abruptly and increase speed.

IV. METHODOLOGY

All the other adder circuit, the delay is mainly due to the carry propagation chain along the critical path, from LSB to the MSB. On the other hand a significant amount of power consumption of an adder is due to the carry propagation[5]. Therefore, if the carry propagation eliminated there will be great achievement in low power and high speed.

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In this ET method we split the input data operands into two parts and the addition operation is carried out in opposite directions at these two parts.One part at the MSB side data inputs are accurate part and the other at the LSB are inaccurate part. As by name, the accurate part havenormal addition operations and the inaccurate part works by proposed method of special addition mechanism. Carry signal is eliminated to minimize the overall critical propagation delays. A special strategy adapted to minimize the error at the inaccurate part, described as 1) check every bit position from MSB to LSB; 2) if both input bits are "0" or different, one-bit addition is performed ; 3) if both input bits are "1", the checking process stopped and from this bit position all the sum bits are set to "1".

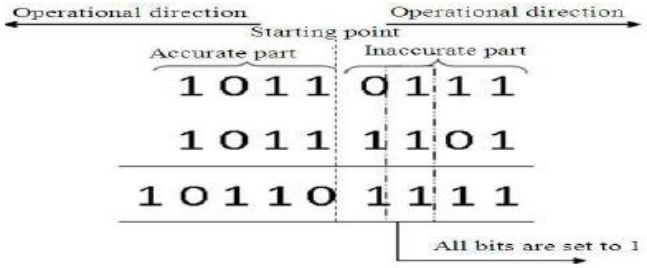

Figure 1:Addition methodology in ETA

V. Design of 64 bit ETA

A. Method of dividing the Adder

In Error Tolerant Adder, the hardware design structure is grouped into two main parts: an accurate part and inaccurate part. The main strategy in dividing the adder depends on the application where and how it going to be used, because the accuracy of the adder will vary by inaccurate part of the adder[6]. If particular application needs the accuracy to be 95%,then the acceptance probability to be around 98%. Here designer divided the adder architecture in the way to get the accuracy at least 98% of all possible input data bits get accuracy more than 95%. Sometimes requirement may not meet the accuracy, that situation the one or two bit position from the inaccurate side is shifted to the opposite accurate part in the adder. Actually in this 64 bit adder architecture having considered the above, 64-bit input data is divided as 24 bits in the accurate part and 40 bits in the inaccurate.

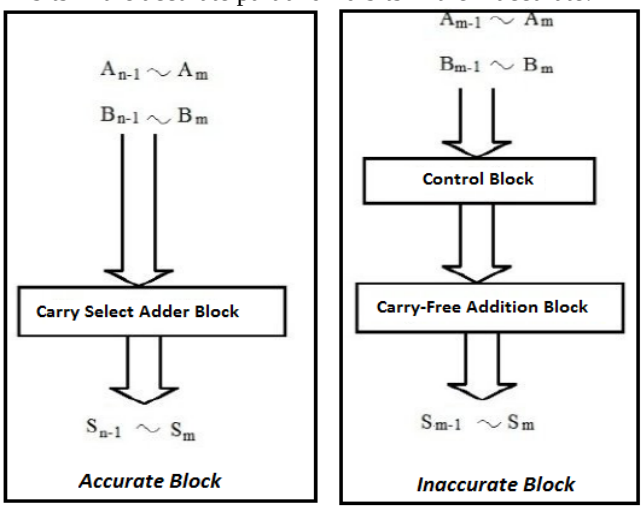

Figure 2: Hardware Implementation of Proposed Adder

B. Design of Accurate part

In this 64-bit ETA[1], the accurate part has 24 bits input data as per the requirement and the addition operation is performed by the conventional adder. The overall speed and performance depend on the inaccurate part and not on the accurate part. So as better option for power saving, ripple carry adder is used and as penalty of speed is given out. But as new idea to increase the speed and to give the additional processing speed to the adder carry select adder is used here.

C. Design of Inaccurate part

The main block in this Error Tolerant adder is the inaccurate part, this part consists of Control block and carry-free addition block.This two blocks in this adder only determines the accuracy, speed performance, and power consumption of the whole adder circuit architecture.

The control block performs the main role in ETA addition operation the function of control block is to detect the first bit position when both input bits are "1", and to set the control signal on this position as well as those on its whole right side. But one complexity is that, each carry free addition bit needs individual control signal and so 40 control signal generating cells (CSGC) were used for inaccurate adder part shown in figure 3. Due to the long chain of 40 cascaded CSGCs, propagation delay may increase as possible as lengthy it is. So the control block is arranged into equal sized groups of five in each group, totally 10 cascaded groups with additional connections between every two neighboring groups by CSGC of type I as shown in figure 4. The beginning part of each group is connected to leftmost cell in the next group by CSGC of type II shown in figure 4.

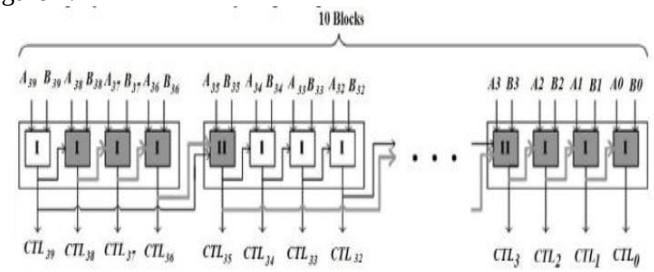

Figure 3: Control Block for first 40 bits

The CSGC II helpto connect the neighbor group to the next group in cascade connection.

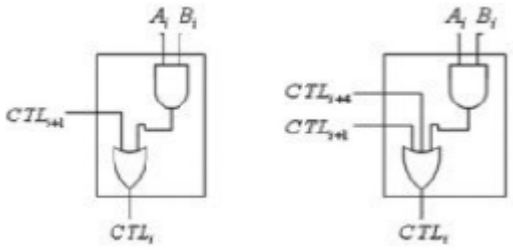

Figure 4: Control signal generating cells of type I & II

This new combination of CSGC will reduce the propagation delay here the dark shaded cells are the critical path of the control block. For example, if sixth CSGC group finds the both input bits '1' then the control signal is made high from this CSGC cell to the rightmost cell, here the delay is reduced hardly by CSGC II. Where the CSGC II in each block helps the control signal from the neighbor block to bypass through separate connections to other CSGC II, so that fast signal processing will happen.

The carry free addition block consists of modified XOR gate, which produce resultant sum by getting the control signal from the control block. Here, 40 modified XOR gates are used shown in figure 5. In this modified XOR gate, three transistors M1, M2 and M3 are added to the conventional XOR gate. The operation mode of the modified XOR gate is decided by the control signal from control block. If CTL=0, then M1 & M2 are turned on, while M3 is turned off, so the circuit will operate in normal mode. When CTL=1, M1 & M2 turned off, while M3 is turned on, sum node is connected to VDD and hence the sum=1.

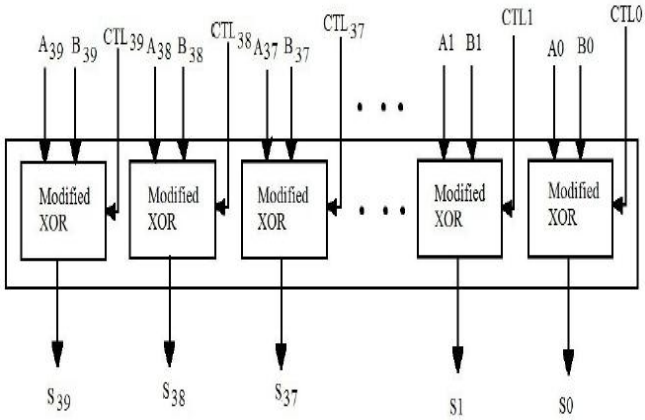

Figure 5: Architecture of Carry Free Addition Block

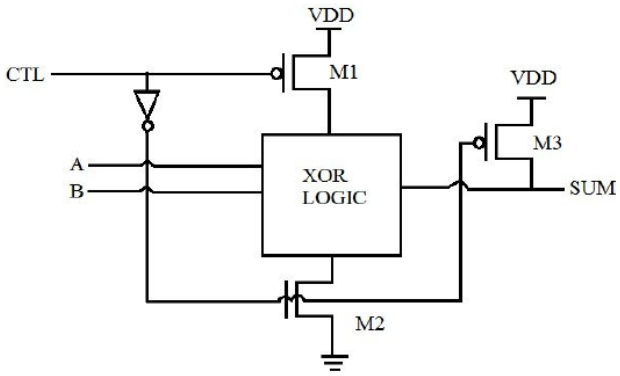

Figure 6: Schematic diagram of XOR gate

VI. Implementation of 64 bit ETA

To prove the effectiveness of the proposed ETA, simulation were done in CADENCE TOOL by Verilog coding and the power consumption, delay and area are measured and also layout of 64 bit architecture is drawn by the CADENCE ENCOUNTER TOOL. All the circuits were implemented using 180nm technology.

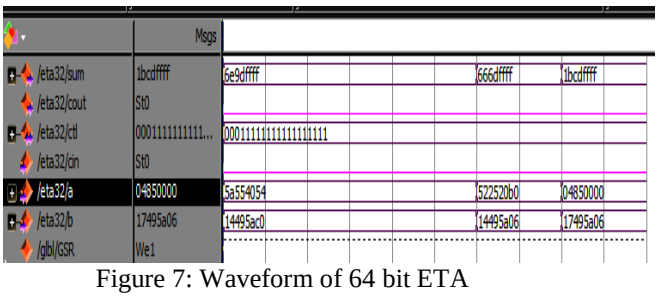

Figure 7: Waveform of 64 bit ETA

Table I. Three Input patterns and their corresponding results and Accuracies

A	B	CORRECT RESULT	OBTAINED RESULT	ACCURACY
5a554054	14495ac0	6e9e9b14	6e9dffff	99.97%
522520b0	14495a06	666e7a66	666dffff	99.99%
4850000	17495a06	1bce5a06	1b00ffff	99.45%

In this table I, the 64 bit input patterns are added by the ETA adder and the obtained result is compared with the correct actual result to get Overall error. Then the Accuracy of each result is manipulated using the formulae, which shows that the accuracy of the adder is above the acceptance probability.

VII. Simulation Results

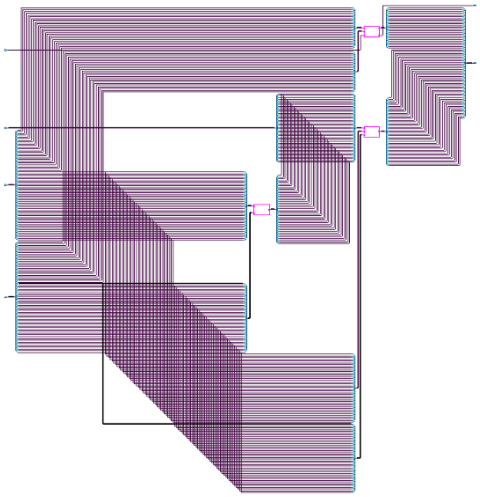

Figure 7: Schematic circuit of 64 bit ETA

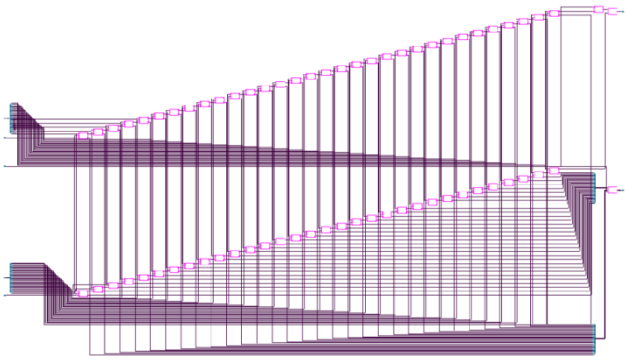

Figure 8:Schematic circuit of carry select adder

Table II
Performance results of ETA and comparison with conventional adders

ADDERS	POWER (mW)	DELAY (ns)	PDP (pJ)	AREA
RCA	0.32	4.53	1.45	2235
CSA	0.77	4.48	3.45	5249
CSK	0.26	2.89	0.75	2235
CLA	0.48	1.92	0.91	2554
ETA	0.10	1.60	0.16	1640

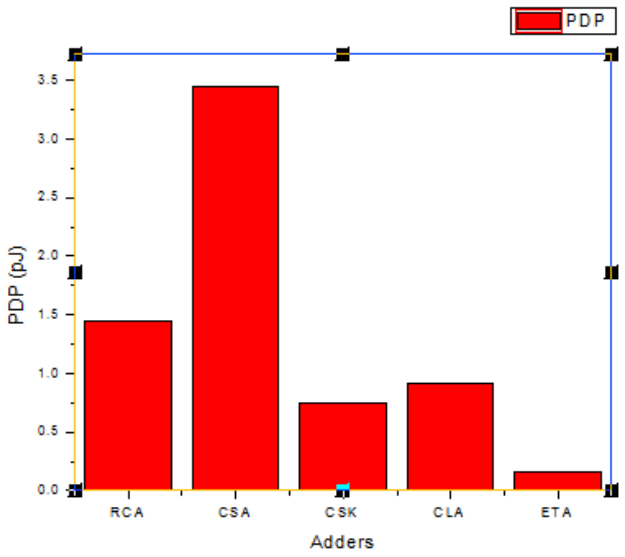

Figure 9: Graph showing performance of Adders

The above table II shows that the ETA adder performance better than the conventional adder in power as well as delay,withminimum power delay product. But the complexity of ETA is little bit more than the other, keeping this area as the penalty giving the good performance for the many digital applications.

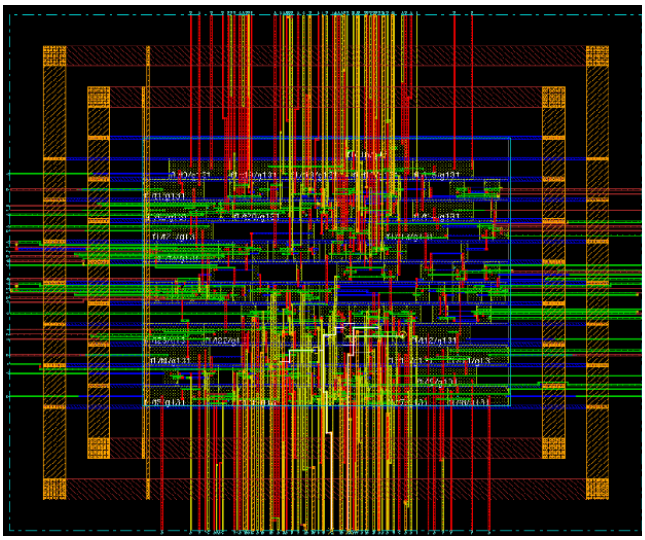

Figure 10: Layout Design of 64-bit ETA

VIII. Conclusion

In this paper, the accuracy of the adder is given out and the speed and power consumption are improved by a novel concept. The main application of this adder is in the DSP and the high speed controlling processors. The ETA found its application advanced mainly in multiply accumulator and which is proved to be efficient. In the present VLSI trend the power and speed are given importance than accuracy, because of rapid and abrupt growth in the portable and cellular devices.

Acknowledgment

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