Pre Layout And Post Layout Analysis Of Parallel Counter Architecture Based On State Look-Ahead Logic

Ulala N Ch Mouli Yadav, J.Samson Immanuel

Abstract— **The main objective of this project presents designing a parallel counter architecture which is used to improve the operating frequency. It is a partitioning methodology which consists of two paths named as counting path and state look-ahead path. The function of counting path is used to find all counting states and which consists of three main modules. Module 1 is 2 bit counter and which generates the counting states for the rest of modules through the state look-ahead logic path. State look a head path is used to prepare the counting path's next counting states, which triggers the all modules simultaneously. We implemented parallel counter and analyzed the parameters and layout is designed in cadence encounter tools.**

Index Terms- **High performance, Parallel counter, Partitioning methodology, Pipeline counter design.**

I. INTRODUCTION

Counters are widely used in almost all digital circuits such as measuring systems, analogue to digital converters, programmable frequency dividers and various arithmetic operations [2] [5]. Since many applications are comprised of these fundamental operations. Counter architecture design methodologies [1] explore tradeoffs between operating frequency, power consumption, area requirements. The key features required will vary greatly depending upon a particular application. In some cases we require counters with long counting width and high count frequency. It is highly desirable that counter must be designed in such a way that they are independent of counting width. While designing fast counters it is big challenge that wide and fast counters will result in much increased chip area since speed and area increase simultaneously [10]. Different kinds of counters has been proposed so far, early design methodologies [4] have been designed and improved counter operating frequency by partitioning large counters into multiple small modules, so that modules of higher significance were enabled when all bits in all modules of low significance saturate. Further enhanced counters have been designed in [12] and improved operating frequency using multiple parallel counting modules separated by DFFs in a pipelined structure. In Hoppe's design [6] counter operating frequency is improved by incorporating a

2-bit Johnson counter into the initial counting module in a partitioned counter architecture. In Hoppe's design counting modules of higher significance were constructed of standard synchronous counters triggered by the Johnson counter and additional synchronization logic. In Kakarountas's design [8] a carry look a head circuit has been used to replace the carry chain. The carry look ahead circuit used a pre scalar technique with systolic 4-bit counter modules ,with an extra detector circuit. In Jone's design [7] a counter specialized for applications with arithmetic operations using half and full adder prefix structure. This structure partially alleviated the cascading adder carry chain delay at the rate of a large area overhead. Systolic counters [9] [11] have high operating frequencies at the expense of representing the count value using two redundant binary numbers, which results in a large area overhead for state decoding. In order to reduce the power consumption Alioto [3] has been presented a low power counter design with a relatively high operating frequency. This design was based on cascading an analog block using MOS current mode logic to represent an analog divider such that each counting states input frequency was halved compared to the previous counting stage.

In this project, The parallel counter architecture is designed. This design is used to achieve high operating frequency through pipeline partitioning methodology. The 8 bit parallel counter is partitioned into four 2 bit synchronous counter. Here using only three simple repeated CMOS logic module types. These three modules are placed in a highly repetitious structure in both the counting path and state look ahead path. The state look ahead logic avoids the use of an over head delay detector circuit. The counting path's counting logic controls counting operation. The state look ahead path's state look ahead logic anticipates future states and thus prepares the counting path for these future states in the parallel counter architecture design, all counting modules are concurrently transition to their next states at the rising clock edge. The objective of this project is to improve the counter operating frequency by eliminating the carry chain delay and reduce the AND gate fan in and fan out.

This project is organized as follows, Section II discusses parallel counter architecture and related formulas. Section III provides simulation results using Cadence Encounter Tools.

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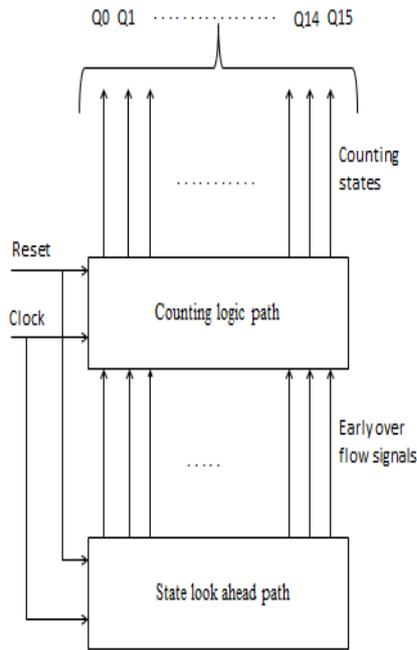
Figure.1 block diagram of parallel counter

II. PARALLEL COUNTER ARCHITECTURE

The block diagram of parallel counter architecture is shown in figure.1 and it consists of two major paths namely counting path and state look a head path.

A. Block Diagram

The block diagram of parallel counter is shown in figure. 1, and its width is 16 bit. As shown in the figure which consists of two paths counting path and state look a head path. It is a partitioning a methodology, counting path circuit consists of different modules are Module-1, Module 2, Module 3 S. In order to design 8 bit width parallel counter module 1 should be a simple synchronous 2 bit counter. Module 2 is a simple D flip flop, module 3 can be acts as a 2 bit counter but which is having different architecture. The State look a head path circuit consists of only module 2 and some logic gates such as AND gates, Inverters. Early over flow signals are generated by state look a head path and which are used to calculate the next states of counting path. Each module will have different functionality which are explained in below.

B. Architecture design

The architecture of parallel counter is shown in figure.2. Counting path and state look a head path has been shown in this figure. In this section we describe the functionality of counting path, state look a head path and each modules.
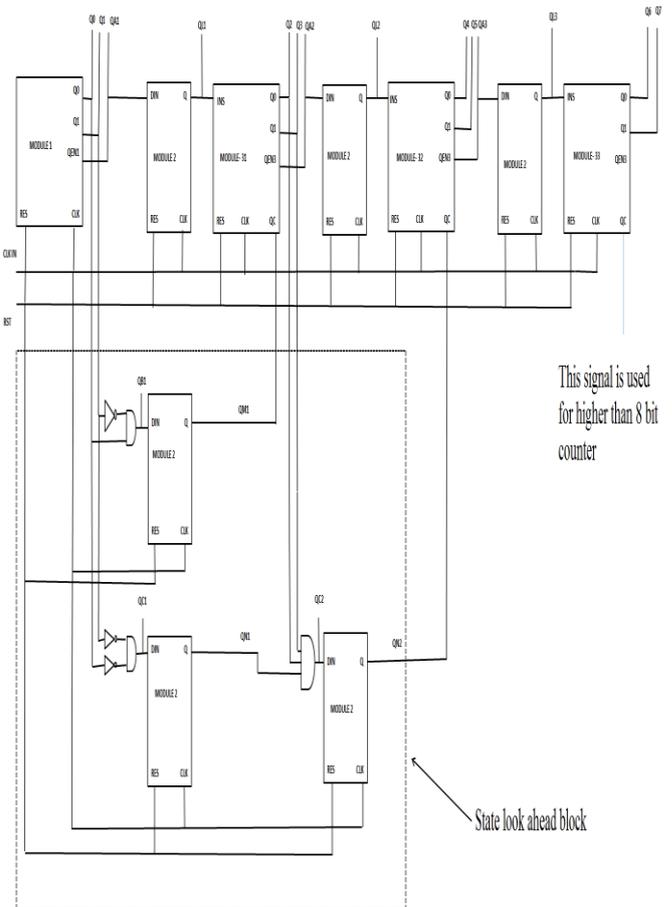

Figure.2 architecture of 8 bit parallel counter

C. Functionality of parallel counter

The counter operation starts with module 1 in the counting path, here counting path is explained below.

1) Counting path:

Counting path consists of different modules module 1, module 2, module 3S, where S =1,2,3 etc. here module 1 and module 3 are 2 bit simple counters but each will have different structure. Module 2 is a positive edge triggered D flip flop and it presents in both counting and state look a head paths. In counting path each module 3 S is preceded by module 2 it takes one clock pulse to trigger.

Module 1 is a synchronous 2 bit binary counter, which is used to find lower significance bits (Q0 Q1) which are needed to calculate higher significance bits through state look a head path. The output states of module 1 are Q1 Q0, and QEN1= Q1 AND Q0 bar. QEN1 connects to the module 2's DIN input
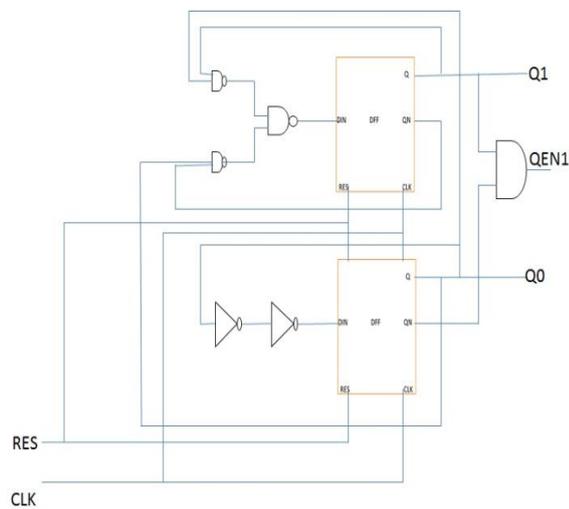
Figure.3 Architecture of Module 1

Module 2s in the counting path act as a pipeline between the module 1 and module 3 1 and between remaining module 3S's.Due to the placement of module 2 counter operating frequency increases by eliminating lengthy AND gates rippling and large AND gate fan in and fan out usually present in parallel counters. Higher significance modules are enabled by module 3 S's preceding module 2 and state look ahead path. The coupling of module 2 with module 3-1 introduces an extra cycle delay before module 3 1 is enabled. Module is triggered only when Q1 Q0 =10 in rest of cases qen1 would be zero. Thus, the module 2s in the counting path can be a 1 –cycle look a head mechanism, because it takes one clock cycle to trigger module 3 S's.

Module 3 S is a synchronous 2 bit binary counter, count is enabled by signal INS. INS is the signal which comes from the output of preceding module 2. The outputs of module 3S Q1 Q0 as shown in fig. 4. QEN3 is a enable signal which is used to trigger next higher level of module 2's.The equation of QEN 3= Q1 AND Q0 AND QC. Where QC is the signal which provides state look a head path and QEN3 connects to the subsequent module 2's DIN input.

2) State look ahead logic path:

The function of state look a head path is like a carry look a head adder, it decodes the lower significant bits and it carries this decoding over several cycles in order to calculate higher significant bits. State look a head logic is principally equivalent to the one cycle look a head mechanism in the counting path. For example, let us consider 4 bit counter, which is constructed of two 2 bit counting modules, the operation starts with module 1 the outputs are Q1Q0, the module decodes the lower significance states Q1Q0=10 and carries this decoding across one clock cycle and enables Q3Q2=01 at module-31 on the next rising clock edge. This process is equivalent to decoding Q1Q0=11 and enabling Q3Q2=01 on the next immediate rising clock edge. For example in a 6 bit ripple counter constructed of three 2 bit counting modules, Q5Q4 enables after decoding the over flow at Q1Q0 to enable Q3Q2 and decoding the over flow at Q3Q2 to enable Q5Q4. Next state higher order bits depends on the early flow states across clock cycles through the module 2's in the state look ahead path. This operation and logic avoids the

use of an overhead delay detector circuit that decodes the lower significance bits to generate the enable state signals for higher order modules and it enables all modules to be triggered concurrently on the clock edge.
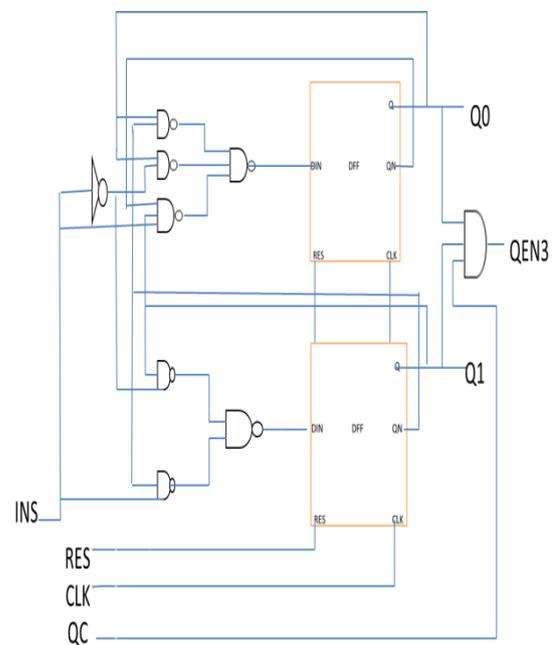

Figure.4 Architecture of Module 3

In order to design scalable parallel counter, the module 1 size increases gradually. For example to design 8 bit counter the module 1 size is a 2 bit counter. If module 1 size is a 3 bit counter then the parallel counter width is 17 bit, if module 1 size is 5 bit then the parallel counter width is 34 bit. 17 bit counter architecture is shown in diagram figure 5. For 17 bit parallel counter all module 2 and module 3's increases. How many number of module 2's and number of module 3's are used in the scalable counters architecture is shown in table I. For 17 bit module 1 will have same architecture as like module 1 in the 8 bit parallel counter with some logic gates. The architecture of 17 bit module is shown in figure. 5

A generalized N-bit counter topology is shown in figure.6, module 2's in the state look ahead logic play major role and responsible for generating the early overflow detection to the corresponding module 3S. Initially, early over flow signals generated by module 1 through the help of state 2 and state 3,etc.The output of module 2 in each early overflow pipelining chain is connected to the QC. QC is the input of appropriate module 3S. Each module 2s in state look ahead path is preceded by a small box (State-X) ,which is used to to decode the appropriate Q1Q0 value for early overflow pipelining. Each State-X block consists of simple AND gate that decodes the module-1 output. X denotes the number of clock cycles that the early overflow pipelining must carry through.
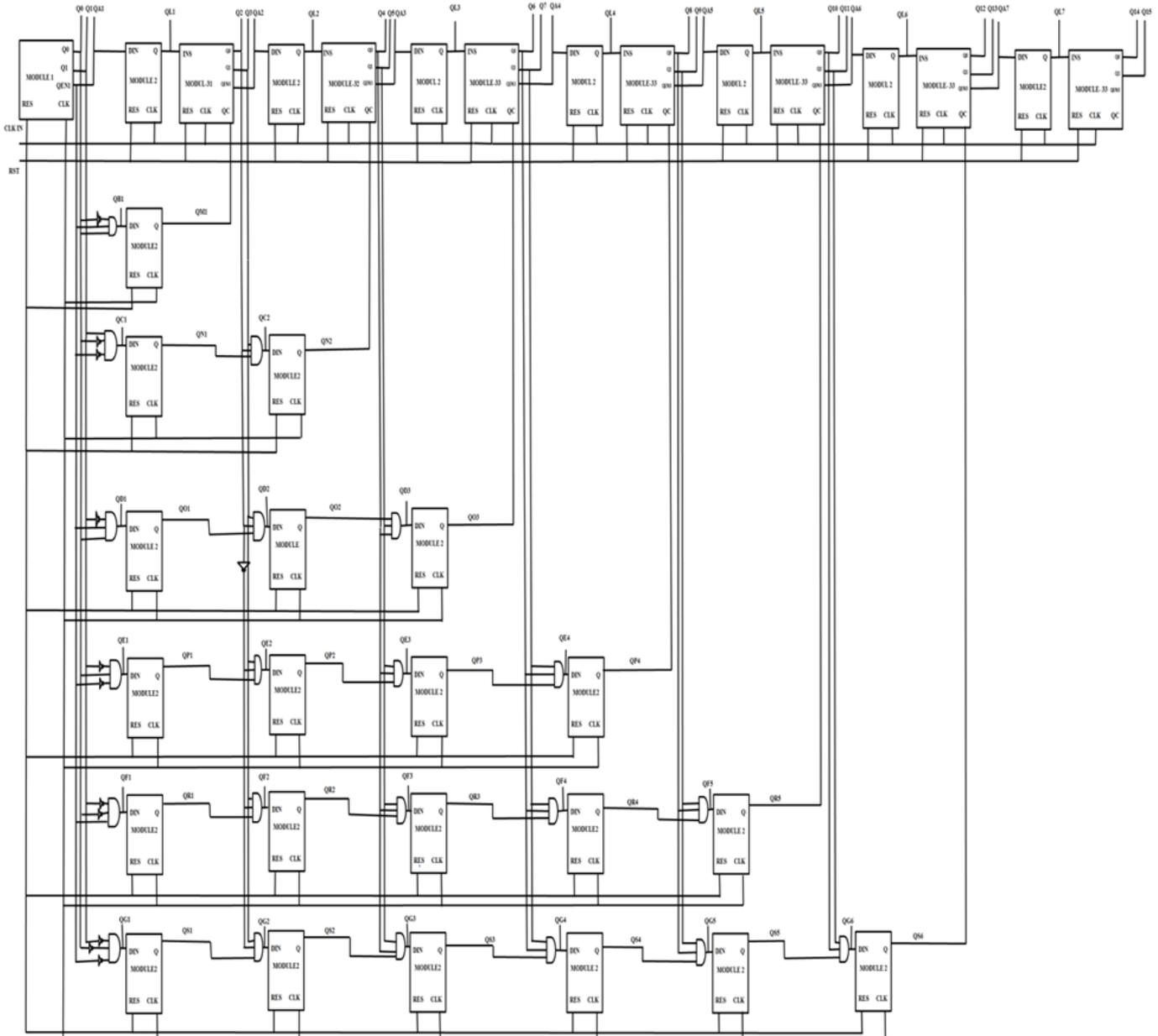
Figure.5. 17 bit parallel counter architecture

D. Operation of counter state equation

In this section, we discuss the operation of counter state equation based on the early flow equations. For example we derive the state equations for 8 bit counter in figure.2. here the previous counter state equations are denoted as $q_7q_6q_5q_4q_3q_2q_1q_0$ and the next state equations are $Q_7Q_6Q_5Q_4Q_3Q_2Q_1Q_0$. Thus the counter state equation necessary to enable Q_7Q_6 will contain $q_5q_4q_3q_2q_1q_0$ consequently, Q_3Q_2 at module 31i is enabled by previous state q_1q_0 from module 1, which carries through one clock cycle in the counting path's module 2 and enables module 31 on the next rising clock edge.

The 4 bit counter state equations can be expressed as

$$Q_3Q_2Q_1Q_0 = Q_3Q_2 \text{ Pipelined } (\overline{q_1q_0}) \qquad (1)$$

Where pipelined (X) denotes the previous bit values represented by X must be pipelined across one clock cycle.

The 6-bit counter state equation can be expressed as

$$Q_5Q_4Q_3Q_2Q_1Q_0 = Q_5Q_4 \text{ Pipelined } [(q_3\overline{q_2}) \text{ pipelined } (\overline{q_1q_0})] \qquad (2)$$

The notation pipelined (pipelined (X)) represents across two clock cycles, consequently the 8 bit counter state equation can be expressed as

$$Q_7Q_6Q_5Q_4Q_3Q_2Q_1Q_0 = Q_7Q_6 \text{ Pipelined}[(q_5\overline{q_4}) \text{ Pipelined}[(q_3q_2) \text{ Pipelined } (\overline{q_1q_0})]] \qquad (3)$$

E. Counter Area Analysis

In this subsection, we discuss the area overhead of parallel counter architecture based on the number of internal components such as module 1, module2 and module 3S. In general module 1 is an m bit counter that provides a set of early overflow states to enable higher significance states. If module 1 is an m bit counter, one early flow state input to the counting path and the rest of the early flow states to the state look-ahead path. Therefore total number of early overflow states (EO) generated by module 1 is

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Table I number of components and counter range

Module-1size Component	m=2 bits	Number Of Components	
		m=3 bits	m=4 bits
CS (counter range)	$8(2^1$ to $2^8)$	$17(2^1$ to $2^{17})$	$34(2^1$ to $2^{34})$
M3_CP	3	7	15
M2	6	28	120
EO_COMP	2	6	14

$$EO = 2^m - 1 \qquad (4)$$

The number of early overflow components needed to propagate early flow states in the state look ahead path is

$$EO\_COMP = EO - 1 \qquad (5)$$

The maximum allowable counter size (CS) can be computed using (4)

$$CS = m + (2*(2^m -1)) \qquad (6)$$

The required number of module 3S's in the counting path (M3_CP) which is equal to number of module 2's in the counting path (M2_CP) is

$$M3\_CP = M2\_CP = (CS - m) \div 2 \qquad (7)$$

The total number of module 2's in the state look-ahead path (M2_SLP) is

$$M2\_SLP = [(M2\_CP - 1) (M2\_CP)] \div 2 \qquad (8)$$

The total number of module 2's in the total architecture (M2) is
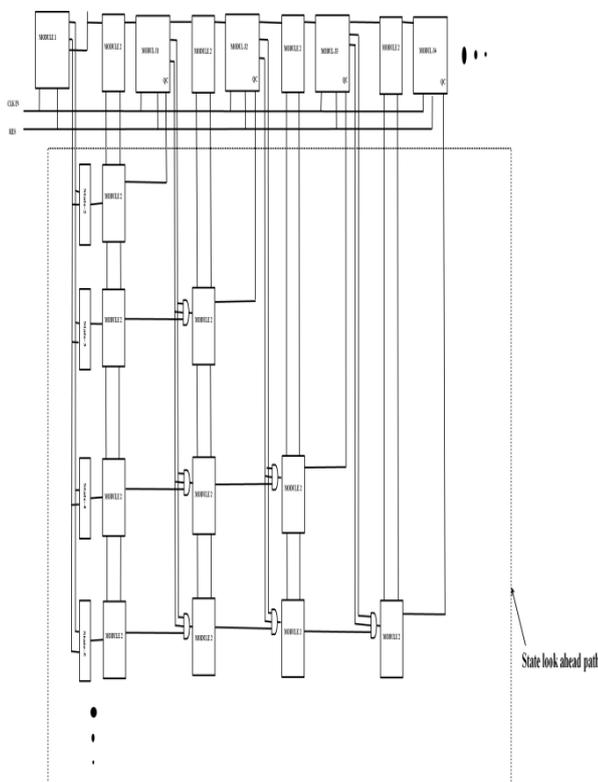
$$M2 = M2\_CP + M2\_SLP \qquad (9)$$

Figure.6 Architecture of N- bit topology

III. SIMULATION RESULTS

In this section, we present a simulation results for 8 bit parallel counter in figure 2. We provide both functional verification, layout design and performance verification using cadence encounter tools.
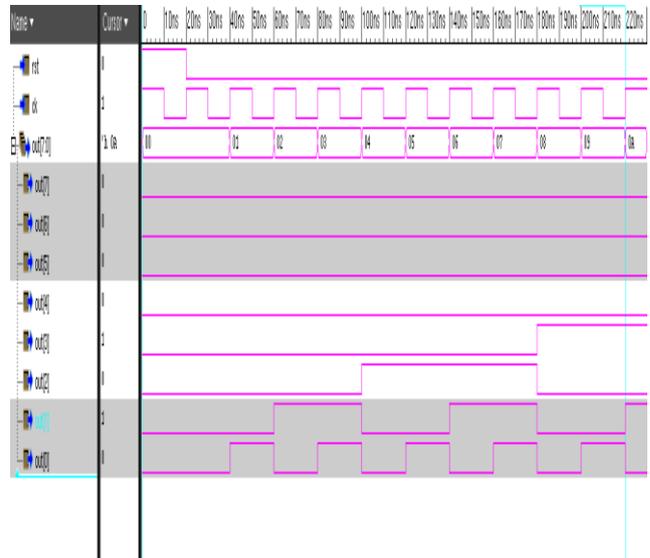
A. *Functional verification*

Figure.7 simulation waveform for 8 bit parallel counter

When the signal rst=1 then the count starts from initial state that is 00000000(Q7Q6Q5Q4Q3Q2Q1Q0), when the rst = 0, the count is going to change from initial state to next states. The count value changes to next state only at the positive edge of the clock and then it counts the value from 00000000(0) to 11111111(255).

B. *Performance verification*

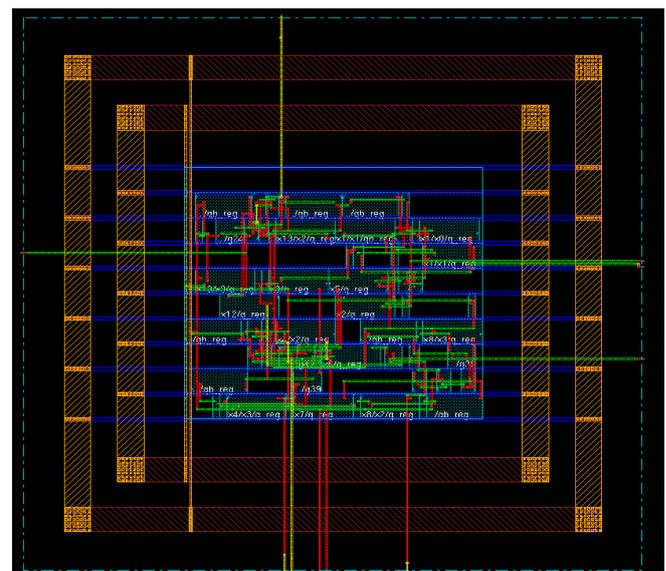To design layout for parallel counter we used cadence encounter tool.

Figure.8 layout for 8 bit parallel counter

Table II comparison results of parallel counter with conventional counter

Component	Cell Area	Power(uw)	Delay(ns)	Frequency (M Hz)	Power delay product
8 bit Parallel counter	1696	45.999	1.106	904.159	50.874894
Conventional Counter	705	30.869	2.220	450.450	68.52918

C. comparison results

Table II compares the parallel counter with conventional counter, it achieved high operating frequency and it has low delay value, but it has high area and quite more power consumption and it has low power delay product.

IV. CONCLUSION

In this project, we presented a high performance parallel counter using partioning methodology. In this design 2 bit counting modules and AND gates has been used. It comprises of 2 paths, state look ahead path activates all modules concurrently at the system's clock edge. In the counting path initial module responsible for generating all early flow states for calculating all higher significance bits. This parallel counter achieved high operating frequency and it can be useful in many digital circuits.

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