ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2 Issue 11, November 2013

An Analysis for Power Minimization at Different Level of Abstraction to Optimize Digital Circuit

Vivechana Dubey, Ravimohan Sairam

***ABSTRACT* — This paper aims at presenting an innovative conceptual framework suitable for achieving accurate and efficient estimation of power dissipation and optimization of digital circuits at all levels of abstraction e.g. circuit, layout, logic, architectural and system level. Aggressive voltage scaling to less than 1V as well as scaling of transistors has been proven to be the key to accurate modeling and estimation of power at early stages of design flow. A survey is presented in this paper depending on state-of- the- art optimization method and utilized CAD tool so that technology circuit and system parameters could be obtained and characterized for low power dissipation.**

***Index Terms*— Circuit optimization, Abstraction levels, Simulators.**

I. INTRODUCTION

The power consumption of recent electronics products has become a major design challenge, due to increase in speed, mobility and miniaturization of these products. Especially for portable and personnel communication devices, power consumption of the circuit determines the battery life-time, the generated heat and the required heat dispersion measures. Therefore, demand for low power digital circuit is rapidly increasing day-by-day. Digital circuit consists of a number of interconnected logic circuits such as gates, flip-flops and many other circuit which together perform function on number of input signals for given conditions . Change of signal propagates through different interconnected path which causes signal switching activity in those path. Power dissipation occurs in the circuit due to signal switching activity resulting in charging and discharging of capacitive **load of CMOS gates. The power dissipation in CMOS circuit** depends on fabrication technology, operating frequency, supply voltage, and switching activity per clock cycle. Therefore, accurate power estimation is needed to be done for given input condition before chip fabrication is actually done[1].

The major part of power dissipation in CMOS devices is due to following expression:

$$P = \frac{1}{2} C.V_{DD}^2.f.N + Qsc.V_{DD}.f.N + I_{leak}.V_{DD}$$

where P is total power of the circuit, VDD is the supply voltage, and f is the frequency of operation.

The first term represents the power required to charge and discharge circuit nodes. Node capacitances are represented by C. The factor N is the switching activity, i.e., the number of gate output transitions per clock cycle.

The second term in Eqn. 1 represents power dissipation due to short circuit current that is current flowing from supply to ground during output transitions. The short-circuit component arises when both the NMOS and PMOS transistors are "ON" simultaneously, providing a direct path from VDD to ground. The factor QSC represents the quantity of charge carried by the short-circuit current per transition.

The third term in Eqn. 1 represents static power dissipation due to leakage current Ileak resulting from reverse biased diode conduction and sub-threshold conduction. The sub-threshold leakage occurs due to carrier diffusion between the source and the drain when the gate-source voltage, Vgs, has exceeded the weak inversion point, but is still below the threshold voltage V, where carrier drift is dominant. In this regime, the MOSFET behaves as a bipolar transistor, and the sub-threshold current is exponentially dependent on the gate-source voltage Vgs. The three terms above for power are called as switching activity power; short-circuit power and leakage current power respectively.

In this paper, the strategy for power minimization involves reduction of switched capacitance, supply voltage scaling and switching activity at various levels of abstraction. An architectural voltage scaling strategy which trade-offs silicon area for lower power consumption has been proposed [2]. Another key strategy for sub-1V operation is to lower the threshold voltage of devices, which unfortunately comes at the cost of increased leakage power. CAD tools that support low-voltage, low power design should explicitly take leakage into account.

The rest of the paper is organized as follows: The remainder of this paper is organized as follows. In Section II, we provide optimization strategy at all levels of abstraction. In Section III, the threshold voltage and supply selection scheme is described. In Section IV, the tool based power analysis is presented. In Section V, we present the summary and conclusion.

II.OPTIMIZATION STRATEGIES

A.CIRCUIT LEVEL

The order of gate input in complex gate design affects power and delay. Paper [3] and [4], explained methods to optimize the power and delay of logic-gates based on transistor reordering. It is obtained that late arriving signals should be placed closer to the output to minimize gate propagation delay. However, the average power dissipated is dependent on the transition probabilities of the gate inputs and the internal node capacitance (due to parasitic drain and source capacitance and interconnect capacitance).

The power and delay of circuit significantly depend on the transistor sizing in a combinational gate .Increased transistor size decreases gate delay however power dissipation and delay of fan-in gate increases due to increased load capacitance. The problem is taken over by computing slack

(represents how much a gate can be slowed down without affecting critical delay of the circuit at each gate in the circuit [5], [4].

B. LOGIC LEVEL

In this level, optimization of combinational logic is done in two phases: technology-independent optimization by manipulating logic equations and technology-dependent optimization by mapping equations to particular technology library [6].

Secondly, path balancing to reduce switching activity power due to spurious transitions in logic circuit is utilized. Ideally delay of paths converging at each gate in the circuit should be equal. Adding minimal number of unit-delay buffer to equalize delay while eliminating spurious switching activity due to additional delay have been proposed. The design of a multiplier with transition reduction circuitry that accomplishes glitch reduction by path balancing is described in [7].

Factorization of logical expressions is another means of technology-independent optimization [8]. Optimized logic equations are now been mapped into a target library that contains optimized logic-gates in the chosen technology. A typical library will contain hundreds of gates with different transistor sizes. Modern technology mapping methods use a graph covering formulation, originally presented in [9], to target area and delay cost functions.

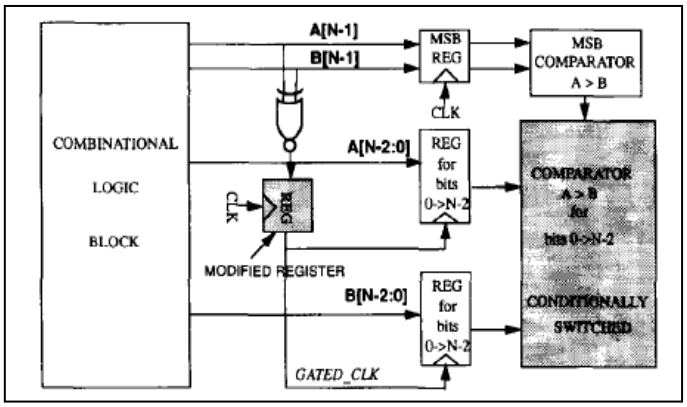

Fig. 1. Gated clock to reduce power

Optimization of sequential logic work at two levels of abstraction: 1) State transition Graph Level and 2) Logic gate and Flip-flop level. Encoding state transition graph for implementation of two-level and multilevel circuit with minimum power dissipation is described in[10]. To reduce switching activity in data path logic encoding is considered. One-hot encoding to reduce switching activity in arithmetic logic is proposed in [11]. Register file in sequential circuit need not to be updated per clock cycle .Power reduction by gating the clocks of the inactive registers can be achieved moreover switching activity within the register can be reduced to negligible levels. As shown in fig. 1. The X-NOR output of A[N-1] and B[N-1] is latched to generate gated clock by a special register.

For a given logic-level circuit and a particular input stimulus, if idling sub circuits can be detected which do not contribute to the computation of the output response for this input stimulus, power reduction can be obtained by "turning off" the idling sub circuits. A technique called pre-computation [12]. Assume a pipelined system for comparing the output of two numbers from a block of combinational logic as shown in Fig. 16; the first pipeline stage is a combinational block and the next pipeline stage is a comparator which performs the function A > B, where A and B are generated in the first stage (i.e., from the combinational block). If the most significant bits, A[N - I] and B[N - 11, are different then the computation of A > B can be performed strictly from the MSB's and therefore the comparator logic for bits A[N- 1 : 01 and B[N- 2 : 01 is not required (and hence the logic can be powered down). If the data is assumed to be random (i.e., there is a 50% chance that A[N - 11 and B[N - I] are different), the power savings can be quite significant. The reduction in power dissipation is a function of the probability that the XNOR gate evaluates to a 0. Other inputs can be added to the pre-computation logic to increase power reduction.

C. ARCHITECTURAL LEVEL

During synthesis of design adequate analysis for power consumption of circuit is needed to explore design space manually. One method of analyzing power of the design is to translate given high level architecture description to the gate, circuit, or physical level; at which point reasonably accurate low-level power analysis tools can be utilized[13].if large number of design alternatives are present and to be evaluated, the method will be infeasible. Power models for the underlying architecture primitives such as data path execution units, control units, memory elements, and interconnect can be created using lower level analysis tool if final lower level is fixed.

The power models are obtained by characterizing the estimated capacitance that would switch when the given module is activated [13]. In [21], known signal statistics are used to obtain models that are more accurate than those obtained from using random input streams. What is needed for this is an estimate of the activity for each module. Activity factors for the modules can be obtained from functional simulation over typical input streams, or from statistical/analytical models that are built where possible. Several of the synthesis methods surveyed in following section, uses power models or estimation methods that have been tailored to their application domain and search method.

Optimization of circuit for low power in this level is done by behavioral synthesis. Behavioral synthesis refers to the process of mapping a high-level specification in the form of data-flow graph and control-flow graph or combination of both of a problem into a register-transfer level design.

The input high-level specification can be modified through specific transformations that potentially lead to power reduction. The most important transformations for fixed throughput systems are those which reduce the number of control steps. Slower clocks can then be used for the same throughput, enabling the use of lower supply voltages

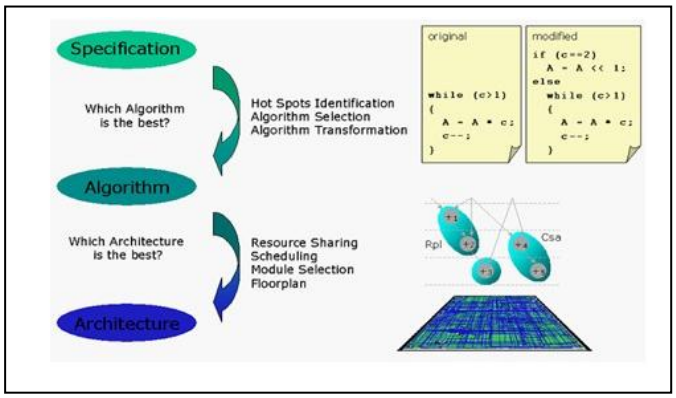

Fig.2. Power optimal Algorithm and Architecture

The allocation and assignment processes map operations in the control/data flow graph to functional units, variables to registers, and define the interconnect between them in terms of multiplexers and buses The power consumed in memories can be a major part of the system power consumption and impact power in two ways. First memory accesses consume a lot of power, especially in off-chip access, and second size of memory, large memory size present greater capacitance that switches per access. Loop ordering as control flow transformations is presented to minimize the memory component of the overall system power consumption.

D. SYSTEM LEVEL

System-level design consists of the mapping of a high-level system model onto an architecture. Different processing algorithms and hardware architectures are needed to be evaluated to achieve reductions in power consumption of about 75% before net list synthesis (see figure 3). The system specification defines system requirements, and is expressed at a very high level of abstraction. This specification is usually written in a standard language, such as C/C++ or System C. Using this system specification, algorithms that realize system functionality are developed and optimized, generally in those same standard languages. The algorithmic description consists of an executable specification, or functional description. This executable specification captures the system function, and enables the verification thereof. It can be written as a behavioral description, which can be refined into a bit-accurate, pure functional design description.

The given algorithms simultaneously comprehend the application-dependent design constraints, such as power and area. To overcome these problems, the current being drawn by the software during the execution of a program needed to be physically measured.

An inexpensive and practical technique in this regard has been developed [10] for analyzing the power cost of programs for a given software. Given the ability to evaluate programs in terms of their power costs, it is possible to search the design space in software power optimization. The choice of the algorithm used can impact the power cost since it determines the runtime complexity of a program [22]

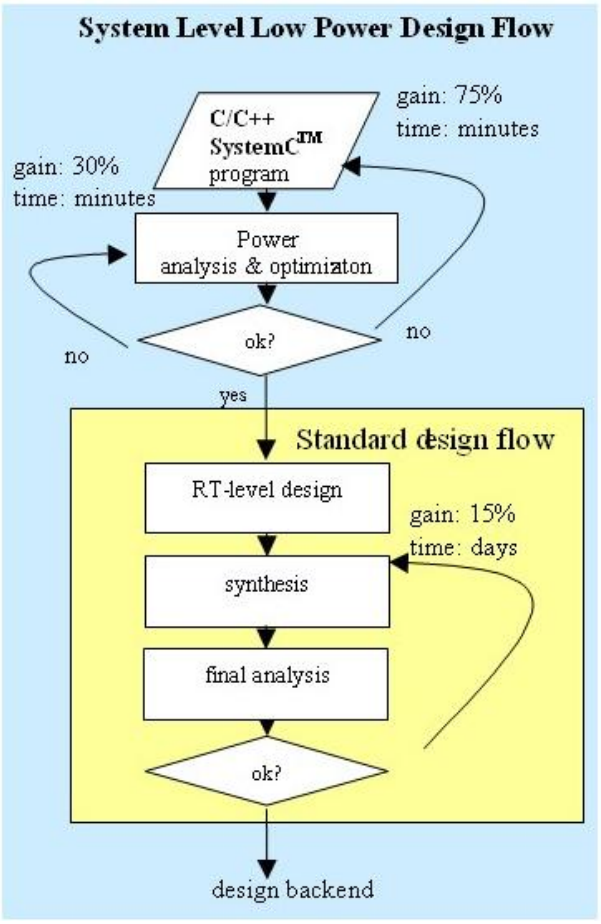

Fig.3. System level low power design flow

E. LAYOUT LEVEL

After algorithmic and architectural selection, layout level implementation in done where power optimization can be done by supplying synthesis tools with a low power cell library. Chip placement and routing can target minimization of activity capacitance product wires.

III. METHOD TO THRESHOLD VOLTAGE AND SUPPLY SELECTION

Dynamic power in CMOS circuit is given by expression:

$$P = \alpha\, CL\, VDD2F\, CLK$$

It is needed to lower supply voltage to reduce power consumption. However, at lower supply voltages the individual circuit elements run slower and hence result in reduced performance. Instead if threshold voltage (Vth) of the device is reduced, the supply voltage could be scaled down (and therefore lower switching power) without loss in performance.

Figure 4 shows an experimentally obtained plot of VDD vs. VT while keeping performance (gate delay) constant.

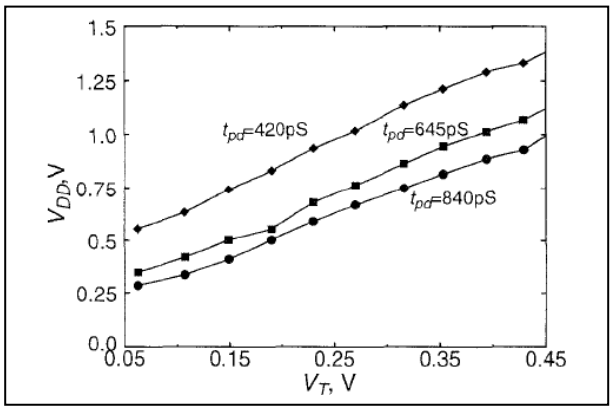

Fig. 4. Experimental VDD vs VT for fixed delay

These experimental plots are obtained from ring oscillator structures by adjusting the VT and VDD for a fixed delay.

Low threshold voltage gives significant power improvement, therefore methods for lowering threshold voltage are given focus. Experiment shows that optimum voltage can be significantly lower than 1V.Switching activity plays important role in selection of threshold voltage and supply voltage the optimum threshold and power supply voltage. For example, a circuit which has very low switching activity will require a high-threshold voltage (and hence high power supply voltage).

IV. TOOL FOR ANALYSIS OF POWER

In this section, we specify he tools which can be used to analyze power of the CMOS circuit at different level.

- Power Mill is one of the simulator tool which is used for simulation of current and power at transistor level from synopsys.
- At RTL (Register Transfer Level) Watt Watcher is a power estimator tool from Sente.
- Power Play is another Dynamic power estimator based on logic simulation. Also, there is one pattern independent current estimator tool named as crest.
- McPower is a power estimator tool which utilizes Monte-Carlo approach to calculate power of the circuit.
- Spice Simulators is a mentor graphics tools consisting of several simulator like Mach PA, ELDO simulator, Silvaco, SmartSpice, etc.
- Altera Quartus II is one of the another simulator used in power estimation and optimization of circuit for area, power and timing characteristics Other CAD tools are also useful in power estimation and optimization of circuit with similar or better results. Figure5. Shows recent extensionsthat allow the user to perform the kind of multilevel optimization.

As shown in the Figure 5, An algorithmic power estimator, an ATP exploration tool, and an architectural power analyzer are the three main tools to facilitate low-power design. All these tools employ a library of power models for data paths, memory, control, and interconnects. Each tool uses whatever information is available at that level of abstraction. By applying these tools in an integrated top-down fashion, the user can begin with a high-level description of the desired functionality and systematically converge to the optimum low-power algorithm and architecture.

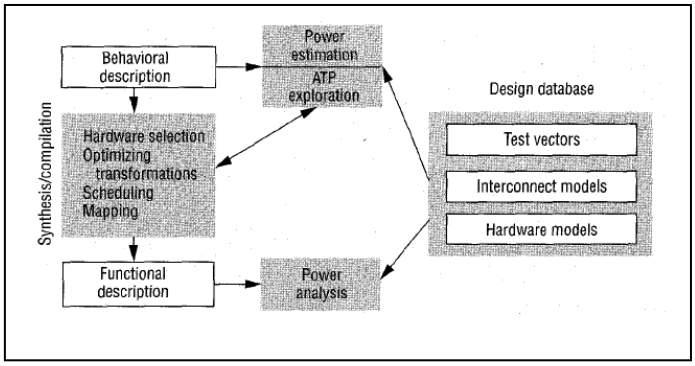

Fig.5. Low-power design Environment. Shading indicates extensions to facilitate Low-power design.

V. CONCLUSION

This paper presented some of the factors of power consumption in CMOS circuit and technologies for low power systems. Optimization of circuit at different levels of abstraction, namely the circuit, logic, architecture, system and layout level, with tools for analysis of power at these levels is specified in the paper. However, the work is not comprehensive, rather described part of power optimization strategy as optimization of threshold voltage lowers supply requirement yielding significant power reduction in the circuit.

REFERENCES

[1]. Nourivand.A, ChunyanWang, Ahmad.M.O "A VHDL-based technique for an accurate estimation of leakage power in digital CMOS circuits," in the 3rd international IEEE-NEWCAS conf., 2005.pp.47-50.

[2]. A. Chandrakasan, R. Brodersen, Low Power Digital CMOS Design, Kluwer Academic Publishers, July 1995.

[3]. S. C. Prasad and K. Roy. Circuit Optimization for Minimization of Power Consumption Under Delay Constraint. In Proceedings of the Int'l Workshop on Low Power Design, pages 15–20, April 1994.

[4]. C. H. Tan and J. Allen. Minimization of Power in VLSI Circuits Using Transistor Sizing, Input Ordering, and Statistical Power Estimation. In Proceedings of the Int'l Workshop on Low Power Design, pages 75–80, April 1994.

[5]. Chandrakasan, et al., "Design considerations and tools for lowvoltage digital system design," in Proc. 33rd. Design Automation Conference, pp. 113-118, 1996.

[6] S. Devadas, A. Ghosh, and K.Keutzer. Logic Synthesis. McGraw Hill, New York, NY, 1994.

[7] C. Lemonds and S. S. Mahant Shetti. A Low Power 16 by 16 Multiplier Using Transition Reduction Circuitry. In Proceedings of the Int'l Workshop on Low Power Design, pages 139–142, April 1994.

[8]. S. Devadas and S. Malik, A Survey of Optimization Techniques Targeting Low Power VLSI Circuits, in: Proc. 32nd IEEE Design Automation Conference, (1995).

[9]K.Keutzer. DAGON: Technology Mapping and Local Optimization. In Proceedings of the 24th Design Automation Conference, pages 341–347, June 1987.

[10]. C-Y. Tsui, M. Pedram, C-A. Chen, and A. M. Despain. Low Power State Assignment Targeting Two- and Multi-level Logic Implementations. In Proceedings of the Int'l Conference on Computer-Aided Design, pages 82–87, November 1994.

[11] W. A. Chren. Low Delay-Power Product CMOS Design Using One-Hot Residue Coding. In Proceedings of the Int'l Symposium on Low Power Design, April 1995.

[12]. M. Alidina, J. Monterio, S. Devadas, A. Ghosh, and M. Papaefthymiou, "Precomputation-based sequential logic optimization for low power," in 1994 International Workshop in Low Power Design.

[13]. F. Najm. A Survey of Power Estimation Techniques in VLSI Circuits (Invited Paper). IEEE Transactions on VLSI Systems, 2(4):446–455, December 1994.

[14]. S. Powell et al. Estimating power dissipation of VLSI signal processing chips: The PFA technique. VLSI Signal Processing IV, pages 250–259, 1990.

[15]. P. Landman and J. Rabaey. Power estimation for high level synthesis. In Proceedings of the European Design Automation Conference, pages 361–366, Paris, Feb. 1993.

[16]. P. w. Ong and R. H. Yan. Power-conscious software design – a framework for modeling software on hardware. In Proceedings of 1994 IEEE Symposium on Low Power Electronics, pages 36– 37, San Diego, CA, Oct. 1994.

[17]. P. Landman et al., "An Integrated CAD Environment for Low Power Design", IEEE Design and Test, pp. 72-82 Summer 1996.

Vivechana Dubey Ms. Vivechana Dubey is currently pursuing M.Tech. (VLSI) from Shri Ram Institute of Technology, Jabalpur under RGPV University Bhopal.She has completed B.E. from TIT College, Bhopal under RGPV University Bhopal .She is a member of research gate.

Ravimohan Sairam Mr. Ravimohan Sairam is a Associate Professor in SRIT College, Jabalpur. He has many publications in National and International Conference. He has guided M.tech Students in their Thesis work