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Design a Low Power Half-Subtractor Using AVL Technique Based on 65nm CMOS Technology

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Abstract: Arithmetic circuits play a vital role in designing of any VLSI system. Subtractor is one of them. In this paper, Half-Subtractor is being designed using Adaptive Voltage Level (AVL) techniques.This design consumed less power as compare to conventional design. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which supply potential is increased. This paper represents how to control power using AVL techniques. The AVL technique based Half-Subtractor compared to conventional design that based on power consumption, propagation delay, speed and layout area is more preferred. Power consumption of the proposed cell is measured and compared. The result shows that there is a significant reduction in power consumption for this proposed cell with the AVL technique. This design is much useful in designing the system that consumed less power. The circuit is simulated on MicroWind 3.1 and DSCH in 65 nanometer CMOS technology.

Keywords: Half–Subtractor, AVL techniques, Low Power, High Speed, VLSI

I. Introduction:

Subtractor is a combinational circuit which represents the smallest unit for subtraction in digital systems. It is not only used for arithmetic calculation in many device processors but also used in other part of processor for calculating address. Stack pointer use subtraction operation in push-pop logical operation for storage of address. The simplest combinational circuit which performs the arithmetic subtraction of two binary digits is called half- Subtractor [1] . This is the necessory building block for designing a VLSI system.Figure1.1 shows the logic diagram of half subtractor. In which , two inputs A and B are applied at the different Gates and corresponding output are gotted. These are the two inputs which consists of two 1-bit numbers A and B ,where A represents Minuend and B represents Subtrahend. From the logic symbol ,there are two outputs corresponding inputs. Those output are the Difference(D) of A and B and Borrow bit denoted by $B_{out.}$

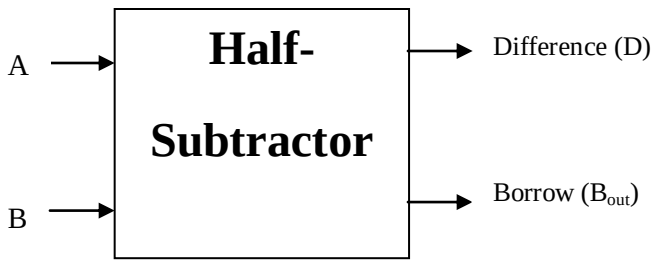

Figure1.1: Logic Symbol of half Subtractor

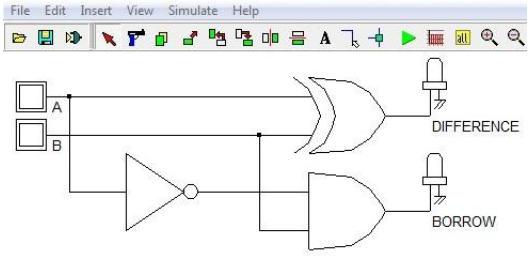

Figure1.2: Logic diagram of Half Subtractor

Table 1.1: Truth Table of Half Subtractor

Inputs		Outputs	
Minuend bit A	**Subtrahend bit B**	**Difference D**	**Borrow B_{out}**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Figure 1.2 shows the logic diagram of Half-Subtractor. From table 1.1, the logic expression for Difference output and Borrow output can be written as

$$D = A \oplus B$$
$$B_{out} = \overline{A}\, B$$

II. Conventional Half Subtractor:

In conventional Half-Subtractor [1], a simple transistor level circuit is designed. Where, all N-MOS are connected to ground terminal and all P-MOS are connected to Source terminal. The circuit is designed using CMOS and whole circuit consists of 6 transistors. In which 3 N-MOS transistors and 3 P-MOS transistors are employed. Leakage current [3] also place a vital role in designing of any system. It should be as low as possible. Power consumption is also an important parameter in system design. Figure 2.1 shows the circuit diagram of conventional Half-Subtractor. Figure 2.2 shows the variation of power Vs supply voltage of conventional Half-Subtractor. At Vdd = 0.7 V, power consumption is 2.735 µw.

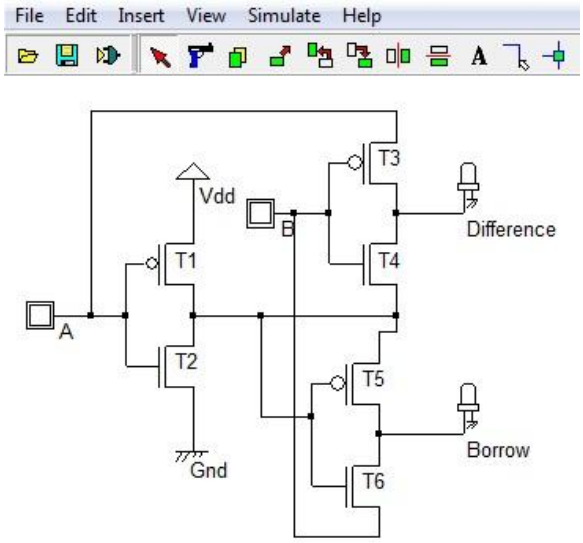

Figure2.1: Circuit diagram of Conventional Half Subtractor

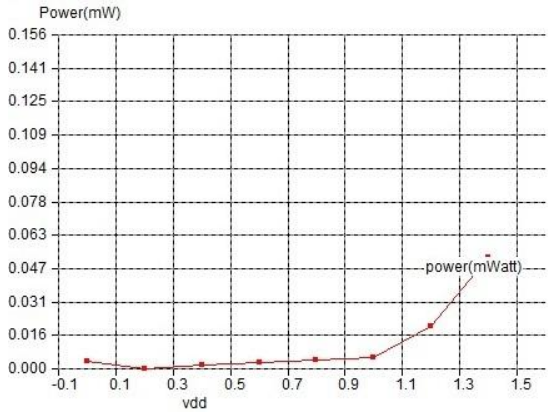

Figure2.2: Variation of Power Vs Supply voltage using conventional design style

III. Half-Subtractor Using Adaptive Voltage Level (AVL) Technique:

An adaptive voltage level technique [2,3] can be used to control circuits and it can be used either at the upper end of the cell to bring down the supply voltage value , called AVLS scheme or at the lower end of the cell to lift the potential of the ground node , called AVLG scheme. By this technique reduction of power dissipation is occurred. The power dissipation is reduced less

than conventional design cell. The complete effect of these techniques on the power consumption is described as follows.

➢ Design Half Subtractor using AVLG :

In AVLG technique [2,3], a combination of 1-N-MOS & 2-P-MOS are connected in parallel. So that a input clock pulse is applied at the N-MOS of circuit of AVLG and rest of all P-MOS are connected to ground. This AVLG circuit is connected at the ground terminal of conventional one by removing ground. This ground terminal is connected to the AVLG circuit. Figure 3.1.1 shows the Logic symbol of Half Subtractor designed using AVLG technique. Figure 3.1.2 shows the circuit diagram of Half-Subtractor designed using AVLG technique.

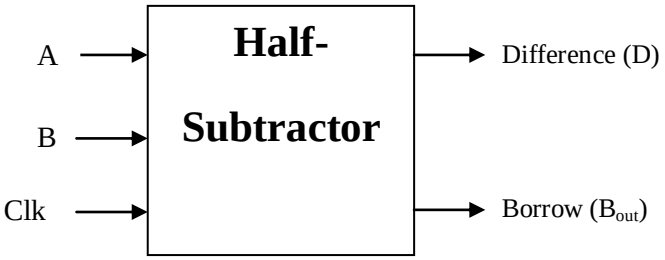

Figure 3.1.1: Logic Symbol of Half Subtractor Incorporated AVLG Technique

Table 3.1.1 shows the truth table of Half Subtractor using AVLG technique. Depending upon the clock and inputs, variation in output is varied. In AVLG circuit, there is a Sharp decrease in the V_{GS} & V_{GD} of transistor T4 due to supply voltage reduction. So that there is less melioration in the V_{GS} & V_{GD} of transistor T2 & T6 .The major power consumption is reduced by Transistor T7. Figure 3.1.3 shows the variation of power Vs supply voltage of Half-Subtractor design using AVLG technique. Where the power consumption is measured at the various supply voltage. At Vdd = 0.7 V, power consumption is 2.321μw.

Table 3.1: Truth Table of Half Subtractor using AVLG technique

Inputs		Outputs	
Minuend bit A	**Subtrahend bit B**	**Difference D**	**Borrow B_{out}**
0	0	X	X
0	1	1	1
1	0	X	X
1	1	0	0

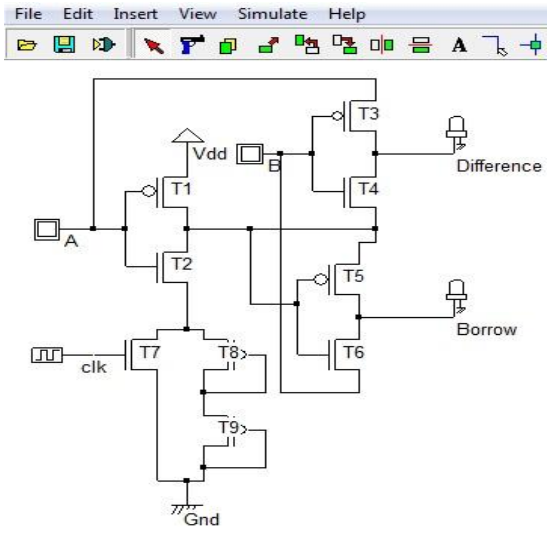

Figure3.1.2: Circuit diagram of Half Subtractor Incorporated with AVLG Technique

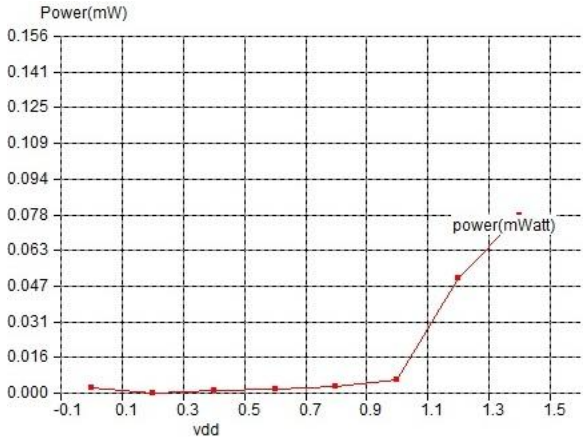

Figure 3.1.3: Variation of Power Vs Supply voltage using AVLG design style

➢ Design Half Subtractor using AVLS:

In AVLS technique, a combination of 2- N-MOS & 1-P-MOS are connected in parallel. So that a input clock pulse is applied at the P-MOS of circuit of AVLS and rest of all N-MOS are connected to drain terminal. This AVLS circuit is connected at the voltage supply source terminal of conventional one by removing voltage supply source. A very small leakage current [4] is flowing in designing using AVLS technique. Also power dissipation [5] is very less here. Figure 3.2.1 shows the Logic symbol of Half –Subtractor designed using AVLS .

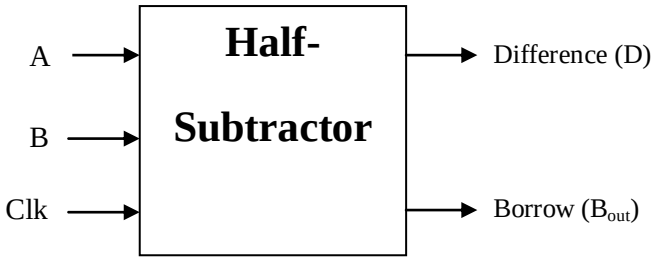

Figure 3.2.1 : Logic Symbol of Half Subtractor using AVLS Technique

Table 3.2 shows the truth table of Half-Subtractor designed using AVLS technique. Figure 3.2.2 shows the circuit diagram of Half –Subtractor designed using AVLS technique. The drain terminals of transistors T1 & T3 are connected to the supply voltage via AVLS circuit and these are under ON state. Figure 3.2.3 shows the variation of power Vs supply voltage of Half-Subtractor design using AVLS technique.

Table 3.2.1: Truth Table of Half Subtractor using AVLS Technique

Inputs		Outputs	
Minuend bit A	**Subtrahend bit B**	**Difference D**	**Borrow B_{out}**
0	0	0	0
0	1	X	X
1	0	1	0
1	1	0	0

There is a decrease in the V_{GS} & V_{GD} in Transistors T3 & T5 which a main source of power reduction. An Additional loss in power consumption also exists due to decrease in drain voltage of transistors T2, T5 & T7. This approach is more valuable for reducing the power consumption also for the leakage current[3] .For very low Power consumption, AVLS technique is most responsible. Subtractor designed at micron CMOS technology [6], produces the better results. But now a day of nanotechnology. At Vdd = 0.7 V, power consumption is 1.622μw.

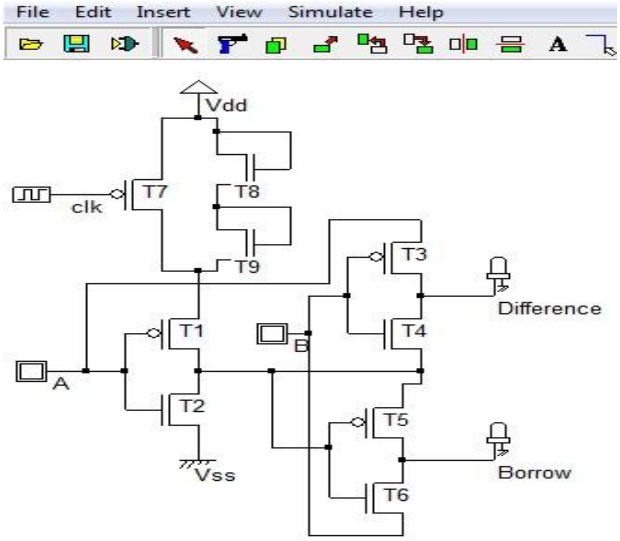

Figure 3.2.2: Circuit diagram of Half Subtractor Incorporated with AVLS Technique

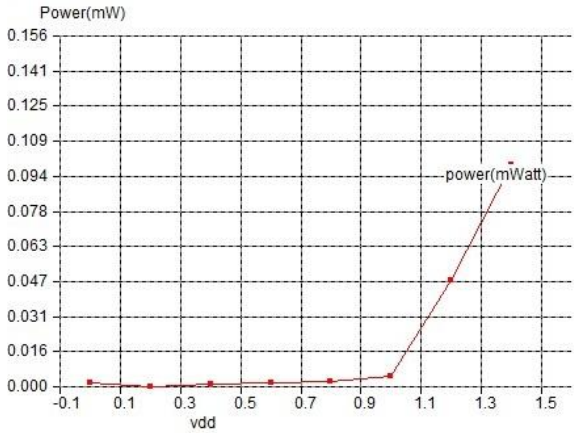

Figure 3.2.3: Variation of Power Vs Supply voltage using AVLS design style

IV. Simulation Results

All the simulation waveforms have shown below. Here, Figure 4.1 shows the simulation Waveform of Conventional Half-Subtractor. Figure 4.2 shows simulation Waveform of Half-Subtractor incorporated with AVLG Technique. Figure 4.3 shows simulation Waveform of Half-Subtractor incorporated with AVLS Technique. From the result, it is very clear that power consumption occurs via AVLS technique very small as compare to other two. Also leakage current [3] is also very small via AVLS technique. Thus designing VLSI system via AVLS technique achieve high performance and low power dissipation.

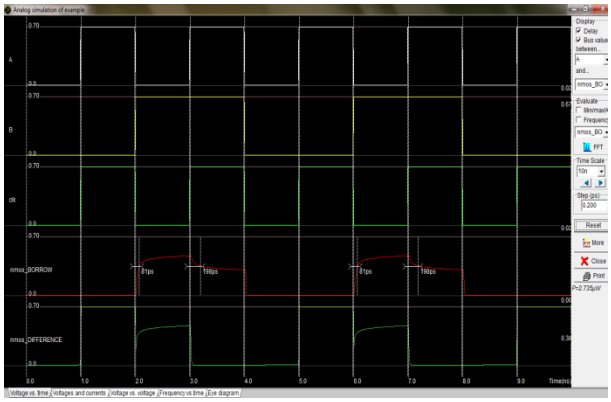

Figure 4.1: Simulation Waveform of Conventional Half-Subtractor

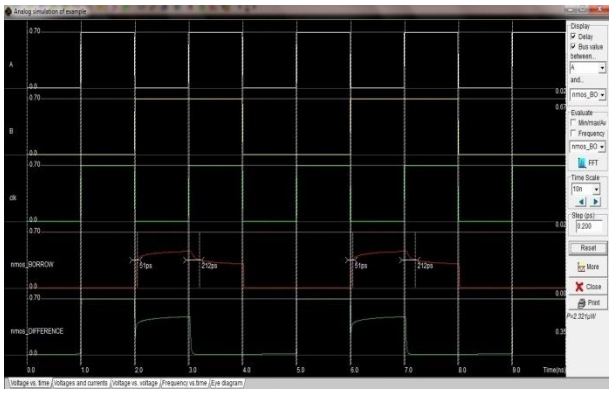

Figure 4.2: Simulation Waveform of Half-Subtractor incorporated with AVLG Technique

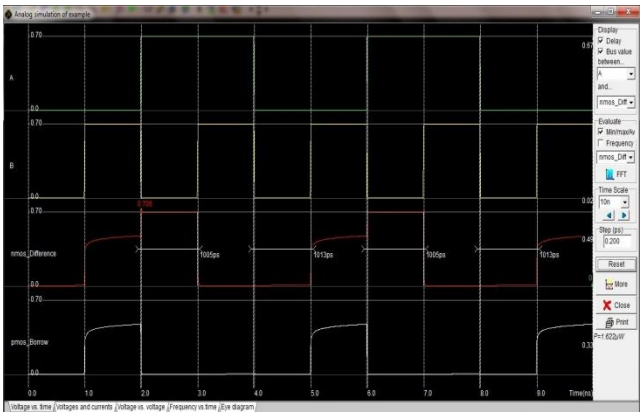

Figure 4.3: Simulation Waveform of Half-Subtractor incorporated with AVLS Technique

From the result, it is very clear that power consumption occurs via AVLS technique very small as compare to other two. Also leakage current [3] is also very small via AVLS technique. Leakage is an important factor during the designing of any system. Thus designing VLSI system via AVLS technique achieve high performance and low power dissipation.

V. Conclusion

The Simulation results clearly explain the reduction in the power consumption by incorporated with AVL Technique that is either AVLG or AVLS Technique. Table 5.1 and Table 5.2 shows the comparison between System design using 65 nm & .90um CMOS Technology respectively . As the technology [7] is being scaled then the various CMOS parameters changes. Mostly affected parameters are the propagation delay & power consumption. The comparison results clearly show that the Half-Subtractor circuit implemented using AVLS technique gives us the appropriate properties of various parameters helping in obtaining an optimum Half-Subtractor circuit. On designing AVLS technique based Half-Subtractor using 65 nanometer technology, we obtain a very low power consumption circuit, less propagation delay and also with lesser number of routed wires

as compared to the conventional Half-Subtractor circuit. Thus this design is suitable for Low power applications [5].

Table 5.1: Comparison of the conventional Half-Subtractor with the Half-Subtractor incorporated with AVLG and AVLS techniques with 0.65 µm

S. No.	Parameters	Conventi -onal	AVLG	AVLS
1.	Power Consumption(µw)	2.735	2.321	1.622
2.	Routed Wires	23	32	31
3.	Compiled Cells	6 / 6	9 / 9	9 / 9
4.	Layout Area (μm^2)	96	136	128
5.	Propagation Delay (ps)	1.09	0.144	0.131
6.	Leakage Current(mA)	0.919	0.902	0.174
7.	No. of N-MOS and P-MOS transistors	3 , 3	5 ,4	4 , 5

Table 5.2: Comparison of the conventional Half-Subtractor with the Half-Subtractor incorporated with AVLG and AVLS techniques with 0.90 um

S. No.	Parameters	Conven -tional	AVLG	AVLS
1.	Power Consumption (µw)	466	233	67.18
2.	Routed Wires	31	41	13
3.	Compiled Cells	16/16	19/19	19/19
4.	Layout Area (μm^2)	55,002	84,357	180,492
5.	Propagation Delay(ps)	50	35	21
6.	No. of N-MOS and P-MOS transistors	8 , 8	9, 10	10,9

VI. References:

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