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ULTRA LOW VOLTAGE, LOW POWER, LOW AREA, PROCESS VARIATION TOLERANT SCHMITT TRIGGER BASED SRAM DESIGN

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Abstract - **Ultra-low voltage operation of memory cells has become a topic of much interest due to its applications in very low energy computing and communications. However, due to parameter variations in scaled technologies, stable operation of SRAMs is critical for the success of low-voltage SRAMs. It has been shown that conventional 6T SRAMs fail to achieve reliable sub-threshold operation.The Schmitt trigger (ST) based SRAM bit cells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bit cell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bit cell. The ST bit cells incorporate a built-in feedback mechanism, achieving process variation tolerance - a must for future nano-scaled technology nodes.The proposed 8T ST bit cell works under ultra low voltages and consumes negligible power. The area is also optimized and less compared to the previous designs. This circuit exhibit better noise tolerance also. The proposed circuit was implemented in Mentor Graphics Design Architect, Simulated using Mentor Graphics ELDO at various Supply voltages ranging from 5V to 100mV with the help of TSMC 180nm technology. Different back end simulation tools were used to compare the power consumption, noise and layout area of all the circuits and to also study the ability to operate in ultra low voltages.**

Index terms- **Schmitt trigger SRAM,6T SRAM cell,process variation.**

INTRODUCTION

By the analysis of Schmitt-Trigger (ST)-based differential- sensing static random access memory (SRAM) bit cells for ultralow-voltage operation, the ST-based SRAM bit cells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bit cell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bit cell. The proposed ST bit cells incorporate a built-in feedback mechanism, achieving process variation tolerance which is a must for future nano-scaled technology nodes. A detailed comparison of different bit cells shows that the ST-1 , ST-2 and proposed bit cell can operate at lower supply voltages.

POrtable electronic devices have extremely low power requirement to maximize the battery lifetime. Variousdevice-/circuit-/architectural-level techniques have been implemented to minimize the power consumption [1]. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order) [1]. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing minimum-sized transistors [2], [3]. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations.Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics [4]. The combined effect of the lower supply voltage along with the increased process variations may lead to increased memory failures such as read-failure, hold-failure, write-failure, and access-time failure [4]. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling [2].

In a given process technology, the maximum supply voltage (referred to as V_{max}) for the transistor operation is determined by the process constraints such as gate-oxide reliability limits.V_{max} is reducing with the technology scaling due to scaling of gate-oxide thickness. The minimum SRAM supply

voltage, for a given performance requirement (referred to as V_{min}), is limited by the increased process variations (both random and die-to-die) and the increased sensitivity of circuit parameters at lower supply voltage. With the technology scaling, is increasing, and this closes the gap between V_{max} and V_{min}[5].

Hence, to enable SRAM bit cell operation across a wide voltage range, V_{min} has to be further lowered. Various design solutions such as read-write assist techniques and bit cell configurations have been explored. Read-write assist techniques control the magnitude and the duration of different node biases (such as word-lines, bit lines, bit cell VSS node, and bit cell V_{CC} node).

In this case, SRAM V_{min} can be lowered without adding extra transistors to the six–transistor (6T) bit cell. Various bit cell topologies are also proposed to enable low-voltage operation. In this work, focus will be only on various bit cell configurations. I believe that read-write assist circuits can be applied to these bit cell configurations for further V_{min} reduction.

Efficient power management is becoming increasingly important with the rapid growth of portable, wireless, and battery-operated applications. Lowering the supply voltage reduces the dynamic power quadratically and leakage power exponentially. Hence, supply voltage scaling has drawn major attention for the low power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor. However, the remarkable decrease in power consumption at ultralow voltage operation is achievable at the cost of processor performance and circuit robustness under process and temperature variation. As the supply voltage is lowered the sensitivity of the circuit electrical parameters to process variation increases.

Further, the circuit with a lowered voltage becomes more vulnerable to the random noise sources, such as thermal noise and soft error, which are not reduced with supply voltage scaling. As a result, the impact of process variation limits the circuit operation at low supply voltages, particularly memories as well as logic. Further, embedded cache memories are expected to occupy 90% of the total die area of a system-on-a-chip. In order to efficiently address these issues we need an integrated circuit-technology-architectural optimization approach to process resilient IC design.

1.1 PROCESS VARIATION

Process variation is the naturally occurring variation the attributes of transistors (length, widths, oxide thickness) when integrated circuits are fabricated. It becomes particularly important at smaller process nodes as the variation becomes a larger percentage of the full length or width of the device and as feature sizes approaches the fundamental dimensions such as the size of atoms and the wavelength of usable light for patterning lithography masks.

Process variation causes measurable and predictable variance in the output performance of all circuits but particularly analog circuits due to mismatch. If the variance causes the measured or simulated performance of a particular output metric (bandwidth, gain, rise time, etc.) to fall below or rise above the specification for the particular circuit or device it reduces the overall yield for that set of devices.

The first mention of variation in semiconductors was by William Shockley, the co-inventor of the transistor, in his 1961 analysis of junction break down. An analysis of systematic variation was performed by Schemmert and Zimmer in 1974 with their paper on threshold-voltage sensitivity. This research looked into the effect that the oxide thickness and implantation energy had on the threshold voltage of MOS devices. Sources of variations 1) gate oxide thickness 2) random dopant fluctuations 3) Device Geometry, Lithography in nanometer region.

Semiconductor foundries run analyses on the variability of attributes of transistors (length, width, oxide thickness, etc.) for each new process node. These measurements are recorded and provided to customers such as fab-less semiconductor companies. This set of files is generally referred to as "model files" in the industry and are used by EDA tools for simulation of designs.

STATIC RANDOM-ACCESS MEMORY

Static random-access memory (SRAM) is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM (DRAM) which must be periodically refreshed. SRAM exhibits data remanence, but it is still volatile in the conventional sense that data is eventually lost when the memory is not powered.

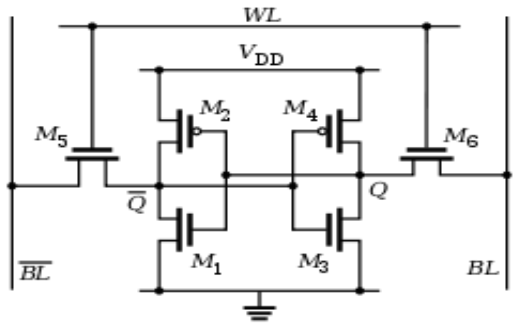


Fig.2.1 CMOS six transistor SRAM cell

A typical SRAM cell is made up of six MOSFETs. Each bit in an SRAM is stored on four transistors (M1, M2, M3, and M4) that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. In addition to such six-transistor (6T) SRAM, other kinds of SRAM chips use 4T, 8T, 10T, or more transistors per bit. Four-transistor SRAM is quite common in stand-alone SRAM devices (as opposed SRAM used for CPU caches), implemented in special processes with an extra layer of polysilicon, allowing for very high-resistance pull-up resistors.

This is sometimes used to implement more than one (read and/or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry.

Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory. Memory cells that use fewer than four transistors are possible but such 3T or 1T cells are DRAM, not SRAM (even the so-called 1T-SRAM).

Access to the cell is enabled by the word line (WL in figure.2.1) which controls the two access transistors M_5 and M_6 which, in turn, control whether the cell should be connected to the bit lines: BL and BL'. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs—in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bit line to swing upwards or downwards. The symmetric structure of SRAMs also allows for differential signaling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time.

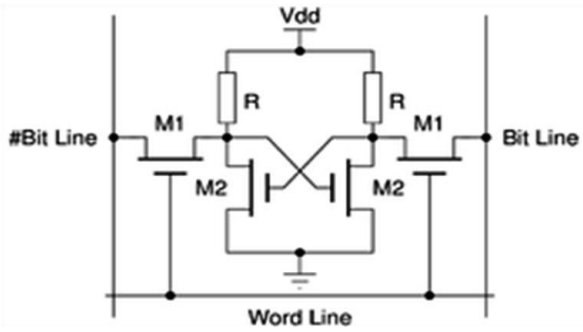


Fig.2.2 A four transistor SRAM cell

By comparison, commodity DRAMs have the address multiplexed in two halves, i.e. higher bits followed by lower bits, over the same package pins in order to keep their size and cost down. The size of an SRAM with m address lines and n data lines is 2^m words, or $2^m \times n$ bits.

2.1 SRAM OPERATION

An SRAM cell has three different states. It can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows.

2.1.1 Standby

If the word line is not asserted, the access transistors M_5 and M_6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by $M_1 - M_4$ will continue to reinforce each other as long as they are connected to the supply.

2.1.2 Reading

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and Q' are transferred to the bit lines by leaving BL at its pre-charged value and discharging BL' through M_1 and M_5 to a logical 0 (i.e. eventually discharging through the transistor M_1 as it is turned on because the Q is logically set to 1). On the BL side, the transistors

M_4 and M_6 pull the bit line toward V_{DD}, a logical 1 (i.e. eventually being charged by the transistor M_4 as it is turned on because Q is logically set to 0). If the content of the memory was a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0. Then these BL and BL will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier, the faster the speed of read operation is.

2.1.3 Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

2.2 CHARACTERISTICS

- SRAM is more expensive, but faster and significantly less power hungry (especially idle) than DRAM.
- It is therefore used where either bandwidth or low power, or both, are principal considerations.
- SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM.
- Due to a more complex internal structure, SRAM is less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.

2.3 CLOCK RATE AND POWER

The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with moderately clocked microprocessors, draws very little power and can have nearly negligible power consumption when sitting idle, in the region of a few micro-watts.

2.4 TYPES OF SRAM

2.4.1 Non-volatile SRAM

Non-volatile SRAMs, or nvSRAMs, have standard SRAM functionality, but they save the data when the power supply is lost, ensuring preservation of critical information. The nvSRAMs are used in a wide range of situations networking, aerospace, and medical, among many others where the preservation of data is critical and where batteries are impractical.

2.4.2 Asynchronous SRAM

Asynchronous SRAM are available from 4 Kb to 64 Mb. The fast access time of SRAM makes asynchronous SRAM appropriate as main memory for small cache-less embedded processors used in everything from industrial electronics and measurement systems to hard disks and networking equipment, among many other applications. They are used in various applications like switches and routers, IP-Phones, IC-Testers, DSLAM Cards, to Automotive Electronics.

2.4.3 Transistor type

- Bipolar junction transistor (used in TTL and ECL) — very fast but consumes a lot of power
- MOSFET (used in CMOS) — low power and very common today

2.4.4 Function type

- Asynchronous — independent of clock frequency; data in and data out are controlled by address transition
- Synchronous — all timings are initiated by the clock edge(s). Address, data in and other control signals are associated with the clock signals

2.4.5 Feature type

- ZBT (ZBT stands for zero bus turn around) — the turnaround is the number of clock cycles it takes to change access to the SRAM from write to read and vice versa. The turnaround for ZBT SRAMs or the latency between read and writes cycle is zero.
- sync Burst (sync Burst SRAM or synchronous-burst SRAM) — features synchronous burst write access to the SRAM to increase write operation to the SRAM
- DDR SRAM — Synchronous, single read/write port, double data rate I/O

- Quad Data Rate SRAM — Synchronous, separate read & write ports, quadruple data rate I/O

2.5 PREVIOUS SRAM BITCELL RESEARCH

Several SRAM bit cells have been proposed having different design goals such as bit density, bit cell area, low voltage operation and architectural timing specifications [6]-[27]. Fig. 1 lists the SRAM bit cells having four to ten transistors. In the four–transistor (4T) loadless bit cell, pMOS devices act as access transistors. The design requirement is such that pMOS OFF state current should be more than the pull-down nMOS transistor leakage current for maintaining data "1" reliably. With increasing process variations and exponential dependence of the sub-threshold current on the threshold voltage, satisfying this design requirement across different process, voltage, and temperature (PVT) conditions may be challenging.

5T bit cell consists of asymmetric cross coupled inverters with a single bit line. Separate bit line pre-charge voltages are used for read and write operations. The intermediate read bit line pre-charge voltage requires a dc–dc converter. Tracking the read pre-charge voltage across PVT corners would require additional design margins in bit cell sizing and may limit its applicability.

A 6T bit cell comprises of two cross-coupled CMOS inverters, the contents of which can be accessed by two nMOS access transistors. The 6T bit cell is the "de facto" memory bit cell used in the present SRAM designs. A single-ended 6T bit cell uses a full transmission gate at one side. Write-ability is achieved by modulating the virtual-VCC and virtual-VSS of one of the inverters.

The single-ended 7T bit cell proposed separately by Tawfik and Suzuki consists of single-ended write operation and a separate read port. Single-ended write operation in this 7T bit cell needs either asymmetrical inverter characteristics or differential VSS/VCC bias. Takeda have proposed another single-ended 7T bit cell in which an extra transistor is added in the pull-down path of one of the inverters. During read mode, the extra transistor is turned OFF, isolating the corresponding storage node from VSS. This results in read-disturb-free operation. In a differential 7T bit cell, the feedback between the two inverters is cut off during the write operation. Successful write operation necessitates skewed inverter sizing, resulting in asymmetrical noise margins.

In a single-ended 8T bit cell, extra transistors are added to the conventional 6T bit cell to separate read and write operation. Liu and Kursun have proposed a 9T bit cell with differential read-disturb-free operation.

In a single-ended 9T bit cell, separate read port is used to decouple read and write operation which is similar to the single-ended 8T bit cell. Stacked read access transistors are used to reduce the bit line leakage. Recently, differential 8T bit cells utilizing RWL/WWL cross-point array and data-dependent VCC have also been reported. Single-ended 10T bit cells are similar to the single-ended 8T bit cell except for the read port configurations. Additional transistors are used to control the read bit line leakage.

Noguchi have proposed a single-ended transmission-gate 10T bit cell .The bit cell contents are buffered using an inverter and then transferred to the read bit line whenever the bit cell is accessed. Use of the transmission gate eliminates domino-style read-bit line sensing. Thus, read bit line does not require pre-charge and keeper transistor. Also, if the accessed data are unchanged, read-bit line toggling is avoided. A differential 10T bit cell with two separate ports for read-disturb- free operation has also been reported. Chang et al. have proposed a read-disturb-free differential 10T bit cell which is suitable for bit-interleaved architecture.

A similar 10T cell with column-assist technique is also reported. However, series-connected write access transistors degrade the write-ability of the bit cell and needs write-assist circuits such as word-line boosting for a successful write operation. In all of the previously reported bit cells, the basic element for the data storage is a cross-coupled inverter pair. Extra transistors are added to decouple the read and write operations. None of the previously reported bit cells incorporate process variation tolerance for improving the stability of the cross coupled inverter pair of an SRAM bit cell operating at ultralow supply voltage.

For successful SRAM operation under PVT variations, the stability of the cross-coupled inverter is important. Traditionally, device sizing has been adopted to mitigate the effect of process variations. However, device sizing is not effective in improving the bit cell stability at very low supply voltage. Hence, we need a different design approach for successful low voltage SRAM design in nano-scaled technologies. In proposed Schmitt Trigger based SRAM bit cell having built-in feedback mechanism that exhibits the process variation tolerance. This

robust process tolerance can be an essential attribute for SRAM scaling into future nano-scaled technology nodes.

SCHMITT TRIGGER (ST) SRAM BITCELLS

In order to resolve the conflicting read versus write design requirements in the conventional 6T bit cell, we apply the Schmitt Trigger (ST) principle for the cross-coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed ST SRAM bit cells, the feedback mechanism is used only in the pull-down path, as shown in Fig.3.1 during 0->1 input transition, the feedback transistor (NF) tries to preserve the logic "1" at output (Vout) node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics.

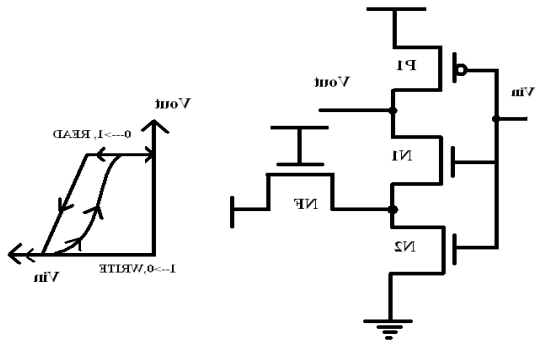


Fig.3.1 Conceptual ST schematics, the gate connection of the feedback transistor is connected to the V_{cc} to show the feedback mechanism during 0->1 input transition.

Since a read-failure is initiated by an input transition 0->1 for the inverter storing logic "1," higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation. For the 1-> 0 input transitions, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bit cell. Two novel bit cell designs are proposed. The first ST-based SRAM bit cell has been presented in our earlier work. Another ST-based SRAM bit cell which further improves the bit cell stability has been reported in. To maintain the clarity of the discussion, the ST bit cell is termed the "ST-1" bit cell .while the other ST bit cell in is termed the "ST-2" bit cell.

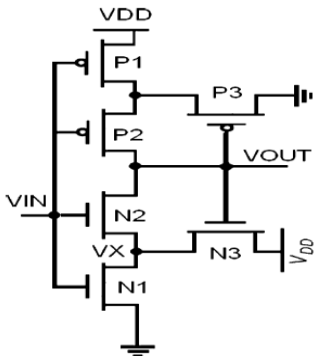


Fig.3.2.Implementation of a Schmitt trigger

To improve the inverter characteristics, Schmitt trigger configuration is used. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition. This adaptation is achieved with the help of a feedback mechanism. One possible implementation of a Schmitt trigger is shown in Fig. 3.2. This structure is used to form the inverter of our memory bit cell. The basic Schmitt trigger requires six transistors instead of two transistors to form an inverter. Thus, it would need 14 transistors in total to form an SRAM cell, which would result in large area penalty. Since pMOS transistors are used as weak pull-ups to hold the "1" state, a feedback mechanism in the pMOS pull-up branch is not used. Feedback mechanism is used only in the pull-down path. The modified Schmitt trigger schematic is shown in Fig.3.3

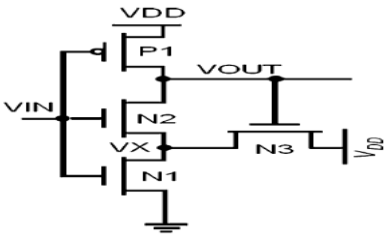


Fig.3.3 Modified Schmitt Trigger

3.1 ST-1 Bit cell

Fig.3.2 shows the schematics of the ST-1 bit cell. The ST-1 bit cell utilizes differential sensing with ten transistors, one word-line (WL), and two bit lines (BL/BR). Transistors PL-NL1-NL2-NFL forms one ST inverter while PR-NR1-NR2-NFR forms another ST inverter. A feedback transistor NFL/NFR raises the switching threshold of the inverter during the 0->1 input transition giving the ST action.

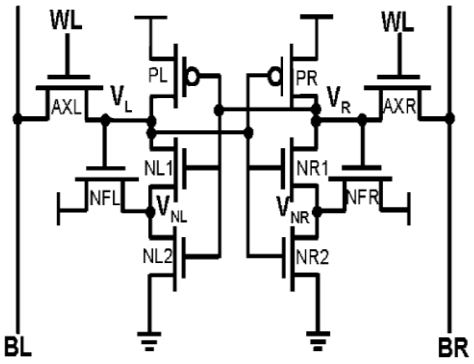


Fig.3.4 ST-1 bit cell

3.2 ST-2 Bit cell

Fig.3.3 shows the schematics of the ST-2 bit cell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bit lines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During the hold-mode, both WL and WWL are OFF. In the ST-2 bit cell, feedback is provided by separate control signal (WL) unlike the ST-1 bit cell, where in feedback is provided by the internal nodes.

In the ST-1 bit cell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback.

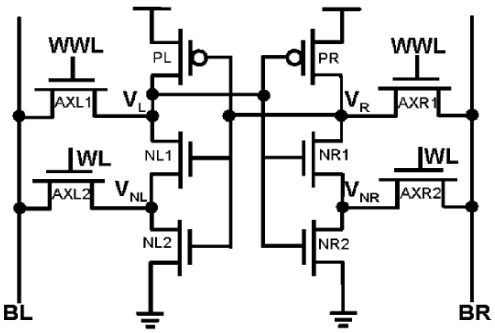


Fig.3.5 ST-2 bit cell

PROPOSED 8T ST BITCELL

A conventional 6TSRAM cell design consists of a cross-coupled inverter pair in Figure 3 (M3-M6) that does data storage and two access transistors (M1-M2) to load/retrieve data on bit lines, BL and BLB. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write operation occurs if the data is correctly latched in the cell. The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation. The bit line (BL) connected to the storage node (V1) storing a „0" gets discharged. The storage node (V1) rises above „0" during a read operation due to voltage division between the access transistor (M1) and the driver transistor (M6). A read failure can occur if the voltage drop rises higher than the threshold voltage of the inverter (M3, M5).A conventional 6T-SRAM cell provides poor read stability since the access transistors provide direct access to the cell storage during a read operation. The proposed design removes the access hazard during a read operation and therefore eliminates the chances of cell content being inadvertently flipped. It consists of a cross-coupled pair (M3-M6) for data storage as in case of a conventional 6T-SRAM cell.

As the Schmitt trigger based designs are having high number of transistors to make the read stability that is 10 Transistors which is comparatively more than the existing 6T SRAM Design. So by combining the mentioned read stability to our work to reduce the area than the previous Schmitt trigger based designs at the same time we will achieve reduced power consumption with reduced transistor count without affecting the read stability. At the same time the proposed design supports separate read and write operations as in the Schmitt Trigger based designs. Idea is to combine these to different technologies & to design a new circuit with much efficiency than the existing two designs.

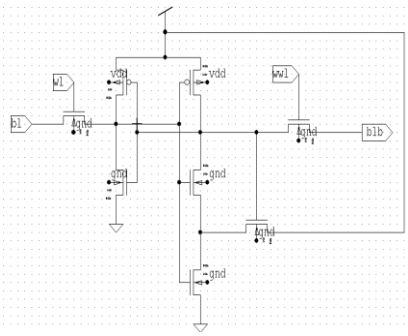
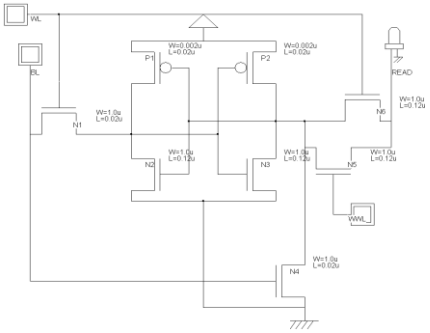


Fig.5.1 Proposed 8T ST Bit cell

The proposed system is an 8T asymmetric Schmitt Trigger bitcell (Figure 5). This bitcell uses single-ended reading and asymmetric inverters, similar to the asymmetric 5T bitcell into improve read margin. By using an asymmetrical design, the trip point of the ST inverter is increased, resulting in higher read stability. Because the 5T bitcell has only one access transistor, write assist methods must be used when trying to write a _1' into the bitcell. The

advantage that this design has over the 5T bitcell is that it is written like a traditional 6T bitcell, which eliminates the need for write assist methods.The WL is pulsed high during both a read and write, and the WWL is only pulsed high during a write.



As the Schmitt trigger based designs are having high number of transistor to make the read stability that is 10 Transistor which very high when compared to the existing 6T SRAM Design we are going to combine the mentioned read stability at the above part to proposed work to reduce the area than the Schmitt trigger based designs at the same time I am going to achieve reduced power consumption with reduced transistor count without affecting the read stability. At the same time the proposed design supports separate read and write operations as in the Schmitt Trigger based designs.My idea is to combine these to different technologies & to design a new circuit with much efficiency than the existing two designs.

In the Proposed Circuit is having one transistor (N4) at the bottom of the circuit connected to the ground directly. This particular transistor is having high (Vth) threshold voltage so that the transistor will be switching ON at high voltages.i.e. whenever voltage fluctuations occur, this transistor will switch ON & dissipate the excess voltage on to the ground. At the same time the transistor at the READline (N5) is used for separating the read operation without disturbing the write line. Thus we are reducing the high voltage &Power dissipation without affecting the working logic. When the Circuit is with normal input voltages the Circuit operates normally providing READ stability, but when the high input voltages are fed, then the excess voltage is dragged by the Transistor N4, providing circuit reliability and READ stability through the Virtual Grounding.

SIMULATION RESULTS

Eldospice simulation tool was used to take the simulation waveforms and 180nm technology was used.Microwind and DSCH was used to get the layout area plots and also the low voltage operation was studied .Ltspice and tanner tools were used to get the power consumption and noise of the circuits.

7.1 Circuit and simulation waveforms

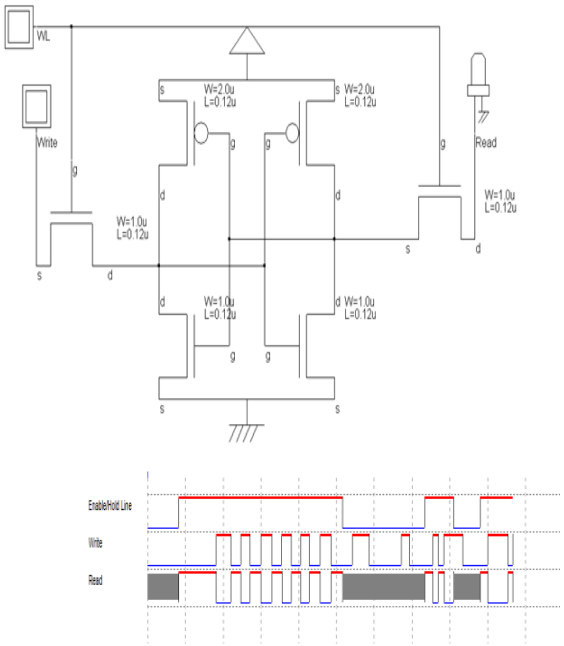
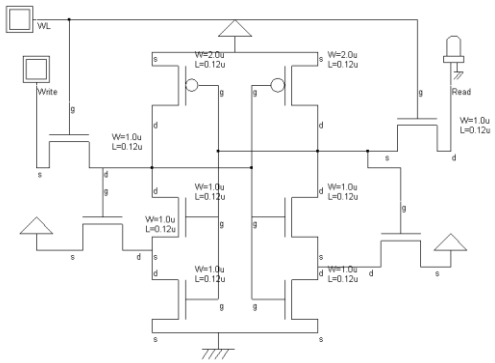


Fig.7.1 Circuit and simulation waveforms for 6T operation



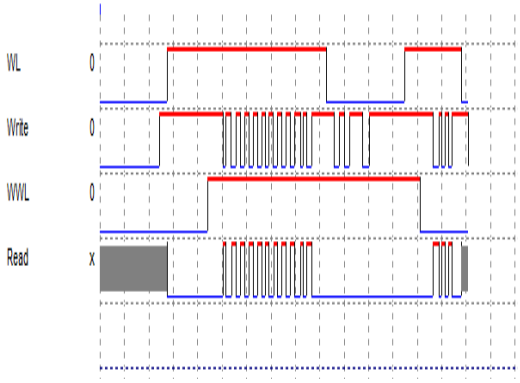


Fig.7.2 Circuit and simulation waveforms for ST1 operation

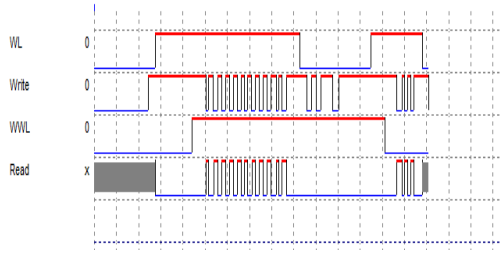
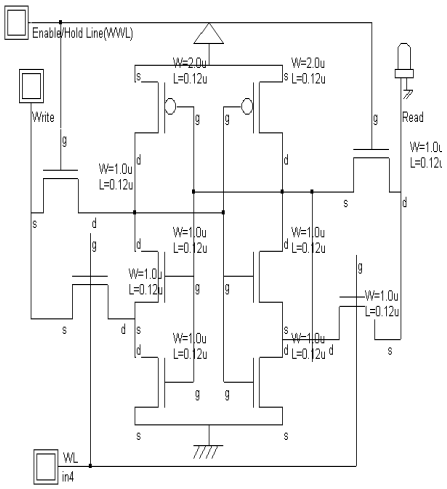


Fig.7.4 circuit and simulation waveforms for 8T ST operation

7. Power Consumption Profiles For The Circuits



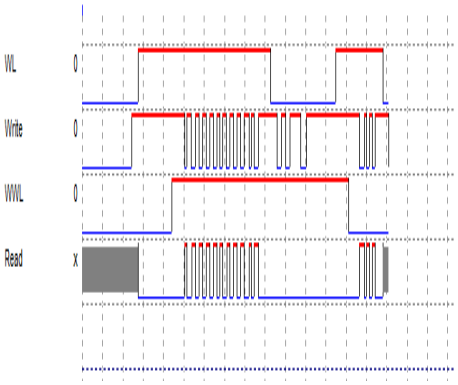


Fig.7.3 circuit and simulation waveforms for ST2 operation

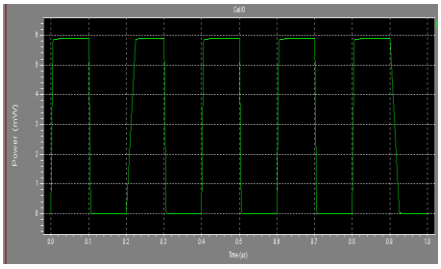


Fig.7.6 Power Consumption Profile For ST1 operation

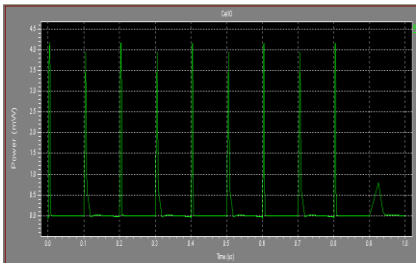


Fig.7.7 Power Consumption Profile For ST2 operation

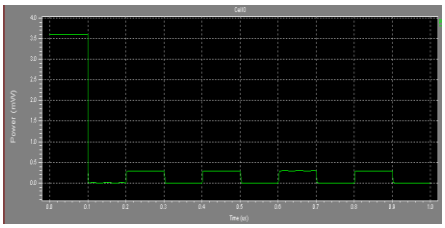


Fig.7.8 Power Consumption Profile For 8T ST Bit cell operation

Comparison of Power Consumption

SRAM CELLS	VDD(5V)
6T SRAM	11.5mw
ST1	5.9 mw
ST2	4.1 mw
8T ST CELL	3.6 mw

Table 7.2 Comparison of Power Consumption

NOISE COMPARISON TABLE

CIRCUIT	NOISE
6T	136.47µV
ST1	5.3µV
ST2	3.4932µV
8T ST cell	903.3nV

Table 7.3 Comparison of Noise in the circuit

7.5 LAYOUT AREA COMPARISONS

Reduction in area

Circuit	Dimension	Area
6T	**43 µm x 88 µm**	**3784 µm^2**
ST1	**37 µm x115 µm**	**4255 µm^2**
ST2	**49 µm x150 µm**	**7350 µm^2**
8T ST	**36µm x 96 µm**	**3456 µm^2**

Table 7.4 Comparison of Layout area

CONCLUSION

Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically. However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases.

Lowering the supply voltage is an effective way to achieve ultra-low-power operation. In the work, evaluation of ST-based SRAM bit cells suitable for ultra-low-voltage applications were be done. The built-in feedback mechanism in the proposed ST bit cell can be effective proposal for process-tolerant, low-voltage SRAM operation in future nano-scaled technologies.

Virtual grounding is used as read assist technique and feedback mechanism is combined to get a low area, low power ,ultra low voltage,process tolerant SRAM cell.

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