

Hardware Implementation of Iris recognition on FPGA: A Selected Review

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Abstract— A biometric system based on the iris recognition is especially an attractive approach for user identification. Implementation of the iris recognition algorithm on FPGA (field programmable gate array) achieving significant reduction in execution time when compared with software implementation. This paper takes a review on selected methods on research of different methods used for Hardware implementation of iris recognition on FPGA. The selection of the paper's dependent on the evaluation of the execution time performance of the proposed iris recognition algorithm when implemented on FPGA.

Index Terms— Biometric, FPGA, Hardware implementation, Iris.

I. INTRODUCTION

The iris recognition is an efficient biometric method for user identification, generally carried out on high-performance microprocessors working at clock frequencies in the range of GHz. However such biometrics application implemented on software restrict to specific markets, because of the microprocessor cost. Devices available in the low-cost consumer market for applications requiring intensive computations are generally too slow. With advances in the VLSI (Very Large Scale Integrated) technology, hardware implementation has become an attractive alternative. The hardware Implementation of these complex computation tasks, by exploiting parallelism and pipelining in algorithms significantly achieve reduction in execution times.

II. REVIEW

Raida Hentati, Moncef Bousselmi, Mohamed Abid[1]: present a HW/SW implementation of algorithm for detection and localization of iris, based on their shape properties & implement the designed system on CCLONE II DE2 BOARD using the NIOS II processor

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Proposed algorithms steps:

- a) The iris localization is done in three steps. The first step is concern with the image preprocessing by average filter in order to reduce noise. In second step the black segmentation is done. In the third step Hough transform technique is deployed to isolate the feature of particular shape within an image.
- b) Now the process of iris recognition is continue with the extraction of code. This phase has two steps. In first step the normalization is done to unwrap the isolated iris part into rectangle, to transform the Cartesian coordinates of iris image to polar coordinates. In second step the encoding is done by Gabor wavelets.
- c) Then the recognition is done by matching the two iris feature by calculating their hamming distance.

The whole system is designed on Cyclone II 2C35 FPGA manufactured by ALTERA which is connected to 8-MB SDRAM, 512-KB SRAM. The image is stored in SRAM. The entire software task is performed by NIOS II. The Hough transform & hamming distance is implemented on FPGA.

Judith Liu-Jimenez, Raul Sanchez-Reillo, Carmen Sanchez-Avila [2]: are developed a different hardware, provide lower processing time with higher security for biometric identification.

Proposed algorithm steps:

- a) Firstly the image of iris is capture by a camera working in infrared light. Then image preprocessing is done to find iris boundaries by Hough transform, and after that image is normalized.
- b) The normalized image is then ready for feature extraction to reduce the image into vector, so that unique features contained in the image are obtained. The Gabor filter is used for feature extraction to reduce the complexity of hardware. According to that, the image is first store in the RAM after preprocessing and then image is translated into polar coordinate. The different section of stretched image is weighted by Gabor filter. The fixed multiplier is used to fix the coefficient. The result obtained after Multiplication is

then integrated for comparison with threshold, to determine 0 or 1 bit.

- c) Xilinx Vertex2 FPGA is used to develop a prototype, having 484 pins to configure as input & output with maximum word length of 242. Among the different verifier like Euclidean distance, Zero-crossing distance and Hamming distance. The hamming distance algorithm is used for matching. To implement these algorithm three different approaches can be applied. In first approach the XOR operation is performed parallel to input vector & then adding is done using adder. In second approach adder is replaced by shift register & counter. And the third approach is based on pipelined structure. The pipelined structure is deployed which reduces the computational time by more than 200%, as the matching processes a word of the feature vector at the same time the feature extraction block is processing the following word, without waiting for the previous block to finish.

K. Grabowski, W. Sankowski, M. Napieralska, M. Zubert, A. Napieralski[3]: are proposed a paper for iris identification based on 2 D Discrete Wavelet Transform which can be optimized for embedded system. In which HAAR wavelet is choose out of Haar and Biorthogonal wavelets because of its easy implementation on fixed point environment. The coefficient of the wavelets is understood as features of iris image. In order to analysis which packet contained more significant information (energy) out of four AHVD packets, the iris image is enhanced by increasing contrast. Where, AHVD (approximation, horizontal, vertical and diagonal details) is basically four decompose part of the image from which next decomposition is performed for each, for energy measurement.

The processed image for feature extraction using DWT method was firstly localized. In which the pupil is segmented first by image thresholding using the histogram analysis. Then morphological operations such as morphological opening & morphological closing are applied for removing reflections and other unwanted elements. The results obtained by pupil segmentation and morphological clearing are easy to achieve in fixed-point environment, therefore can be implemented e.g. in FPGA.

Bethuna[4]: has implemented matching part of iris recognition algorithm on Spartan 3AN FPGA using verilog HDL to achieve reduction in execution time as compare to software based application.

A. Adopted architecture description:

The architecture has four main parts Memory Module, HD modules, Adder tree, Comparator and display which perform their respective operation as follow.

- a) The ROM & RAM memory is used to store the database & live image. The Live image is compared with Database using hamming distance.

- b) The 2048 generated code of iris image is applied to sixteen HD modules. Each HD modules receiving 128 bits as input bits. The 12 bit length output from adder tree, which is the addition of 8 bit output of HD modules is compared with the predetermined threshold value.

- c) The threshold value is set to 30%. For matched irises HD should be less than threshold (HD < threshold).

The whole algorithm steps like Localization, Normalization and Encoding is done using Matlab and the text file of generated templates will be transferred to FPGA using UART cable.

Babasaheb G. Patil, Nikhil Niwas Mane, Shaila Subbaraman[5]: introduce SVD algorithm implemented on hardware architecture to extract feature of iris image. SVD is basically a Singular Value Decomposition algorithm give a set of less than or equal to n values sequenced in descending order for representing the 2D image. Out of which a subset of only first few values are significantly treated as a set of features for that image. The two steps of the complete system image acquisition and image segmentation are implemented on PC system and remaining two steps feature extraction & classifications are implemented on FPGA.

Proposed algorithm steps:

- a) Basically SVD operation factorized an mxn matrix ($m \geq n$) into three other matrices describe by

$$A_{m \times n} = U_{m \times m} \cdot S_{m \times n} \cdot V_{n \times n}^T \quad (1)$$

{Where T denotes transpose, U is an mxm orthogonal left unitary matrix, V is an nxn orthogonal right unitary matrix and S is an mxn diagonal The S matrix is unique then A matrix. The dimension of input matrix mxn is reducing to vector of n elements that is because of the Matrix element of S is zero everywhere except in the main diagonal}.

- b) Out of the n elements only the first k elements, when arranged in descending order, contain substantial information, and the vector tail without significant loss of information can be cropped out, leading to further reduction in the dimension of the vector representing 2- D mxn matrix.

- c) After that the jacobi rotations on A iteratively derived U & V

$$S_{m \times n} = U_{m \times m}^T \cdot A_{m \times n} \cdot V_{n \times n} \quad (2)$$

- d) The modified iterative form is

$$A^{i+1} = J^{iT} \cdot A^i \cdot J^i \quad (3)$$

The off diagonal elements of the iterated matrix A tend to zero as the. Iteration number (i) tends to infinity .The singular values of the original matrix A are then obtained by taking the square root of diagonal elements of the transformed matrix.

B. SVD Core description:

Matrix Multiplier, Jacobi Transformer, Finite State Machine, Reorder Unit and Square Root block are the major components of SVD core. The function of each component is as follow.

a) Matrix Multiplexer used to select appropriate input matrix

by which in first step image matrix is selected, in second step J^T is selected and in third step C & J are selected. The outputs of this unit are multiplexed to Jacobi transformer to generate

Jacobi matrix by operating on A and selecting pivot element by tournament ordering method.

b) Finite State Machine generates the control signals for various operations carried out.

c) Reorder Matrix block implements sequential search algorithm to arrange the diagonal element in descending order.

III COMPARATIVE ANALYSIS OF RESEARCH WORK

S.NO.	Author/Research Study-Year	Title	Technology/ Methods	Results/Conclusion
1.	Raida Hentati, Moncef Bousselmi, Mohamed Abid - IEEE 2010	An Embedded System for iris Recognition	Implemented the Designed system on CYCLONE II DE2 Board using the NIOSII Processor(HW/SW implementation)	Hough transform and Hamming distance are implemented in FPGA. Which present the high performance, reliability & speed.
2.	Judith Liu-Jimenez, Raul Sanchez-Reillo, Carmen Sanchez-Avila - IEEE 2005	Full Hardware solution for processing iris biometric	Gabor filter is used for feature extraction & used pipelined architectures for hardware system	This paper introducing pipeline structure for hardware & Processing time is reduced 80% but Within the feature extraction block performance is worse than the Software.
3.	K. Grabowski, W. Sankowski, M. Napieralska, M. Zubert, A. Napieralski- IEEE 2006	Iris Recognition Algorithm Optimized for Hardware Implementation	This paper proposed iris identification based on 2 D Discrete Wavelet Transform which can be optimized for embedded system	In this image in database does not have any eyelids or eyelashes Inside iris area & do not have any disturbances in iris pattern.
4.	Buethna- IJSR 2012	Hardware Implementation of Iris Matching	Implemented matching part of iris recognition algorithm on Spartan 3AN FPGA	This method achieving significant reduction in execution time as compared with conventional software based applications.

5.	Babasaheb G. Patil, Nikhil Niwas Mane, Shaila Subbaraman-IJECE 2012	Iris Feature Extraction and Classification using FPGA	Implemented SVD algorithm by hardware architecture to extract feature of iris image.	The result for SVD value in matlab & FPGA is very close. The iris is identified in less than 250 μ s.
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d) And square root block implements non-restoring type method to compute square root of diagonal elements which are primary outputs of SVD core.

The hamming classifier is used to compute simple hamming distance between SVD values of the test image with pre-stored values of all images one by one.

IV CONCLUSION

Selected surveys on research work of iris recognition techniques/method are presented in this paper. The research in the area of iris recognition techniques in these research papers are critically reviewed and reported for the benefit of researchers in this field. The iris recognition techniques are developed from last few years to reduce frauds and to make the facilities more secure. Basically the iris recognition is based on biometric characteristics of users that they possess, so that's why it is more securing than the traditional ID or password methods for user authentication.

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