

An Efficient MRC based RNS-to-Binary Converter for the $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$ Moduli Set

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Abstract— In this paper, we suggest the moduli set $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$ as an alternative candidate to the moduli set $\{2^{n+1}, 2^n-1, 2^n, 2^{2n+1}-1\}$, which contains a relatively long delay modulus 2^{n+1} . Subsequently, we propose an efficient reverse converter, based on Mixed Radix Conversion, for the moduli set $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$. When compared to the best known equivalent state of the art reverse converter, the proposed converter is about $3nFA$ s and $(n+1)t_{FA}$ better in terms of area cost and conversion time, respectively, where FA and t_{FA} represent Full Adder and delay of 1 Full Adder, respectively. Consequently, the proposed scheme outperforms existing similar lesser dynamic range 3-moduli sets in terms of area cost while it outperforms the state of the art 4-moduli set from which it was derived, in terms of both area cost and conversion time.

Index Terms—Residue Number System, Reverse Converter, Multiplicative Inverses, Chinese Remainder Theorem.

I. INTRODUCTION

Residue Number System (RNS) offers very high speed concurrent operations in addition and multiplication dominated digital signal processing applications. This is because RNS supports carry free addition, borrow free subtraction, and digit by digit multiplication without partial product. However, RNS has not found a widespread usage in general purpose computing due to the following difficult RNS arithmetic operations: overflow detection, magnitude comparison, sign detection, moduli selection, and both reverse and forward conversions. Out of these numerous RNS challenges, moduli selection and reverse conversion are the two most critical issues [1],[7],[17].

Many interesting reverse converters have been proposed for many moduli sets such as $\{2^n, 2^n-1, 2^n+1\}$ [18], $\{2^n, 2^{2n}-1, 2^{2n}+1\}$ [9], $\{2^n, 2^n-1, 2^{n-1}-1\}$ [8], $\{2n+1, 2n-1, 2n\}$ [3], [5], $\{2n+2, 2n+1, 2n\}$ [4], $\{2^{n+1}+1, 2^{n+1}-1, 2^n\}$ [12], $\{2^{n+1}-1, 2^n, 2^n-1\}$ [11], [14], [6], $\{2^n-1, 2^n, 2^{2n+1}-1\}$ [2], [15], $\{2^n, 2^{2n}-1, 2^{2n+1}-1\}$ [10], $2n-1, 2n, 2n+1, 2^{2n+1}-1$ [13], $2n-1, 2n, 2n+1, 2^{2n+1}-1$ [13], to mention just a few.

The 4-moduli set $\{2^n-1, 2^n, 2^n+1, 2^{2n+1}-1\}$ was recently proposed in [13]. Even though the computation time of all the operations of the processor corresponding to the modulus $2^{2n+1}-1$ will be higher than that of 2^n+1 , the modulus 2^n+1 should be avoided because 2^n+1

modulus is not as simple as circular left shift in 2^n-1 modulus and this degrades the entire RNS architecture. The major disadvantage of the moduli set $\{2^n-1, 2^n, 2^n+1, 2^{2n+1}-1\}$ is that it is unbalance.

In this paper, we combine the moduli 2^n+1 and 2^n-1 into one from the 4-moduli set $\{2^n-1, 2^n, 2^n+1, 2^{2n+1}-1\}$ [13] in order to obtain the 3-moduli set $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$. This choice, with smaller conversion time, evidently achieves the same dynamic range as the moduli set $\{2^n-1, 2^n, 2^n+1, 2^{2n+1}-1\}$ [13]. Subsequently, we propose an efficient Mixed Radix Conversion (MRC) RNS-to-binary converter for the moduli set $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$. When compared to the converter proposed in [13], the proposed converter is about $3nFA$ s and $(n+1)t_{FA}$ better in terms of area cost and conversion time, respectively, where FA and t_{FA} represent Full Adder and delay of 1 Full Adder, respectively. Consequently, the proposed scheme outperforms the one in [13] in terms of both delay and area cost. Additionally, the proposed converter requires less area cost when compared to lesser dynamic range similar state of the art reverse converters proposed in [2] and [15].

The rest of the article is organized as follows: Section II presents the proposed algorithm. In section III, we present the hardware realization of the proposed algorithm and a comparison with the state of the art reverse converters is provided in Section IV. The paper is concluded in Section V.

II. PROPOSED ALGORITHM

In this section, a two-level residue-to-binary conversion algorithm for the moduli set $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$ is presented. The first level combines the first and the second residues with respect to the subset $\{2^n, 2^{2n}-1\}$. The second level combines the third residue with the first level with regard to the composite moduli set $\{2^n(2^{2n}-1), 2^{2n+1}-1\}$.

First, we wish to show that the moduli $2^{2n}-1, 2^n$, and $2^{2n+1}-1$ are relatively.

Theorem 1: The moduli set $\{2^{2n}-1, 2^n, 2^{2n+1}-1\}$ contains pairwise relatively prime moduli.

Proof: From Euclidean theorem, we have:

$$\gcd(a, b) = \gcd(b, |a|_b),$$

therefore,

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$$\begin{aligned} \gcd(2^{2n} - 1, 2^n) &= \gcd(2^n, |2^{2n} - 1|_{2^n}) \\ &= \gcd(2^{2n}, -1) = 1 \end{aligned}$$

Also,

$$\begin{aligned} \gcd(2^{2n+1} - 1, 2^{2n} - 1) &= \gcd(2^{2n} - 1, |2^{2n+1} - 1|_{2^{2n-1}}) \\ &= \gcd(2^{2n} - 1, 1) = 1 \end{aligned}$$

Again,

$$\begin{aligned} \gcd(2^{2n+1} - 1, 2^n) &= \gcd(2^n, |2^{2n+1} - 1|_{2^n}) \\ &= \gcd(2^n, 1) = 1 \end{aligned}$$

Thus, the moduli $\{2^{2n} - 1, 2^n, 2^{2n+1} - 1\}$ relatively prime since all the greatest common divisors are equal to 1. ■

Theorem 2: For the moduli set $\{2^{2n} - 1, 2^n, 2^{2n+1} - 1\}$, the followings hold true:

$$|(2^n)^{-1}|_{2^{2n-1}} = 2^n, \tag{1}$$

$$|(2^n(2^{2n} - 1))^{-1}|_{2^{2n+1-1}} = 2^{2n+1} - 2^{2n+2} - 1, \tag{2}$$

Proof: If it can be demonstrated that $|(2^n)^{-1}|_{2^{2n-1}} = 2^n$, then 2^n is the multiplicative inverse of 2^n with respect to $2^{2n+1} - 1$. $|(2^n)^{-1}|_{2^{2n-1}}$ is given by:

$|2^{2n}|_{2^{2n-1}} = 1$, thus (1) holds true.

In the same way if $|(2^n(2^{2n} - 1))^{-1}|_{2^{2n+1-1}} = 2^{2n+1} - 2^{2n+2} - 1$, thus $(2^n(2^{2n} - 1))$ is the multiplicative inverse of 2^n with respect to $2^{2n+1} - 1$. $|(2^n(2^{2n} - 1))^{-1}|_{2^{2n+1-1}}$ is given by:

$$\begin{aligned} |(2^n(2^{2n} - 1))^{-1}|_{2^{2n+1-1}} &= |1|_{2^{2n+1-1}} = 1, \text{ thus (2) holds true.} \end{aligned}$$

The following MRC algorithm and properties are needed for the derivation of the RNS-to-binary converter:

Suppose that we have a residue number $(x_1, x_2, x_3, \dots, x_n)$ for the moduli set $\{m_1, m_2, m_3, \dots, m_n\}$ and a set of digits $\{a_1, a_2, a_3, \dots, a_n\}$, which are the Mixed Radix Digits (MRDs). The decimal equivalent X of the residues can be computed as follows [16]:

$$\begin{aligned} X &= a_1 + a_2 m_1 + a_3 m_1 m_2 + \dots + a_n m_1 m_2 m_3 \dots m_{k-1} \tag{3} \end{aligned}$$

where the MRDs are given as follows:

$$\begin{aligned} a_1 &= x_1 \\ a_2 &= |(x_2 - a_1)|_{m_1^{-1}}|_{m_2}|_{m_2} \\ a_3 &= |((x_3 - a_1)|_{m_1^{-1}}|_{m_3} - a_2)|_{m_2^{-1}}|_{m_3}|_{m_3} \\ &\vdots \\ a_k &= \left| \left((x_k - a_1)|_{m_1^{-1}}|_{m_k} - \right. \right. \\ &\quad \left. \left. a_2|m_2-1|mk-\dots-ak-1|mk-1-1|mkmk \right. \right. \end{aligned} \tag{4}$$

Property 1: Modulo $(2^s - 1)$ multiplication of a residue number by 2^t , where s and t are positive integers, is equivalent to t bit circular left shifting.

Property 2: Modulo $(2^s - 1)$ of a negative number is equivalent to the one's complement of the number, which is obtained by subtracting the number $(2^s - 1)$.

For the considered moduli set $\{2^n, 2^{2n} - 1, 2^{2n+1} - 1\}$ with the corresponding residues (x_1, x_2, x_3) , let the binary representations of the residues be:

$$x_1 = (x_{1,n-1}x_{1,n-2} \dots x_{1,1}x_{1,0}) \tag{5}$$

$$x_2 = (x_{2,2n-1}x_{2,2n-2} \dots x_{2,1}x_{2,0}) \tag{6}$$

$$x_3 = (x_{3,2n}x_{3,2n-1} \dots x_{3,1}x_{3,0}) \tag{7}$$

Now, let us consider the moduli set $\{2^n, 2^{2n} - 1\}$ and $Z_1 = (x_1, x_2)$. Using the MRC algorithm, given by (3), for the two moduli set $\{2^n, 2^{2n} - 1\}$ and making use of (1), we have:

$$\begin{aligned} z_1 &= a_1 + a_2 m_1 \\ &= x_1 + 2^n | |(2^n)^{-1}|_{2^{2n-1}}(x_2 - x_1)|_{2^{2n-1}} \\ &= x_1 + 2^n | 2^n(x_2 - x_1)|_{2^{2n-1}} \end{aligned} \tag{8}$$

Let

$$z_2 = x_2 - x_1 \tag{9}$$

Note that x_2 is a $2n$ bit number while x_1 is an n bit number. In order to add x_2 and \bar{x}_1 , x_1 must be converted to a $2n$ bit number, which is given by:

$$\begin{aligned} x_1 &= \underbrace{(00 \dots 0)}_n \underbrace{(x_{1,n-1}x_{1,n-2} \dots x_{1,1}x_{1,0})}_n \\ \bar{x}_1 &= \underbrace{(11 \dots 1)}_n \underbrace{(x_{1,n-1}x_{1,n-2} \dots x_{1,1}x_{1,0})}_n \end{aligned} \tag{10}$$

Using property 1, z_1 can be simplified. Supposed that:

$$z_1 = a_1 + a_2 z_3 \tag{11}$$

where

$$\begin{aligned} z_3 &= |2^n z_2|_{2^{2n-1}} \\ &= \left| 2^n \underbrace{z_{2,2n-1} \dots z_{2,n+1}x_{2,n}}_n \underbrace{z_{2,n-1} \dots z_{2,1}x_{2,0}}_n \right|_{2^{2n-1}} \\ &= \underbrace{z_{2,n-1} \dots z_{2,1}z_{2,0}}_n \underbrace{z_{2,2n-1} \dots z_{2,n+1}z_{2,n}}_n \end{aligned} \tag{12}$$

Note that z_1 in (11) can be achieved by a shift and concatenation operation. Thus z_1 is a $3n$ bit number and can be represented as:

$$z_1 = \underbrace{z_{2,n-1} \dots z_{2,0}}_n \underbrace{z_{2,2n-1} \dots z_{2,n}}_n \underbrace{x_{1,n-1}x_{1,0}}_n \tag{13}$$

Next, consider the composite moduli set $\{2^n(2^{2n} - 1), 2^{2n+1} - 1\}$ and let $X = (z_1, x_3)$. Using the MRC algorithm, given by (3), for the two moduli set $\{2^n(2^{2n} - 1), 2^{2n+1} - 1\}$, X can be computed as:

$$X = z_1 + 2^n(2^{2n} - 1)z_4 \tag{14}$$

where

$$z_4 = |z_5(x_1 - z_1)|_{2^{2n+1-1}} \tag{15}$$

From (2), z_5 is given by:

$$\begin{aligned} z_5 &= |(2^n(2^{2n} - 1))^{-1}|_{2^{2n+1-1}} \\ &= 2^{2n+2} - 2^{n+2} - 1 \end{aligned} \tag{16}$$

Using (16) and (11), (15) can be written as:

$$z_4 = |(2^{2n+2} - 2^{n+2} - 1)(x_1 - z_1)|_{2^{2n+1-1}}$$

$$\begin{aligned}
&= |-2^{n+2}(x_1 - z_1)|_{2^{2n+1}-1} \\
&= |-2^{n+2}(x_3 - x_1 - 2^n z_3)|_{2^{2n+1}-1} \\
&= |-2^{n+2}x_3 + 2^{n+2}x_1 + 2^n(2^{2n+1})z_3|_{2^{2n+1}-1} \\
&= |-2^{n+2}x_3 + 2^{n+2}x_1 + 2z_3|_{2^{2n+1}-1} \quad (17)
\end{aligned}$$

Let

$$z_4 = |u_1 + u_2 + u_3|_{2^{2n+1}-1}, \quad (18)$$

where

$$u_1 = -2^{n+2}x_3, u_2 = 2^{n+2}x_1, u_3 = 2z_3.$$

u_1, u_2 and u_3 can be simplified using properties 1 and 2 as follows:

$$\begin{aligned}
u_1 &= \left| -2^{n+2} \underbrace{(x_{3,2n} \dots x_{3,1} x_{3,0})}_{2^{n+1}} \right|_{2^{2n+1}-1} \\
&= \left| -2^{n+2} \underbrace{(x_{3,2n} \dots x_{3,n-1})}_{n+2} \underbrace{(x_{3,n-2} \dots x_{3,0})}_{n-1} \right|_{2^{2n+1}-1} \\
&= \underbrace{(\bar{x}_{3,n-2} \dots \bar{x}_{3,0})}_{n-1} \underbrace{(\bar{x}_{3,2n} \dots \bar{x}_{3,n-1})}_{n+2} \quad (19)
\end{aligned}$$

$$\begin{aligned}
u_2 &= \left| 2^{n+2} \underbrace{(x_{1,n-1} \dots x_{1,1} x_{1,0})}_n \right|_{2^{2n+1}-1} \\
&= \left| 2(2^{n+1}) \underbrace{(x_{1,n-1} \dots x_{1,0})}_n \right|_{2^{2n+1}-1} \\
&= \left| 2 \underbrace{(x_{1,n-1} \dots x_{1,0})}_n \underbrace{00 \dots 0}_{n+1} \right|_{2^{2n+1}-1} \\
&= \underbrace{(x_{1,n-2} \dots x_{1,0})}_{n-1} \underbrace{00 \dots 0}_{n+1} \underbrace{x_{1,n-1}}_1, \quad (20)
\end{aligned}$$

$$\begin{aligned}
u_3 &= \left| 2 \underbrace{(z_{3,n-1} \dots z_{2,0})}_n \underbrace{z_{2,2n-1} \dots z_{2,n}}_n \right|_{2^{2n+1}-1} \\
&= \underbrace{(z_{3,n-1} \dots z_{2,0})}_n \underbrace{z_{2,2n-1} \dots z_{2,n}}_n \underbrace{0}_1. \quad (21)
\end{aligned}$$

Now, let (14) be represented as

$$X = B + C, \quad (22)$$

where

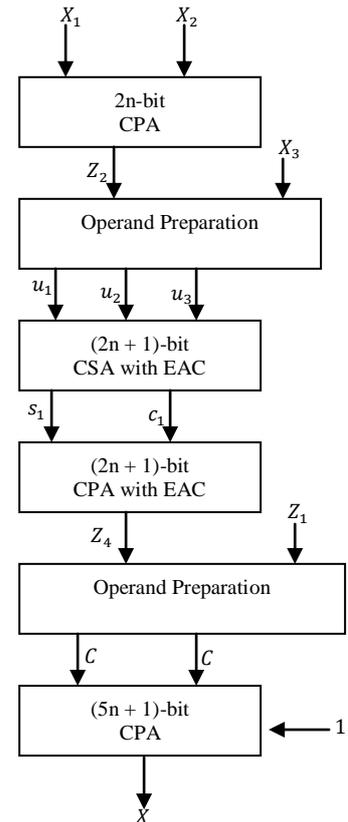
$$\begin{aligned}
B &= z_1 + 2^{3n}z_4 \\
&= \underbrace{z_{1,3n-1} \dots z_{1,0}}_{3n} + \underbrace{z_{4,2n} \dots z_{4,0}}_{2n+1} \underbrace{00 \dots 0}_{3n} \\
&= \underbrace{z_{4,2n} \dots z_{4,0}}_{2n+1} \underbrace{z_{1,3n-1} \dots z_{1,0}}_{3n}, \quad (23)
\end{aligned}$$

$$\begin{aligned}
C &= -2^n z_4 \\
&= -(\underbrace{00 \dots 0}_{2n} \underbrace{z_{4,2n} \dots z_{4,0}}_{2n+1} \underbrace{00 \dots 0}_n) \\
&= (\underbrace{11 \dots 1}_{2n} \underbrace{\bar{z}_{4,2n} \dots \bar{z}_{4,0}}_{2n+1} \underbrace{11 \dots 1}_n). \quad (24)
\end{aligned}$$

III. HARDWARE REALIZATION

The hardware implementation of the proposed reverse converter is based on (9), (18), and (22). The proposed RNS-binary converter is depicted by Figure 1. In the figure, x_2 and \bar{x}_1 are added using a Carry Propagate

Adder (CPA). Since there are n bits of '1's, n bits Half Adders (HAs) and n bits Full Adders (FAs) can be utilized in order to reduce the area cost. The variables u_1, u_2 and u_3 are added by a Carry Save Adder (CSA) with an End-Around Carry (EAC) producing the values s_1 and c_1 . These values must be added $2^{2n+1} - 1$ to obtain z_4 , i.e., a CPA with EAC. The CSAs contain $(n + 2)$ bits HAs and $(n - 2)$ bits of '0's. Thus, the area cost can also be reduced by employing $(n + 2)$ bits HAs and $(n - 2)$ bits FAs. The final result is obtained by adding B and C, given by (22), using a CPA with "1" carry in. it should be noted that B is a $(5n + 1)$ bit number and for C to be added to B, it must also be converted to a $(5n + 1)$ bit number. In order to do this, 1's are appended to the result of complementations, as given in (24). Since there $3n$ bits of 1's, the area cost can be further reduced by using $3n$ bits of HAs and $(2n + 1)$ of FAs. In Figure 1 above, there three CPAs with the following delays: $4nt_{FA}$, $(4n + 2)t_{FA}$, and $(5n + 1)t_{FA}$ bits. This implies that the proposed design requires $(5n + 2)$ HAs and $(6n + 1)$ area cost with a conversion time of $(13n + 4)$.



IV. PERFORMANCE EVALUATION

The performance of the proposed converter is evaluated in terms of area cost and conversion delay. The theoretical analysis result is presented in Table 1. We note that for reverse converters with different moduli sets to be fairly compared, the moduli sets should provide the same dynamic range and also rely on the same arithmetic unit speed [15]. The converters presented in [2], [15], and the proposed converters are for moduli sets that rely on similar

arithmetic unit speed. While the converters [15] and [2] are for $4n$ -bits dynamic range moduli sets, the proposed converters is for $5n$ -bits dynamic range moduli set. Thus, comparing the performances of the proposed converter with the ones in [15] and [2] is not very appropriate. The performances of the converters [15 and [2] have been included in Table 1 to show that the proposed converter, with larger dynamic range, can compete favourably with the existing similar 3-moduli set converters.

Since the proposed converter and the one for the moduli set $\{2^n, 2^n - 1, 2^n + 1, 2^{2n+1} - 1\}$ in [13] enjoy the same dynamic range, we compare their performances in terms of area and delay. From Table 1, it can be seen that the proposed converter outperforms the one in [13], from which it was derived, in terms of both area cost and conversion time.

It should be note that apart from RNS to binary conversion speed and cost advantages, efficient internal RNS

arithmetic circuits and efficient binary-to-RNS converter can easily be developed for the considered moduli set.

V. CONCLUSIONS

In this paper, we proposed an efficient MRC based RNS-to-binary converter for a new three-moduli set $\{2^{2n} - 1, 2^n, 2^{2n+1} - 1\}$ derived from the four-moduli set $\{2^n, 2^n - 1, 2^n + 1, 2^{2n+1} - 1\}$ presented in [13] by combining $2^n - 1$ and $2^n + 1$ into $2^{2n} - 1$. When compared to the converter proposed in [13], the proposed converter is about $3nFA$ s and $(n + 1)t_{FA}$ better in terms of area cost and conversion time, respectively. Consequently, the proposed scheme outperforms the one in [13] in terms of both delay and area cost. Additionally, the proposed converter requires less area cost when compared to lesser dynamic range similar state of the art reverse converters proposed in [2] and [15].

Table 1: AREA-DELA COMPARISON

Converter	[15]	[2]	[13]	Proposed Converter
Dynamic Range	$4n$ -bits	$4n$ -bits	$5n$ -bits	$5n$ -bits
FA	$9n + 2$	$9n + 2$	$10n + 4$	$6n + 1$
HA	$2n + 2$	$5n + 4$	$3n - 2$	$5n + 2$
Delay	$(10n + 5)t_{FA}$	$(7n + 7)t_{FA}$	$(14n + 5)t_{FA}$	$(13n + 4)t_{FA}$

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