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A Survey of Metastability Errors in CMOS Digital Circuits

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Abstract— **Recent advances in complementary metal oxide semiconductor (CMOS) technology have led to unparalleled levels of integration in digital logic systems. By and large, these digital logic systems require a clock to synchronize signals and ensure proper operation. Due to the path propagation delay and clock synchronization setup hold time failure errors are occurs in digital circuits. Depending upon the application, the errors are described by a number of different terms including "synchronization failure," "arbitration error," and "metastability error." The underlying mechanism for all of these problems is the same, and of these terms, "metastability error" is the most general because it describes the failure of the element within the circuit and not the application. Metastability is a widespread phenomenon and errors may occur in any synchronous circuit where an input signal can change randomly with respect to a reference signal. The reference signal may be either a voltage based reference, such as a bias voltage, or a time based reference, such as a clock signal.**

***Index Terms*— CMOS, metastability, setup & hold time, synchronization.**

I. INTRODUCTION

In synchronous digital logic systems, asynchronous external signals must be referenced to the system clock or synchronized. Synchronization of asynchronous signals, however, inevitably leads to metastability errors. Metastability error rates can increase by orders of magnitude as clock frequencies increase in high performance designs, and supply voltages decrease in low-power designs. This research focuses on the characterization of metastability parameters and error reduction with no penalty in circuit performance. Two applications, high-speed flash analog-to-digital conversion and synchronization of asynchronous binary signals in application-specific integrated circuits have been investigated. Recent advances in complementary metal oxide semiconductor (CMOS) technology have led to unparalleled levels of integration in digital logic systems. By and large, these digital logic systems require a clock to synchronize signals and ensure proper operation.

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However, in practical applications, digital systems must communicate with the outside world or other systems. This requires external signals asynchronous to the clocked system to be converted to signals the clocked digital system can understand. The requirement for synchronous systems is that all circuits required to respond to an input uniformly agree on the binary value of the input. In many applications, however, due to the nature of one or more of the external inputs, the input requirements for the synchronous circuit will be violated, and errors will result. Depending upon the application, the errors are described by a number of different terms including "synchronization failure," "arbitration error," and "metastability error." The underlying mechanism for all of these problems is the same, and of these terms, "metastability error" is the most general because it describes the failure of the element within the circuit and not the application.

Metastability is a widespread phenomenon and errors may occur in any synchronous circuit where an input signal can change randomly with respect to a reference signal. The reference signal may be either a voltage based reference, such as a bias voltage, or a time based reference, such as a clock signal. Circuits in which metastability can occur include analog-to-digital converters, memories, time digitizers, and bus controllers etc.[1],[2].

II. METASTABILITY

Whenever there are setup and hold time violations in any flip-flop, it enters a state where its output is unpredictable, this state is known as metastable state (quasi stable state); at the end of metastable state, the flip-flop settles down to either '1' or '0'. This whole process is known as metastability. In the figure below T_{su} is the setup time and T_h is the hold time. Whenever the input signal D does not meet the T_{su} and T_h of the given D flip-flop, metastability occurs.

We study metastability using regenerative circuit, A regenerative circuit is a circuit with two stable states. The stable states are arbitrarily called one and zero. The regenerative circuit can be forced into either of these two states provided the circuit inputs meet some timing and voltage requirements. If the inputs are not sufficient to unambiguously define either a one or zero, the circuit will become metastable, and the final state is not deterministic.

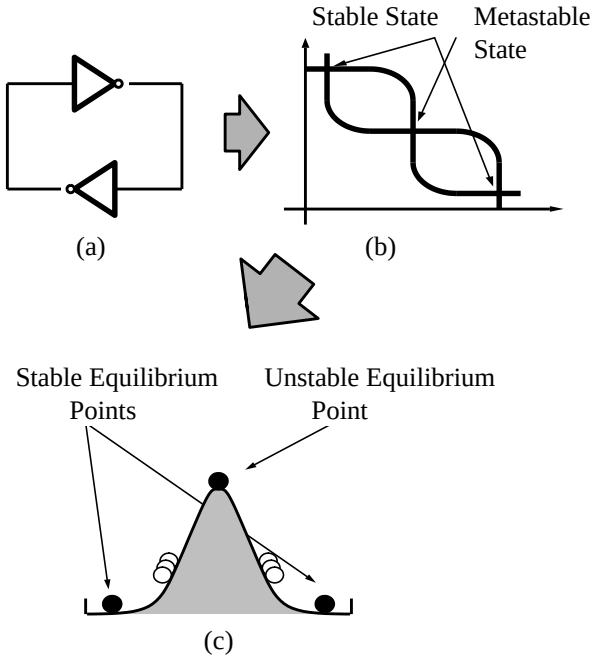

Figure 1: Mechanical analogy for metastable state. (a) Regenerative circuit; (b) load line representation; (c) mechanical analogy

The circuits required to respond to a metastable regenerative circuit may not agree on the value, leading to intermittent errors posing reliability problems.

Figure 1 shows a conceptual view of the metastability problem in regenerative circuits. The simplest regenerative circuit is shown in (a), two cross-coupled inverting gain stages shown here as inverters. Possible operating points for the circuit are represented with the load line intersection points in (b) on the right hand side of the figure. The center intersection point in the load line plot is the circuit's operating point which corresponds to the ball on the hill's energy maximum and is an unstable operating point. However, in passing from one state to another, there is inevitably an energy maximum. The two stable states are near the positive and negative supply. Eventually the circuit will exit the unstable operating point due to noise, but the amount of time spent in the state is not well controlled.[5]

The circuit remaining in the metastable state can be modeled conceptually as a ball on a hill as shown in Figure 1. The two stable states of the system correspond to the valleys, or stable equilibrium points, on either side of the hill [4]. If the ball is placed in either location, it will remain there indefinitely. However, if the ball is placed at the very top of the hill, it will remain there indefinitely, even though this is not an energy minimum. This is termed an unstable equilibrium point. If the ball is displaced to the left or right, it will quickly find one of the stable states. A metastable circuit operates in much the same manner. However, to characterize the circuit, the rate of entering the metastable state and the escape mechanism must be characterized. In addition, the distance that the ball must be displaced from the energy maximum before the location can be unequivocally declared in the left hand valley or the right hand valley must be ascertained.

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If we look deep inside of the flip-flop we see that the quasi-stable state is reached when the flip-flop setup and hold times are violated. Assuming the use of a positive edge triggered "D" type flip-flop, when the rising edge of the flip-flop clock occurs at a point in time when the D input to the flip-flop is causing its master latch to transition, the flip-flop is highly likely to end up in a quasi-stable state. This rising clock causes the master latch to try to capture its current value while the slave latch is opened allowing the Q output to follow the "latched" value of the master. The most perfectly "caught" quasi-stable state (on the very top of the hill) results in the longest time required for the flip-flop to resolve itself to one of the stable states. The delay flip-flop can transfer the binary input towards the output depends on the edge triggered on clock pulse. The input must be stable at the edge trigger duration of clock signal which is called as setup and hold time. If the data changes during the setup and hold time violets the value of Q (Q_Metastable) may enter the metastable region resulting in a long time for Q to resolve to a stable value and therefore an unpredictable final value of Q. Flip flop is a high gain circuit, it will amplify the input voltage and output becomes at stable state. Due to the setup and hold time violation the latch may have no initial voltage to amplify and thus the output of the flip-flop may become unpredictable and take an unbounded amount of time to settle to a stable level. Fig. 2(a) shows the schematic of a flip-flop when the clock and data are transitioning at the same time. As the clock transitions the transfer gate which isolates the latch from the input is in the process of being opened, and the transfer gate which enables the positive feedback of the latching element is in the process of being closed.

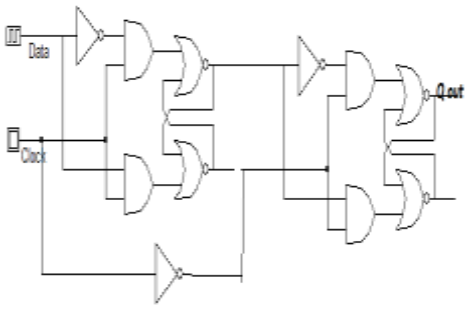

Figure 2(a): Delay Latch using cross coupled NAND gates

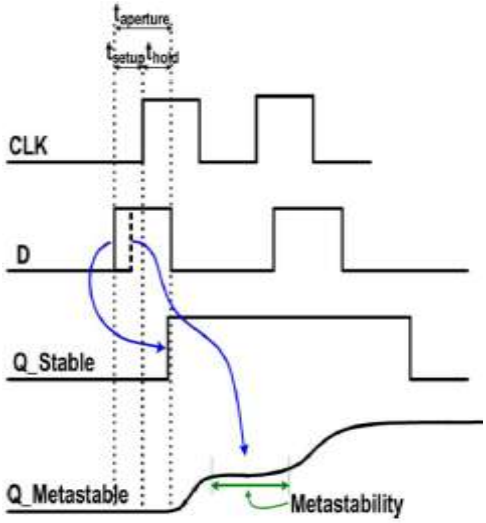

Figure 2(b): Flip-Flop waveforms in case of stable and metastable output

III. Metastability Parameter Estimation

As we have seen that whenever setup and hold violation time occurs, metastability occurs, so we have to see when signals violate this timing requirement:

When the input signal is an asynchronous signal.

When the clock skew/slew is too much (rise and fall time are more than the tolerable values).

When interfacing two domains operating at two different frequencies or at the same frequency but with different phase.

When the combinational delay is such that flip-flop data input changes in the critical window (setup+hold window).

MTBF gives information on how often a particular element will fail or in other words, it gives the average time interval between two successive failures.

If the data signal transitions at a frequency of with respect to a clock signal with a frequency of, a common metric used to characterize metastability is the mean-time-between failure (MTBF),

$$MTBF = 1 / f_D f_{CLK} T_0 e^{-ts/T}$$

where,

$T_0$is the width of the aperture window where a transition in the input data may result in metastability,

T is the resolution time constant that represents the inverse of the gain-bandwidth product of the feedback element in the flip-flop.

f_D is the data signal transitions frequency.

f_{CLK} is a clock signal frequency.

Due to the exponential relationship of MTBF, a lower T value corresponds to a faster resolution time, which increases the MTBF, resulting in a more metastable-hardened flip-flop.

The improvement in metastability will comes at the expense of additional power consumption and an increase in delay. The metastability-power-delay product (MPDP), is a useful merit to illustrate the inherent trade-off between, power, and delay.

MPDP = T x power x delay [3]

IV. Limiting Metastability

Synchronize any asynchronous input through one path that has at least one and preferably two flip-flops in series. The flip-flops should be running on the same edge of your system clock as the rest of the circuit. This will limit the area of potential problems to one path instead of several, and minimize the possibility of metastability entering the main part of the circuit. In the simplest case, designers can tolerate metastability by making sure the clock period is long enough to allow for the resolution of quasi-stable states and for the delay of whatever logic may be in the path to the next flip-flop. This approach, while simple, is rarely practical given the performance requirements of most modern designs. The most common way to tolerate metastability is to add one or more successive synchronizing flip-flops to the synchronizer. This approach allows for an entire clock period (except for the setup time of the second flip-flop) for metastable events in the first synchronizing flip-flop to resolve themselves. This does, however, increase the latency in the synchronous logic's observation of input changes. Using faster flip-flops decreases the setup and hold times of the flip-flop, which in turn decreases the time window that the flip-flop is vulnerable to metastability. When the input frequency is decreased, the chances of the input changing during the setup and hold time also decreases.[3].

V. Conclusion

It shows that flip-flop base module will have the best metastability performance. This indicates the differential feedback paths in the flip flop are a beneficial feature in improving metastability and offering soft-error protection. While the power and delay penalties are non-trivial, for robust application the flip-flop base module is attractive in terms of both soft-error protection and metastability performance. Digital circuit designers must determine the metastability characteristics of their circuit in order to ensure reliability. The degree to which metastability occurs within a circuit can to a great degree determine the reliability of a circuit. Designers must be versed in knowing about metastability, predicting the occurrence of metastability, and limiting the frequency of metastable outputs. Ways of limiting metastability include using only one clock, using faster flip-flops, decrease the asynchronous input frequency, and use synchronization hardware. These steps can easy be taken by designers to increase the reliability of a circuit.

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