ISSN: 2278 – 1323
International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)
Volume 2, Issue 1, January 2013

DDS architecture for digital frequency generation

Ms. Shruti S.Desai, Prof. A.S.Joshi

Abstract:

Direct digital synthesizers (DDS) are important components in many digital communication systems[4].DDSs are now available as integrated circuits and their output waveforms up to hundreds of megahertz. Direct digital synthesis (DDS) is a technique for using digital data processing blocks as a means to generate a frequency- and phase-tunable output signal referenced to a fixed-frequency precision clock source. While DDS is slowly gaining acceptance in new system designs, methods used to improve the quality of the generated waveform are seldom used, even nowadays. From Colpitts oscillators [7] to phase locked-loops [8], methods have been proposed to improve stability, frequency resolution, and spectral purity. Among the all-digital approaches such as the one presented in [9], direct digital frequency synthesis (referred to here as DDS) appeared in 1971 [10]. Three years later, this technique was embedded in a commercial unit measuring group delay of telephone lines [11]. This paper provides an overview of the basics of DDS, along with simple formulas to compute bounds of the signal characteristics. Moreover, several methods are presented to overcome some of the limits of the basic DDS with a focus on improving output signal quality. This paper also describes the architecture of DDS & the various blocks involved.

Index Terms: **DDS, Digital Communication Systems, Frequency Precision**

I. INTRODUCTION

Today's cost-competitive, high-performance, functionally-integrated, and small package-sized DDS products are fast becoming an alternative to traditional frequency-agile analog synthesizer solutions.

The integration of a high-speed, high-performance, D/A converter and DDS architecture onto a single chip (forming what is commonly known as a Complete-DDS solution) enabled this technology to target a wider range of applications and provide, in many cases, an attractive alternative to analog-based PLL synthesizers. For many applications, the DDS solution holds some distinct advantages over the equivalent agile analog frequency synthesizer employing PLL circuitry.

II. DIRECT DIGITAL FREQUENCY SYNTHESIS

DDS (Direct Digital Synthesis) is the new technology appearing with the digital integrated circuit and the development of micro-electric technique[3]. It adopts the digital sample store technology, proceed from angle of the phase and carry on frequency to synthesis, have high, advantage that conversion time is short of resolution ratio of accuracy of phase, frequency. DDS special-purpose chip uses a built-in high performance DAC convert the reference frequency to the sample sinusoidal wave which is controlled by the extremely meticulous frequency. It adopts the digital control technology, that's means it does not need manual system to adjust, thus can offer needed frequency signals very conveniently. It is one new generation frequency synthesizer, from measure apparatus to the wireless and satellite communication field, it get widely used. It offers sizable performance advantages, they are reflect specifically in the relative wide bandwidth, short conversion time for the frequencies, the high resolution ratio of frequency, continuously output phase and it can produce the broadband orthogonal signal and other many kinds of modulation signals.

At present, many large chip manufacturers introduce the high performance and multi-functional DDS chip that adopt the advanced CMOS craft produced in succession, have offered many kinds of choices to circuit designer. But in some occasions, the special-purpose DDS chip is far behind requirement for the system in such aspects as control method, operating frequency, speed, so designing DDS circuit meeting it self's needs with high-performance FPGA device is a very advisable solution.

III. PRINCIPLE OF DIRECT DIGITAL SYNTHESIS TECHNOLOGY

The principle block diagram of DDS is shown as Figure 1, it has five parts include the phase accumulator, wave form memory, DAC, low pass filter and reference clock of cloc[4]. Under control of the clock signal, the controls words of phase accumulator to accumulate the frequency linearly, phase got seeks the location to wave form memory, enable its output's corresponding range, get the corresponding ladder wave, the wave form of the necessary frequency changed continuously through the low open wave filter finally through the DA converter.

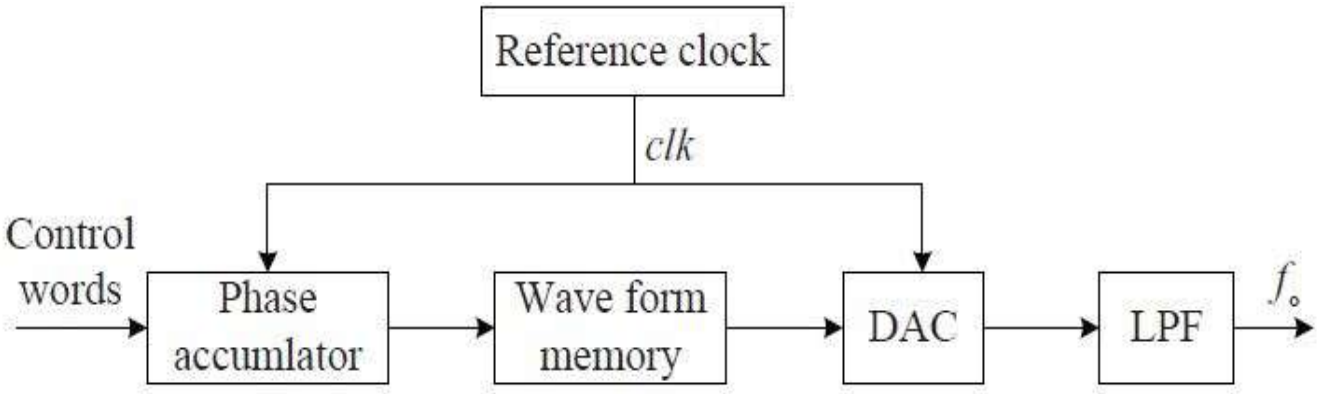

Figure 1. Principle block-diagram of DDS

In Figure 1, the clock signal was produced by a high and stable crystal oscillator, used for guaranteeing every part works in step in DDS, the frequency control word K send to the addition device data input terminus in N location phase accumulator, the accumulator of phase is under the control of the clock frequency, controlling the data and accumulating the linear phase to frequency constantly, will produce and overflow when the accumulator of phase accumulates the data and reaches the preserving value, the frequency of overflowing of the accumulator is the frequency signal of DDS outputted. The relationship between the output signal of the DDS fout , clock signal fc , the frequency control word K and the number of bits of the phase accumulator is shown as formula ,

$$f_{out} = \frac{kf_c}{2^N}$$

IV.THEORY OF OPERATION

A high-level view of the DDS Core is presented in Figure 2.The integrator (components D1 and A1) computes a phase slope that is mapped to a sinusoid (possibly complex) by the look-up table T1. The quantizer Q1, which is simply a slicer, accepts the high-precision phase angle and generates a lower precision representation of the angle denoted as in the figure. This value is presented to the address port of a look-up table that performs the mapping from phase-space to time.

The fidelity of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process. The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively. These resolution limits are equivalent to time base jitter and to amplitude quantization of the signal, and add spectral modulation lines and a white broad-band noise floor to the signal's spectrum. Direct digital synthesizers use an addressing scheme with an appropriate look-up table to form samples of an arbitrary frequency sinusoid. If an analog output is required, the DDS presents these samples to a digital-to-analog converter (DAC) and a low-pass filter to obtain an analog waveform with the specific frequency structure. Of course, the samples are also commonly used directly in the digital domain. The look-up table traditionally stores uniformly spaced samples of a cosine and a sine wave. These samples represent a single cycle of a length $N = 2^{B_{\theta(n)}}$ prototype complex sinusoid and correspond to specific values of the sinusoid's argument as shown in Eq.(1).

$$\theta(n) = n\frac{2\pi}{N} \qquad (1)$$

Where n is the time series sample index.

Quarter wave symmetry in the basis waveform can be exploited to construct a DDS that uses shortened tables. In this case, the two most significant bits of the quantized phase angle are used to perform quadrant mapping. This implementation results in a more area efficient implementation because the memory requirements are minimized: either fewer FPGA block RAMs or reduced distributed memory. Based on the Core customization parameters, the DDS core will automatically employ quarter-wave symmetry when appropriate1.

A. Output Frequency

The output frequency f_{out} of the DDS waveform is a function of the system clock frequency f_{clk}, the number of bits $B_{\theta(n)}$ in the phase accumulator and the phase increment value $\Delta\theta$. That is, $F_{out}=f(f_{clk}, B_{\theta(n)}, \Delta\theta)$. Output frequency in Hertz is defined as,

$$f_{out} = \frac{\Delta\theta * f_{clk}}{2^{B_{\theta(n)}}} \qquad (2)$$

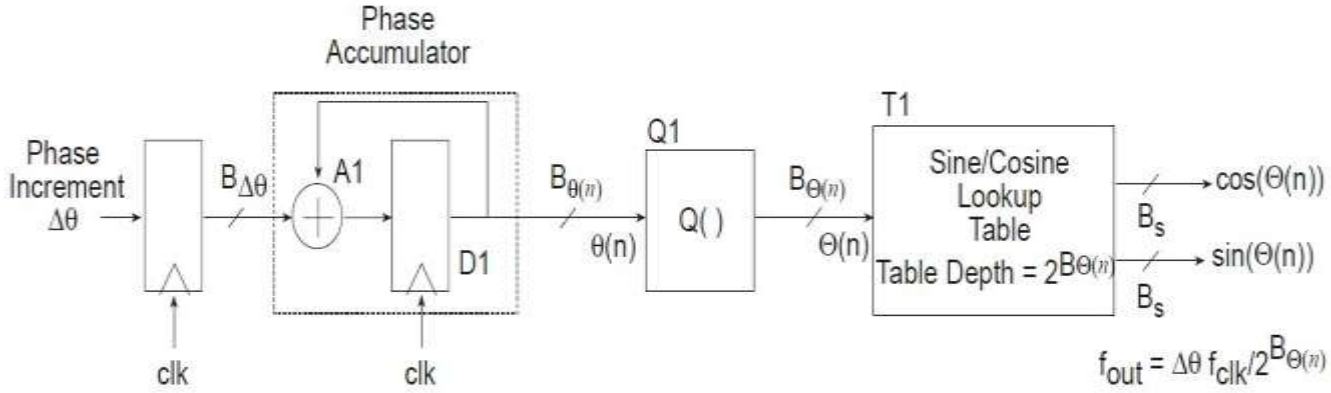

Figure 2 : Simple view of DDS

$$\Delta\theta = \frac{f_{out}\, 2^{B_{\theta(n)}}}{f_{clk}} \qquad (5)$$

B. Frequency Resolution

The frequency resolution of the synthesizer is a function of the clock frequency and the number of bits,employed in the phase accumulator. The frequency resolution can be determined using the following equation,

$$\Delta f = \frac{f_{clk}}{2^{B_{\theta(n)}}} \qquad (6)$$

C. Phase Increment

The phase increment is an unsigned value. The phase increment term defines the synthesizer output frequency. Consider a DDS with the following equation,

$$\Delta\theta = \frac{f_{out}\, 2^{B_{\theta(n)}}}{f_{clk}} \qquad (8)$$

D.Spectral Purity Considerations

The fidelity of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process. The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively. These resolution limits are equivalent to time base jitter and to amplitude quantization of the signal and add spectral modulation lines and a white broad-band noise floor to the signal's spectrum. In conjunction with the system clock frequency, the phase accumulator width determines the frequency resolution of the DDS. The accumulator must have a sufficient field width to span the desired frequency resolution. For most practical applications, a large number of bits are allocated to the phase accumulator in order to satisfy the system frequency resolution requirements. The field width of the accumulator is,

$$B_{\theta(n)} = log_2 \left\lceil \frac{f_{clk}}{\Delta f} \right\rceil \qquad (9)$$

where $\lceil\ \rceil$ denotes the ceiling operator. Due to excessive memory requirements, the full precision of the phase accumulator cannot be used to index the sine/cosine look-up table. A quantized (or truncated) version of the phase angle is used for this purpose. The block labeled Q1 in the phase truncation DDS, Figure 1, performs the phase angle quantization. The lookup table can be located in block or distributed memory. Quantizing the phase accumulator introduces time base jitter in the output waveform. The jitter results in undesired phase modulation that is proportional to the quantization error. Figure 3 [4]shows the look-up table addressing error, complex output time-series and the spectral domain representation of the output waveform produced by the DDS structure shown in Figure 1.

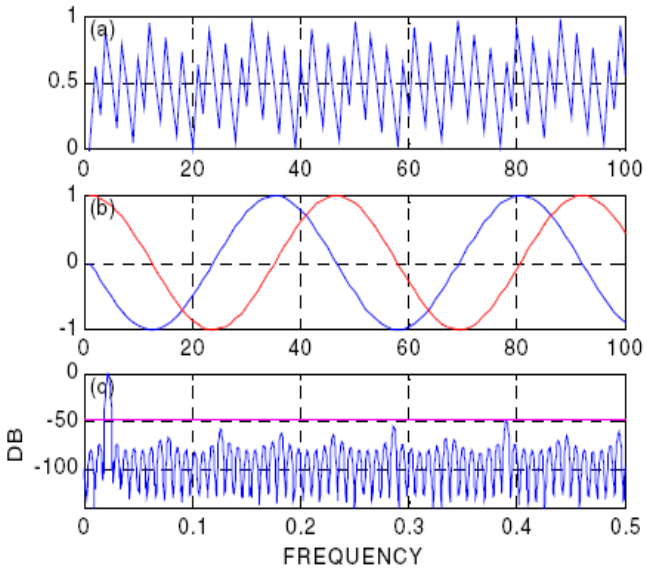

Figure 3: Phase truncation DDS. f_{out}= 0.022 Hz, table depth = 256 12-bit precision samples. (a) Phase angle addressing error; (b) Complex output time series; (c) Output spectrum.

Figure 4 [4]demonstrates the performance of a similar DDS to the one presented in Figure 2 but in this example 16-bit precision output samples have been used. Observe that the highest spur is still at the –48 dB level, and allocating 4 additional bits to the output examples has not contributed to any further spur reduction. For a phase truncation DDS, the only option to further reduce the spur levels is to increase the depth of the look-up table.

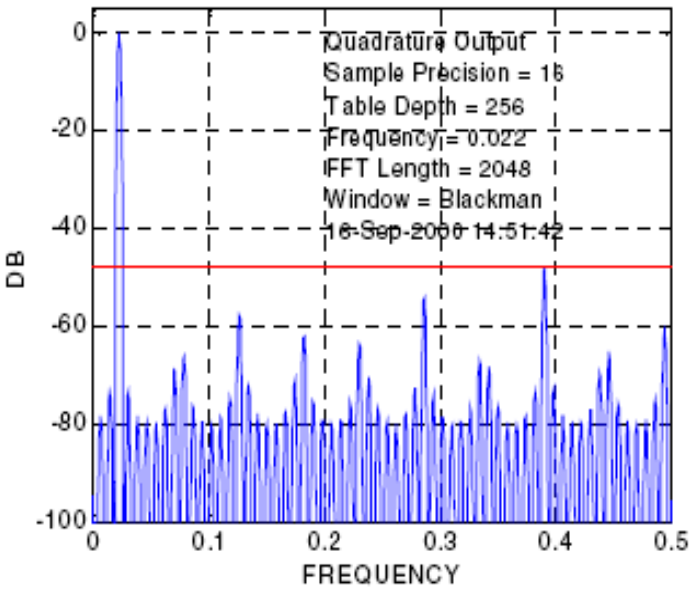

Figure 4: **Phase truncation DDS. Hz, table depth = 256 16-bit precision samples.**

V. MAIN FEATURES OF THE DDS

A.*Extremely high resolution ratio of frequency*

From formula (1), it can be found out that if the reference clock is confirmed, the frequency resolving enough, can receive the enough high resolution ratio of frequency. When K=1, the lowest frequency fmin produced by DDS is named the frequency resolution ratio,

$$f_{min} = \frac{f_c}{2^N}$$

For example, if the reference clock of DDS f =40MHz, N = 32 , then the fmin can be $0.9*10^{-5}$ Hz.

B. Phase continuity when the frequency agility

In the hopping frequency communication system, the traditional frequency synthetic technology has some difficulties to realize the frequency agility. But in DDS, the ones that outputted the signal and
changed are not two signals, but it is the change of the phase rate of increase of the same signal, so phase which outputs the signal is continuous.

C. The arbitrary wave form outputs ability

The wave form of outputting the location sought of the phase accumulator is determined by the data that are stored in the wave form memory in DDS. If the frequency of the high-frequency weight stored in the memory is smaller than the half of sampling frequency, that means so long as the data stored accord with the theorem of sampling, then this wave form can be produced by DDS, and because DDS is the module structure, so, the data that only need changing in the memory, can utilize DDS to produce arbitrary wave forms such as the sine, square wave, triangular wave, saw tooth wave, etc.

VI. ADVANTAGES

- Micro-Hertz tuning resolution of the output frequency and sub-degree phase tuning capability, all under complete digital control.
- Extremely fast “hopping speed” in tuning output frequency (or phase), phase-continuous frequency hops with no over/undershoot or analog-related loop settling time anomalies.
- The digital control interface of the DDS architecture facilitates an environment where systems can be remotely controlled, and minutely optimized, under processor control.
- The DDS digital architecture eliminates the need for the manual system tuning and tweaking associated with component aging and temperature drift in analog synthesizer solutions

VII. CONCLUSION

Simplified block diagram of DDS along with theory of operations, features & advantages is discussed here. According to the discussion, Direct digital synthesizer can be used for high precision frequency generation. By increasing the look up table the spur level can be reduce.

VIII. REFERENCES

1. 2012 International Conference on Solid State Devices and Materials Science,High Precision Digital Frequency Signal Source Based on FPGA,SHI Yanbina,GUO Jianb, CUI Ningc.
2. L. Cordesses, "Direct Digital Synthesis: A Tool for Periodic Wave Generation (Part 1)" IEEE Signal Processing Magazine, DSP Tips & Tricks column, pp. 50–54, Vol. 21, No. 4 July 2004.
3. L. Cordesses, Direct Digital Synthesis: A Tool for Periodic Wave Generation (Part 2) IEEE Signal Processing Magazine, DSP Tips & Tricks column, pp. 110–117, Vol. 21, No. 5, Sep. 2004.
4. www.xilinx.com/Products/Intellectual/property/Direct_Digital_Synthesizer.html
5. Chen Cheng; Qin Li-tao; Su Yan-qun. Implementation of DDS Signal Source Based on FPGA, Computer and Information Technology, 2010.02
6. YANG Xin Chun; REN Lu Juan; HUANG Yang Wen, Design of adjustable signal source based on FPGA, Microcomputer & Its applications, 2010.04
7. U.L. Rohde, J. Whitaker, and T.T.N. Bucher, Communications Receivers, 2nd ed. New York: McGraw Hill, 1997.
8. U.L. Rohde, Digital PLL Frequency Synthesizers—Theory and Design. Englewood Cliffs, NJ: Prentice-Hall, 1983.

9. C.L. Turner, "Recursive discrete-time sinusoidal oscillators," IEEE Signal Processing Mag., vol. 20, no. 3, pp. 103–111, May 2003.
10. J. Tierney, C. Rader, and B. Gold, "A digital frequency synthesizer," IEEE Trans. Audio Electroacous., vol. 19, no. 1, pp. 48–57, Mar. 1971.
11. D.H. Guest, "Simplified data-transmission channel measurements," *Hewlett-Packard J*, vol. 26, no. 3, pp. 15–24, Nov. 1974.

Ms. Shruti S. Desai is currently working as an assistant professor in the department of electronics & Telecommunication, at Sipna College of Engineering & Technology, Amravati M.S. (India). Her areas of interest are embedded systems & Very large scale integrated circuits.

Prof. Atul S. Joshi is currently working as a Associate Professor in Department of Electronics & Telecommunication Engineering, at Sipna College of Engineering & Technology, Amravati M.S.(India). His areas of interest are Communication Engineering, data mining, Communication Network & Electronic Circuits Design.