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Scaling of Dimensions & Gate Capacitances of MOSFET

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***Abstract*-- The scaling of complementary metal oxide semiconductor (CMOS) transistors has led to the silicon dioxide layer used as a gate dielectric becoming so thin (1.4 nm) that its leakage current is too large. It is necessary to replace the SiO2 with a physically thicker layer of oxides of higher dielectric constant (κ) or 'high *K*' gate oxides such as hafnium oxide and hafnium silicate. Little was known about such oxides, and it was soon found that in many respects they have inferior electronic properties to SiO2, such as a tendency to crystallise and a high concentration of electronic defects. Intensive research is underway to develop these oxides into new high quality electronic materials. This review covers the choice of oxides, their structural and metallurgical behaviour, atomic diffusion, their deposition, interface structure and reactions, their electronic structure, bonding, band offsets, mobility degradation, flat band voltage shifts and electronic defects. The use of high *K* oxides in capacitors of dynamic random access memories is also covered.**

***KEY WORDS:*scaling, capacitance and MOSFET.**

I. INTRODUCTION

In order to get more conductivity out of a MOSFET, we have to increase the efficiency of it by reducing its dimension & this phenomenon is termed as SCALING. Such Scaling effects in an increase in the channel electric field and in a higher drain current and operates at a higher frequency this in turn increases the dynamic power consumption per unit area. The lateral dimensions of devices are reduced. This reduction in size is referred to as "scaling" of the integrated circuit. This minimum feature size of integrated circuit has shrunk considerably over the time of several decades. As a consequence, the number of transistors has increased over time.

II. SCALING OF MOS CIRCUITS

Design of high density chip in MOS VLSI technology requires that packing density should increase accordingly size of the IC must decrease. This reduction in size, i.e. the dimensions of the MOSFET is termed as SCALING.

In order to increase the conductivity of the MOSFET by factor (say) **S,** where S>1, we should reduce the dimensions by S. This S is generally known as SCALING FACTOR**.**This fig. shows how the dimensions of the MOSFET are altered due to scaling.

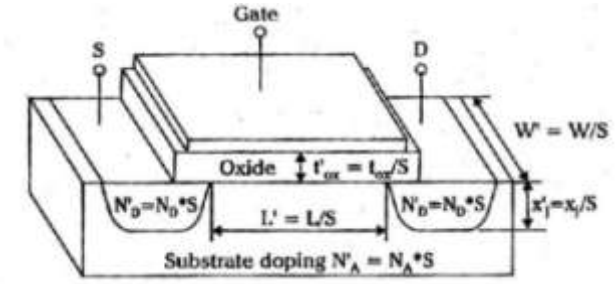


Fig 1: Scaling of typical MOSFET by a Scaling factor of S.

III. MOORE'S LAW OF SCALING

The performance of these MOSFET devices is widely improved by Moore's law of scaling.**Moore's law** is the observation that over the history of computing hardware, the number of transistors on integrated circuits doubles approximately every two years. The law is named after Intel co-founder Gordon E. Moore, who described the trend in his 1965 paper.

With the use of Moore's Law in semiconductor electronics, capabilities such as, processing speed, memory capacity, efficiency have been improved greatly.

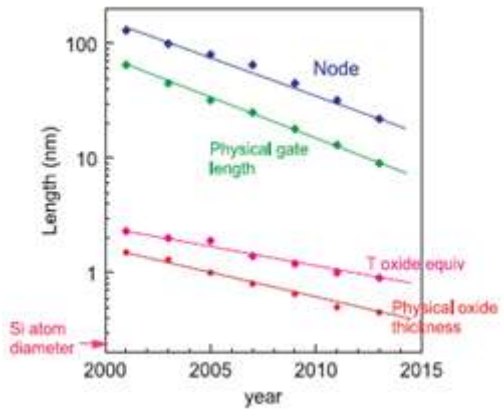
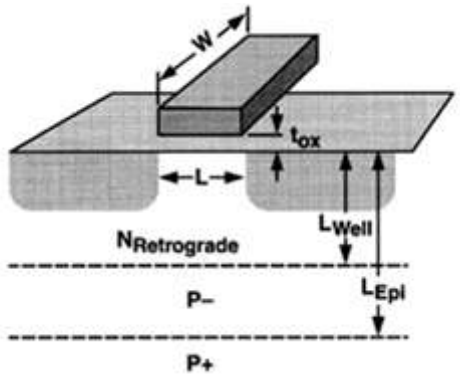


Fig 2: Scaling of feature size,gate length and oxide thickness

Following can be seen

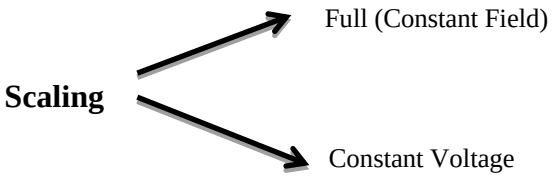
a. **Transistors per integrated circuit.**
b. **Density at minimum cost per transistor.**



Channel Length	**L'= L/α**
Channel Width	**W' = W/α**
Gate Dielectric Thickness	**tox'=tox'/α**
Epi Depth	**L'Epi = LEpi/α**
Well Depth	**L'Well=L Well/α**
Doping	**N'=Nα**

α = Scaling parameter

IV. TYPES OF SCALING



A. FULL SCALING(Constant Field Scaling)

Full scaling is that scaling which preserves the magnitude of the electric field inside the MOSFET while the dimensions are scaled by a factor **S.**Due to this scaling technique, the charge densities are advanced by **S** in order to maintain the magnitude of the fields inside.Say for the scaling factor, S=α, we have the following observations:If we go for the influence of full scaling on the current voltage characteristics of MOS transistors, we make an assumption that the surface mobility, μ_n is not significantly affected by the scaled doping density.But the gate oxide capacitance is changed as follows

$$C'_{OS} = \frac{\epsilon_{ox}}{t'_{ox}} = S.\frac{\epsilon_{ox}}{t_{ox}} = S.C_{ox} \quad (1)$$

The aspect ratio W/L will remain unchanged under scaling. Consequently, the transconductance parameter k_n, will also be scaled by the factor S. since all terminal voltage are also scaled down, the linear mode drain current of the scaled MOSFET can now be found as

$$I'_D(lin) = \frac{k'_n}{2}\left(2(V'_{GS} - V'_T)V'_{DS} - V'^2_{DS}\right)$$
$$= \frac{SK_n}{2}\frac{1}{S^2}\left(2(V'_{GS} - V'_T)V'_{DS} - V'^2_{DS}\right)$$
$$= \frac{I_D(lin)}{S} \quad (2)$$

Similarly, for the saturation mode drain current,

$$I'_D(sat) = \frac{k'_n}{2}((V'_{GS} - V'_T)^2)$$
$$= \frac{SK_n}{2}\frac{1}{S^2}((V'_{GS} - V'_T)^2)$$
$$= \frac{I_D(sat)}{S} \quad (3)$$

Before scaling, the instantaneous power dissipated by the MOSFET will be

$$P = I_D V_{DS} \quad (4)$$

Noticing that both of the drain current and drain to source voltage are reduced by a factor S, and then the power also gets by S^2.

$$P' = I'_D V'_{DS} = \frac{1}{S^2} I_D V_{DS}$$
$$P' = \frac{P}{S^2} \quad (5)$$

This reduction in power dissipated is a very attractive feature of full scaling. We also find that the power density per unit area remains virtually unchanged for the scaled device.Charging & discharging of the capacitance in the MOSFET eventually affects the transient operation of it. Consider the gate oxide capacitance defined as $C_g=WLC_{ox}$. Since it is scaled down by a factor S, the charge-up and charge-down time from the transient characteristics of the device after scaling get improved accordingly. This proportional reduction of on-chip dimensions, improves the overall performance by decreasing the parasitic capacitances as well as resistances.

Quantity	**Before Scaling**	**After Scaling**
Oxide capacitance	C_{ox}	$C'_{ox}.S$
Drain current	I_D	I'_D/S
Power Dissipation	P	P'/S^2
Power Density	P/Area	P'/Area'=P/Area

The table shown summarizes the changes in scaled-device characteristics as a result of full (constant-field) scaling.

B. CONSTANT-VOLTAGE SCALING

In particular, the peripheral and interface circuitry may require certain voltage level for input and output voltages, which in turn will necessitates multiple power supply voltages and complicated level-shifter arrangements. So, this practically leads constant-field scaling. As done in full scaling, here too the dimensions of the MOSFET are reduced by S. but on the other hand, power supply and power density remains unchanged.Constant voltage scaling of MOSFET dimensions, potentials & doping densities are as shown

Quantity	Before Scaling	After Scaling
Dimensions	W,L,t_{ox},x_j	Reduced by S
Voltages	V_T	Remain unchanged
Doping Densities	N_A,N_D	Increased by S^2

Here, the transconductance parameter is increased by S as well i.e. the gate oxide capacitance per unit area C_{ox} is increased by S. Since the terminal voltage remains unchanged, then the linear mode drain current of the scaled MOSFET can be given as

$$I'_D(lin) = \frac{k'_n}{2}\left(2(V'_{GS} - V'_T)V'_{DS} - V'^2_{DS}\right)$$
$$= \frac{SK_n}{2}\left(2(V'_{GS} - V'_T)V'_{DS} - V'^2_{DS}\right)$$
$$= SI_D(lin) \quad (6)$$

This scaling also affects the saturation mode drain current, which also gets increased by factor S, i.e. the drain current density (current per unit area) gets elevated by S^3, which causes serious reliability problems to the MOSFET transistor.

$$I'_D(sat) = \frac{k'_n}{2}((V'_{GS} - V'_T)^2)$$
$$= \frac{SK_n}{2}((V'_{GS} - V'_T)^2)$$
$$= S\,I_D(sat) \quad (7)$$

Since, the drain current is increased by S; the drain to source voltage undergoes no change. So, the power dissipated by the MOSFET in increased by a factor S.

$$P' = I'_D V'_{DS}$$
$$= (S\,I_D)V_{DS}$$
$$= S.P \quad (8)$$

Finally, the power density is found to be increased by a factor of S^3 after the constant voltage scaling, accompanying with possible adverse on the device reliability.

Table beneath shows the effect of constant-voltage scaling in the key device characteristics.

Quantity	Before Scaling	After Scaling
Oxide Capacitance	C_{ox}	$C'_{ox}=S.C_{ox}$
Drain Current	I_D	$I'_D=S.I_D$
Power Dissipation	P	P'=S.P
Power Density	P/Area	P'/Area'=S^3(P/Area)

As constant-voltage scaling is a disaster for the device reliability, but still it's preferred over full (constant-field) scaling in many practical cases because of the external voltage level constraints. However, it must be known that constant voltage scaling elevates the drain current density and power density by S^3, which may cause problems, as, electro migration, hot-carrier degradation, oxide breakdown and electrical overstress in the scaled MOS transistor.

As device dimensions are systematically reduced through full scaling, various physical limitations become increasingly more prominent, and ultimately restrict the amount of feasible scaling for some device dimension. Consequently, scaling may be carried out on a certain subset of MOSFET dimensions in many applications. Also the simple Gradual Channel Approximation (GCA) used for the derivation of current voltage relationship doesn't accurately reflect the effects of scaling in smaller size transistors. The current equations have to be modified accordingly.

Comparison of the two scaling techniques

Full Scaling	Constant-Voltage Scaling
The power supply voltage and terminal voltage are scaled.	The power supply voltage and terminal voltage are not scaled.
Drain current are scaled by factor S in both linear and saturation mode of operation.	Drain current are multiplied by S in both linear and saturation mode of operation.
Power dissipation is described by the factor of S^2 in full swing.	Power dissipation is described by the factor of S.
Power density doesn't change in case of full swing	Power density is increased by a factor of S^3, in case of constant voltage scaling.

V. SECOND ORDER SCALING EFFECTS

The first order scaling discussed above deals with direct transformation of MOSFET dimensions, doping levels, voltage and current. Second order effect arises when the interdependence of device characteristics on these parameters is examined.

Mobility can serve as an example of second order effect. In general, μ is a function of background doping such that

$$\left(\frac{\partial \mu}{\partial N}\right) < 0 \quad (9)$$

i.e. the mobility decreases with increase in level of doping. Since scaling theory uses an upward scaling to

N'=SN or N'=S^2N, increased impurity scattering gives that

$$\mu' < \mu(10)$$

After this, the transconductance no longer exhibits linear scaling characteristics.The effects of ion implants also changed when the vertical dimensions are scaled. However, if the drain and source junctions depth are scaled according to

$$x'_j = \frac{x_j}{S}(11)$$

Then the ion implant penetration depth may be comparable with x'_j. A similar comment applies to the charge terms

$$-\frac{1}{C_{ox}}\left(Q_f + Q_{ox}\right) \quad (12)$$

In the flat band voltage as x_{ox} is scaled. Along with all these, we must also scale the thickness of all other layers in the device. This includes the gate material and metal interconnects in particular. Although these didn't affect directly on device characteristics but affect the performance of circuit since they will alter the values of various parasitic.

VI. BASIC SCALING THEORY

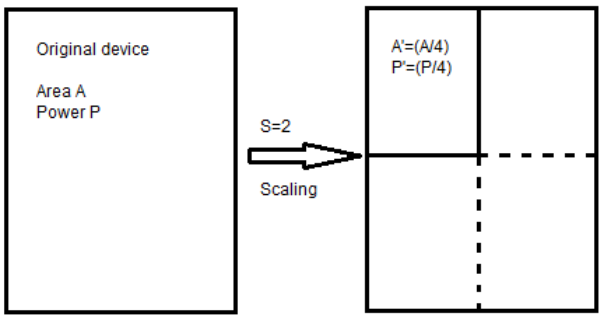
The effectof basic scaling with S=2.
This would imply that the channel dimension W and L will change to new values

$$L' = \frac{L}{2} \quad and \quad W' = \frac{W}{2}$$

And the original area A=WL gets reduced to

$$A' = \frac{A}{4}$$

This is portrayed as shown below



The reduction in surface area is obvious. However, full scaling also reduces the power of the scaled device to 1/4th of its original layout value.

VII. CONCLUSION

We have seen that both of the scaling, viz. full (constant-field) and constant voltage scaling, we tend to describe the dimensions of the MOSFET dimensions by scaling factor, S.But still latter type of scaling is preferred much over the former one practically, because of the fact that the power supply and external voltage applied to this also gets scaled by same factor S, wherein this is not performed in full scaling. Though constant voltage scaling is a disaster for MOStransistor reliability, still it is preferred over full scaling.

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