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Implementation Of Fully-Pipelined 16-Point DHT Architectures Using 8-Point And 4-Point DHTs for FPGA Realization

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Abstract— **Fully–pipelined simple modular structures are presented in this project for efficient hardware realization of Discrete Hadamard transform (DHT).From the kernel matrix of HT three different pipelined modular designs are derived for transform length N=4.It is shown further that the HT of transform length N=8 can be obtained from two 4-point HT modules, and similarly, the HT of the transform length N=16 can be obtained from four 4-point HT modules.Higher – length transforms can be obtained from these short length modules as N-point transforms can be computed from 2M number of M point HT-modules, where $M=N^{1/2}$.The proposed architectures are coded in Verilog, simulated by Xilinx ISE tool for validation and testing and may be synthesized thereafter to be implemented in FPGA device, Spartan-3 and the performance will be compared with the one of the present structures.**

***Index Terms*—Discrete Orthogonal Transforms (DOTs), Discrete Hadamard Transforms (DHTs), Best Achievable Frequency (BAF), Field Programmable Gate Arrays (FPGA).**

I. INTRODUCTION

The Discrete orthogonal Transform (DOT) has highly practical value for representing signals and images, especially for the purposes of data compression. The reason for the practicality of this transforms its simplicity. The elements of the Hadamard matrix are either +1 or -1.Thus the computation of the transform of a signal consists of additions and subtractions of the signal samples. This leads to savings in hardware resources, as no multiplier is used.

Hence The DHT is utilized for efficient generation of pseudo noise sequences for CDMA (Code Division Multiple Access) technique in wide band communication systems.

It can be used for basic digital Signal Processing (DSP) operations like computation of the DFT, implementation of digital filters and spectral estimation.

It is also an important tool for speech processing and error control coding.

In addition to its frequent use for audio and video Processing, it has a lot of other applications in data encryption, and many signal processing and data compression algorithms such as JPEG and MPEG.

FPGA devices are becoming more popular in recent years, due to their lower cost compared with application specific integrated circuits (ASICs) and also due to their scope of reusability as programmable device and scope for increasing transistor density available in it to implement various complex algorithms in signal processing, image processing and communication.

In this paper we propose two simple and efficient pipelined designs for computation of a 16-point DHT by using two pipelined stages of either two 8-point add/subtract units each or by using four 4- point DHT modules. The same can be used to generate DHT of higher transform-lengths.

The rest of the paper is organized as follows:

II. Derivation of the algorithms of FPGA implementation of DHT.

III Description of the proposed architectures.

IV Presentation of the results of implementation

V Conclusions.

II. MATHEMATICAL FORMULATION

A. Basic Formulations:

The Discrete Hadamard Transform of a sequence { x(n) for n=0,1,2,……,N-1}

$$X(k) = \sum_{n=0}^{N-1} H_N(k.,n).x(n), \qquad \text{(i)}$$

For $0 \le k \le N-1$, where H_N is a Hadamard matrix of size N X N , which is defined recursively as

$$H_N = H_{N/2} \otimes H_2 = H_2 \otimes H_{N/2} \qquad \text{(ii)}$$

where the symbol $\otimes$ denotes Kronecker product, and

$$H_2 = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \qquad \text{(iii)}$$

The Hadamard matrix H_N may therefore be given by

$$H_N = \begin{bmatrix} H_{N/2} & H_{N/2} \\ H_{N/2} & -H_{N/2} \end{bmatrix} \qquad \text{(iv)}$$

Using (iv), the HT of N-point sequence {x (n)}, given by (i) can be written as,

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$$\begin{bmatrix} X_2^1 \\ X_2^2 \end{bmatrix} = H_{N/2} \otimes \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \cdot \begin{bmatrix} x_2^1 \\ x_2^2 \end{bmatrix} \quad \text{(v)}$$

where

$$X_2^1 = [X(0) \quad X(1) \quad X(2) \quad X(3) \quad . \quad . \quad . \quad X(N/2-1)]^T \quad (vi.a)$$
$$X_2^2 = [X(N/2) \quad X(N/2+1) \quad \ldots\ldots\ldots\ldots X(N-1)]^T \quad (vi.b)$$
$$x_2^1 = [x(0) \quad x(1) \quad X(2) \quad X(3) \quad . \quad . \quad . \quad x(N/2-1)]^T \quad (vi.c)$$
$$x_2^2 = [x(N/2) \quad x(N/2+1) \quad \ldots\ldots\ldots\ldots x(N-1)]^T \quad (vi..d)$$

suchthat

$$X_2^1 = H_{N/2} \cdot (x_2^1 + x_2^2) \quad \text{(vii.a)}$$
$$X_2^2 = H_{N/2} \cdot (x_2^1 - x_2^2) \quad \text{(vii.b)}$$

The Hadamard matrix $H_{N/2}$ of size $N/2 \times N/2$, may similarly be obtained from (ii) as

$$H_{N/2} = \begin{bmatrix} H_{N/4} & H_{N/4} \\ H_{N/4} & -H_{N/4} \end{bmatrix} \quad \text{(viii)}$$

Using it in (iv), the HT of N-point sequence{X(n)}, can be written as

$$\begin{bmatrix} X_4^1 \\ X_4^2 \\ X_4^3 \\ X_4^4 \end{bmatrix} = H_{N/4} \otimes \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} x_4^1 \\ x_4^2 \\ x_4^3 \\ x_4^4 \end{bmatrix} \quad \text{(ix)}$$

such that

$$X_4^1 = H_{N/4} \cdot (x_4^1 + x_4^2 + x_4^3 + x_4^4) \_\_\_\_\_ (x.a)$$
$$X_4^2 = H_{N/4} \cdot (x_4^1 - x_4^2 + x_4^3 - x_4^4) \_\_\_\_\_ (.x.b)$$
$$X_4^3 = H_{N/4} \cdot (x_4^1 + x_4^2 - x_4^3 - x_4^4) \_\_\_\_\_ (x.c)$$
$$X_4^4 = H_{N/4} \cdot (x_4^1 - x_4^2 - x_4^3 + x_4^4) \_\_\_\_\_ (x.d)$$

It can be noted from (vii) and (x) respectively that the DHT of an N-point sequence could be obtained either from two N/2-point sequences or from four N/4-point sequences, derived from the original sequence, by suitable add/subtract operations.

The recursive behavior of DHT matrix can therefore be utilized to compute an N-point DHT by 2-point or 4-point DHT.

III. Description Of The Proposed Architectures For FPGA Implementation For 4-Point DHT

In this section, we begin with deriving four different computing structures for a 4-point DHT which are very simple to implement in a single processing element (PE) of linear systolic array, 2-D systolic array, and Transverse pipelined design and forward pipelined design for 4-point DHT to be used further for the computation of DHT of higher lengths.

A. Basic Structure for 4-point DHT

The DHT of a 4-point sequence {x (0), x (1), x (2), x (3)} can be obtained from (i) and (ii) as

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \bullet \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \end{bmatrix} \quad \text{(xi)}$$

To obtain higher throughput, a 2-dimensional structure (2D) as shown in Fig (1), can be used instead of linear systolic array design, for the computation of 4-point DHT.

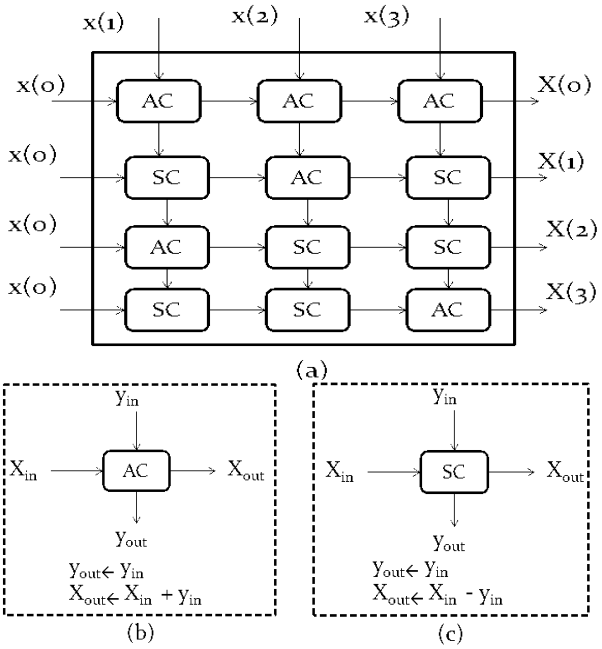

Figure1.Proposed 2-D systolic architecture for 4-point Discrete Hadamard Transform.(a)The 2-D structure. (b)Function of Adder Cell.(c)Function of Subtractor Cell

The proposed 2-D structure yields its first output three cycles after the first input arrives at the structure. After the horizontal and vertical pipelines are filled in the first seven cycles, the structure yields four outputs during every cycle. The duration of cycle period of 2-D structure is $T=T_A$, where T_A is the time required for an addition operation.

The linear systolic array can be extended further for any higher length DHT, so that a linear array consisting of (N-1) PE's can be used for N-point DHT.

Similarly, the 2-D array of Fig 1 can also be extended further for higher length DHT, so that a 2-D array consisting of N (N-1) adder/subtractor cells can be derived accordingly for N-point DHT.

B. Two –Stage algorithm for 4-point DHT

From the kernel values of (xi), a two-stage algorithm for computation of 4-point DHT can be evaluated in parallel as follows in two stages:

$$\begin{aligned} &Stage-1: \\ &a(0) = x(0) + x(1) \\ &a(1) = x(2) + x(3) \\ &a(2) = x(0) - x(1) \\ &a(3) = x(2) - x(3) \end{aligned} \quad \text{(xii)} \qquad \begin{aligned} &Stage-2: \\ &X(0) = a(0) + a(1) \\ &X(1) = a(0) - a(1) \\ &X(2) = a(2) + a(3) \\ &X(3) = a(2) - a(3) \end{aligned} \quad \text{(xiii)}$$

Based on the two stage algorithm of (xii) and (xiii) two pipelined designs, both transverse and forward are derived for 4-point DHT as given in Fig 2 and Fig 3 respectively.

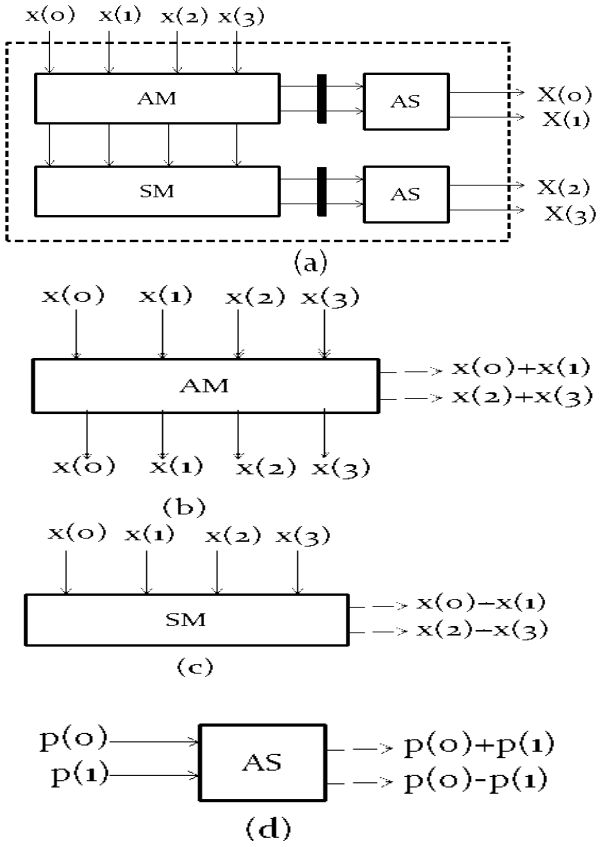

Figure2.(a).Transverse pipelined design for 4-point Discrete Hadamard Transform. (b) Adder Module. (c) Subtractor Module. (d) Add/Subtract Unit.

C. The Transverse Pipelined Structure for 4-Point DHT

The transverse pipelined structure consists of an addition module (AM), a subtraction module (SM) and an add/subtract module (AS).The function of AM, SM and AS are shown in Fig.2. (b), (c), (d) respectively.AM consists of 2 adders; SM consists of two subtractors; and AS module consists of an adder and a subtractor.

The 4-point structure of Fig.2 takes four input values during every cycle and feeds them to the AM and SM.

The pair of outputs from AM and SM are latched out to their respective AS modules in each cycle.

The pair of AS modules yields 4-point DHT output in every cycle of duration $T=T_{A,}$ after a latency of two cycles.

D. The Forward Pipelined Structure for 4-Point DHT

The Forward pipelined design for 4-point DHT, shown in Fig.3 consists of two add-subtract modules AS-1 and AS-2, working in two pipelined stages of AS-1 and AS-2. Each consists of two adders and two subtractors, and perform the computation as shown in figure.

Like the Transverse pipelined design, this structure also produces four components of 4-point DHT output in every cycle period of duration $T=T_A$, after a latency of two cycles.

The throughput of the two pipelined designs of Fig.2 and Fig.3 is same as that of the 2-D systolic array design, but involve less number of adders and subtactors.

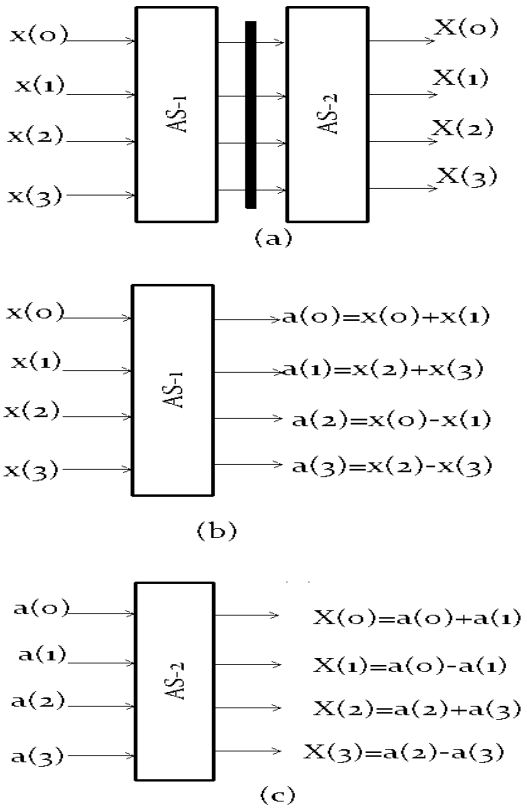

Figure3.(a).Transverse pipelined design for 4-point Discrete Hadamard Transform. (b) AdderModule. (c) Subtractor Module. (d) Add/Subtract Unit.

IV. The Structure of Proposed Architecture For 8-Point DHT For FPGA Implementation

The DHT of a 8-point sequence can be obtained from (i) and (ii) as the sequence be x(n), for $0 \le n \le 7$ is given as

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \\ X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 \\ 1 & -1 & 1 & -1 & -1 & 1 & -1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 \end{bmatrix} \begin{bmatrix} x(0) \\ x(1) \\ x(2) \\ x(3) \\ x(4) \\ x(5) \\ x(6) \\ x(7) \end{bmatrix} \quad \text{(xiv)}$$

For the simplification of the architecture we can decompose the matrix vector product (xiv) into two halves through two 4.point DHTs by using (vii) as

$$\begin{bmatrix} X(0) \\ X(1) \\ X(2) \\ X(3) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \bullet \begin{bmatrix} x(0)+x(4) \\ x(1)+x(5) \\ x(2)+x(6) \\ x(3)+x(7) \end{bmatrix} \quad \text{(xv)}$$

$$\begin{bmatrix} X(4) \\ X(5) \\ X(6) \\ X(7) \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{bmatrix} \bullet \begin{bmatrix} x(0)-x(4) \\ x(1)-x(5) \\ x(2)-x(6) \\ x(3)-x(7) \end{bmatrix} \quad \text{(xvi)}$$

This proposed structure implementation of 8-point DHT from (xv) and (xvi) is shown in Fig 4 below.

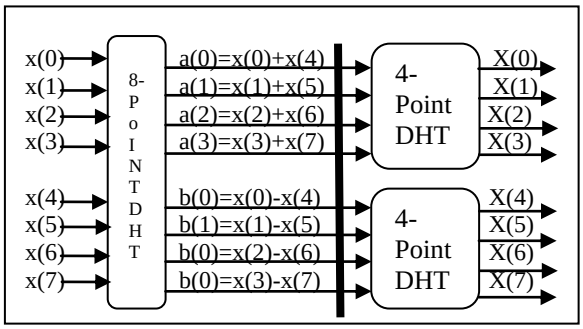

Figure 4.Proposed Linear Systolic Array for 8-point Discrete Hadamard Transform

The two 4-point input sequences a(i) and b(i) for $0 \leq i \leq 3$ are derived from the 4-point sequence x(i) for $0 \leq i \leq 7$ by an input add/subtract unit and latched to two 4-point DHT modules. These modules produce the desired output after two cycles of duration $T=T_A$.

V. The Structure of Proposed Architecture For 16-Point DHT For FPGA Implementation

The 16-point DHT can be also obtained from the four modules of 4-point DHT using (xi) in two different structures as shown in Fig 5a and 5b.

In Fig 5a, 16-point DHT can be obtained from four modules of 4-point DHT, using two pipelined stages of add/subtract units.

In Fig 5b, the structure consists of two pipelined stages, of which the first stage consists of four modules of 4-point DHTs to accesses the inputs and the second stage also consists of four 4-point DHT modules to generate the required 16-point DHT sequence.

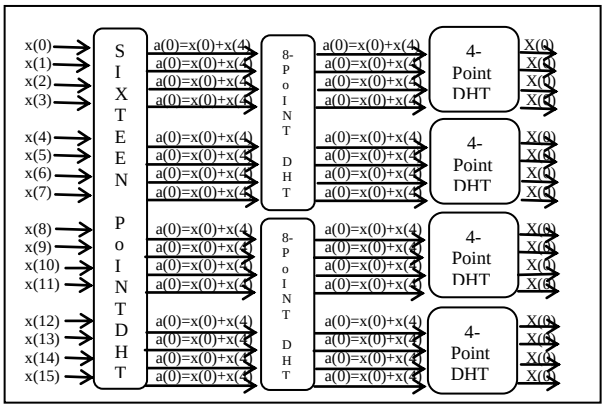

Figure 5a.proposed linear systolic array for 16-point Discrete Hadamard Transform

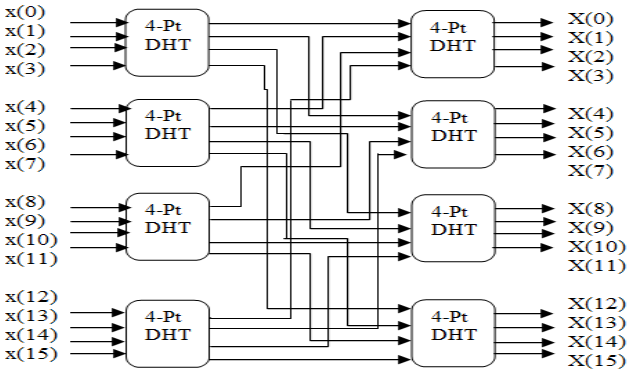

Figure 5b.proposed linear systolic array for 16-point Discrete Hadamard Transform

VI. FPGA Implementation

In order to verify the performance of the proposed architecture for DHT, the design has been prototyped on the Board contacting the Xilinx Spartan 3 named as XC3S50 (FPGA) .Available on chip logic resource :1536 slices, number of 4-input LUTs 1536, BRAM utilization ratio 100.

The proposed designs are coded in Verilog and simulated by using Xilinx ISE tool for the study of their performance for FPGA implementation of the DHT.

The word length of both input and output words are taken to be 8-bit wide. The latching between the different pipelined stages are performed by one D-flip flop per bit. The proposed designs are synthised and implemented in Spartran 3 device. The area complexity of the proposed designs in terms of number of slices are obtained from the synthesis results for N=4,8, and 16.

The speed performance of the structures in terms of BAF (Best Achievable Frequency) is obtained after performing place-and-route by using the place and route tool available in the Xilinx ISE package.

The area and timing results for the structures of Fig 3, 4,5(a) for N=4,8 and 16 respectively are listed in the table below, along with those of the recently published results.

It is from that the proposed structures involve significantly less number of slices and offer higher BAF in the devices for DHT of different lengths. The number of slices required is found to be the same in different devices, ut the BAF is found to change with the devices.

VII. Implementation Results for Proposed Structure in Comparision with Sturcture[14]

Device	Length N	Area (Slices) (out of 768)	4-input LUTs (out of 1536)	I/Os	Maximum combinational path delay(ns)
-3 (Proposed)	4	8(1%)	15(0%)	25	19.639
	8	64(8%)	119(7%)	96	19.339
	16	216(28%)	379(24%)	192	21.143

Table1: Implementation results of a proposed structure

Device	Length N	Area (Number ofSlices) (out of 768)
Structure[14]	4	32(4%)
	8	96(12.5%)
	16	256(33%)

Table1: Implementation results of a structure[9]

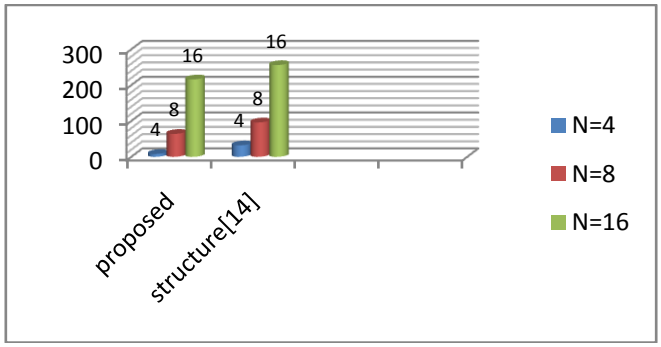

Fig.6 Comparison of Area of the proposed structures with the structure[14]

VIII. CONCLUSIONS

Simple and efficient fully-pipelined structures are designed for implementation of the DHT.

Three different pipelined and modular designs are proposed for transform length N=4.It is shown that

1.) The DHT of transform length N=8 can be obtained from two 4-point DHT modules and

2.) The DHT of transform length N=16 can be obtained from four 4-point DHT modules.

3.) Finally the proposed structures for lengths N=4, 8, 16 are compared with the structure[14] and displayed as in fig 6

Higher length transforms can be computed from these short length modules as N-point transforms can be

Computed from 2M number of M point DHTs, where $M=N^{1/2.}$

The proposed architectures are coded in Verilog, and synthesized for FPGA device Spatron-3.

From the synthesis results it is found that the the proposed designs involve considerably fewer slices when compared with the existing architectures for FPGA implementation of DHT for all the transform sizes.

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