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Radix -4/-8 Dual Encoder Block for Multiplier Architecture using GDI Technique

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***Abstract*— A hybrid radix-4/-8 multiplier is proposed for portable multimedia applications that demand high speed and low energy operation. Depending on the input pattern, the multiplier operates in the radix-8 mode in 56% of the input cases for low power, but reverts to the radix-4 mode in 44% of the slower input cases for high speed. For this Radix 4/8 Dual encoder block is designed. Compared to a conventional CMOS radix-4/8 encoder, the proposed radix-4/8 encoder consumes 43.6% less power, and 46.51% less area and 3.3% less delay time.**

Index Terms - dual encoder, multiplier,* gate-diffusion input (GDI), *power consumption.

I. Introduction

Multipliers are essential components in signal-processing for multimedia applications. While many previous works focused on implementing high-speed multipliers, recently there have been many attempts to reduce power consumption [2]. This is due to the increased demand for portable multimedia applications which require low power consumption as well as high speed operation.

However low-power multipliers without any consideration for high-speed are not the appropriate solutions of low-energy embedded signal processing for multimedia applications [1] [4]. Previously, a hybrid radix-4/-8 modified Booth encoded (MBE) multiplier was proposed for low-power and high-speed operation. This multiplier architecture had conventional CMOS radix 4/8 dual encoder [1].

The paper is organized as follows. Section II introduces hardware sharing radix4/8 dual encoder. Section III introduces GDI circuit methodology. In Section IV, introduces the conventional CMOS radix 4/8 dual encoder architecture. In Section V, the proposed GDI radix 4/8 dual encoder architecture is introduced. Implementation results are summarized in Section VI. Finally, conclusion of this paper is made in Section VII.

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II. Hardware Sharing: Radix-4/-8 Dual Encoder

After detecting the ±3B term, an encoding signal is generated. Considering similarities between radix-4 and radix-8 encoding schemes enabled shared hardware architecture called the radix-4/-8 dual encoder block [1]. We propose a hybrid radix 4/8 dual encoder with GDI technique which consumes less power with higher speed. The overall structure of the proposed radix 4/8 dual encoder is illustrated in Figure 1.

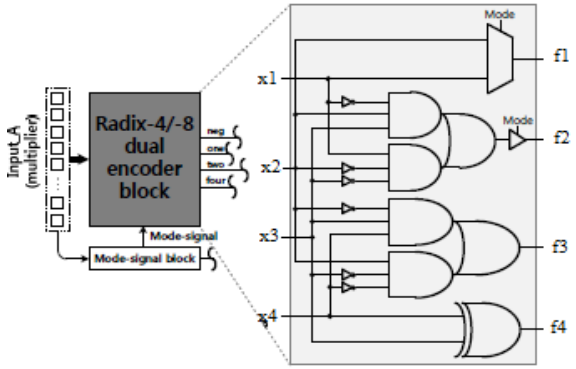

Figure 1. Radix-4 and radix-8 dual encoder circuit

Figure 2 shows the booth encoding segmentation of an 8x8 multiplier for (a) radix-8 architecture and (b) radix-4 architecture [9]. Only the encoding for the last segment (x6, x7) is identical between the two architectures. Therefore, in a naïve approach, only one radix-4 encoder block is shared, and two radix-8 encoder blocks and four radix-4 encoder blocks are necessary to provide both radix-4 and radix-8 encoding.

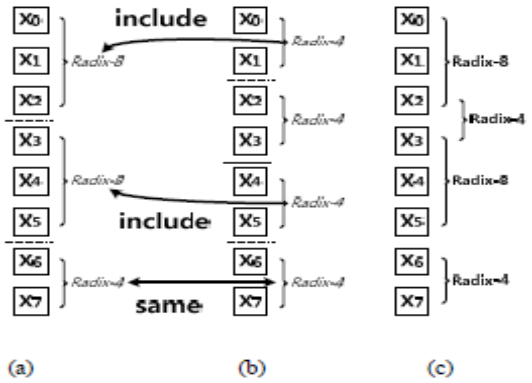

Figure 2. Multiplier segmentation (a) radix-8 (b) radix 4 (c) Hardware sharing: radix-4/-8 dual encoding

However, there is more possibility for hardware sharing when comparing with radix-4's and radix-8's encoding equation. For hardware sharing, we have to generate encoding signals of radix-4 or radix-8 within one block depending on a mode signal value. Figure 4 shows how to arrange bits to share hardware efficiently. Radix-4 mode does not need to use the MSB because it only uses 3-bit segment (including the last bit of the previous segment). On the other hand, radix-8 mode divides input A (multiplier) into 4-bit segment. Therefore we can obtain following four equations by sharing a 3-bit segment.

$$f_1 = \begin{cases} x_2 & (mode = 0) \\ x_1 & (mode = 1) \end{cases}$$

$$f_2 = \begin{cases} \overline{x_1}x_2x_3 + x_1\overline{x_2}\overline{x_3} & (mode = 0) \\ Z\,(high - impedence) & (mode = 1) \end{cases}$$

$$f_3 = \overline{x_2}x_3x_4 \; + \; x_2\overline{x_3x_4}$$

$$f_4 = x_3 \oplus x_2$$

The f_4 signal and the f_3 signal are exactly the same in both radix-4 and radix-8 modes. A circuit which generates the f_1 signal is composed of one MUX. Also the f_2 signal generation circuit has the same architecture as the f_3 signal generation circuit except a tri-state buffer at the end.

III. GDI Circuit Methodology

The GDI method [6]–[7] is based on the simple cell shown in Figure 3. At a first glance the basic cell resembles the standard CMOS inverter, but there are some important differences: The GDI cell contains four terminals – G (the common gate input of the nMOS and pMOS transistors), P (the outer diffusion node of the pMOS transistor), N (the outer diffusion node of the nMOS transistor) and the D node (the common diffusion of both transistors). P, N, and D may be used as either input or output ports, depending on the circuit structure.

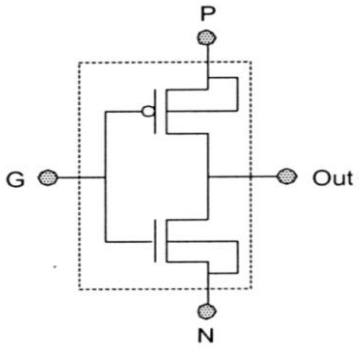

Figure 3. GDI basic cell

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics. Multiple-input gates can be implemented by combining several GDI cells.

TABLE 1
Logic functions that can be implemented with a single GDI cell

N	P	G	D	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

Table I shows an example of how simple configuration changes of the inputs P, N, and G in the basic GDI cell correspond to very different Boolean functions at the output D. Most of these functions require a complex (6-12 transistors) gate in CMOS (as well as in standard PTL implementations [8]), but are very simple (only two transistors per function) in the GDI design methodology.

IV. Conventional CMOS Radix-4/-8 Dual Encoder

All the used sub-circuits used to make the conventional CMOS radix 4/8 dual encoder architecture are being implemented using CMOS style. The transistor count for the conventional CMOS dual encoder is 86. Its area is very large as a result it is more complicated, consumes more power and has slow speed. Schematic and output waveforms of CMOS dual encoder is shown in figure 4(a) and figure 4(b) respectively.

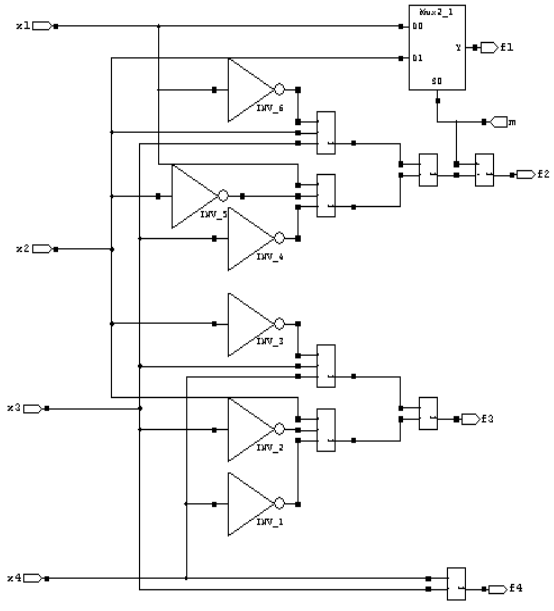

Figure 4 (a) Schematic of CMOS dual encoder

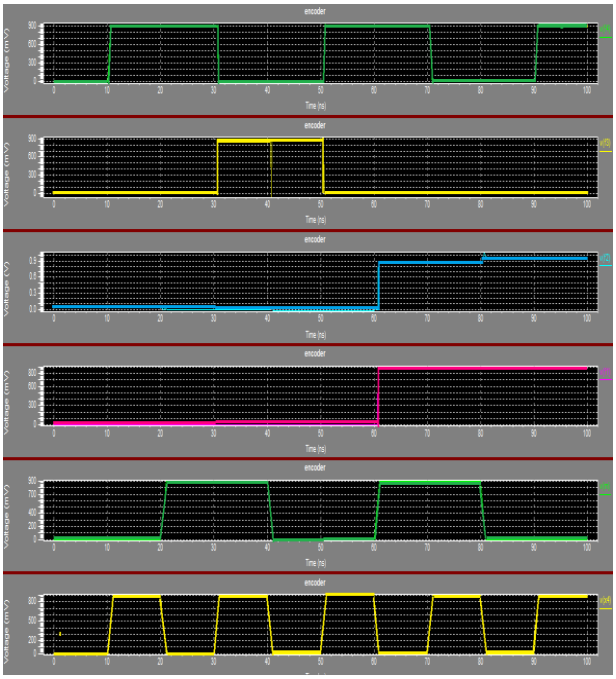

Figure 4(b) Waveforms of CMOS dual encoder

Figure 5(b) Waveforms of GDI dual encoder

V. PROPOSED GDI RADIX-4/-8 DUAL ENCODER

All the used sub-circuits used to make the GDI radix 4/8 dual encoder architecture are being implemented using GDI technique. The transistor count for the GDI dual encoder is 46. Its area is small as compared to conventional CMOS dual encoder as a result it consumes less power and has higher speed with the expense of less voltage output swing. Schematic and output waveforms of GDI dual encoder is shown in figure 5(a) and figure 5(b) respectively.

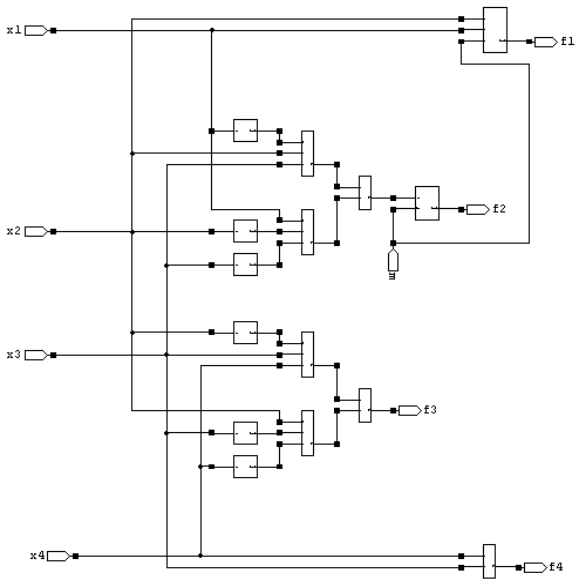

Figure 5(a) Schematic of GDI dual encoder

VI. EXPERIMENTAL RESULT

Table II shows implementation results including the proposed encoder's hardware area, critical path delay, and power consumption compared to previous work. The multiplication of power and propagation delay means energy. [2] [3] [5]. As a result, the proposed GDI radix-4/-8 encoder architecture consumes 43.6% less power, and 46.51% less area and 3.3% less delay time compared to previous work [1].

The proposed GDI radix-4/-8 8x8 dual encoder architecture is implemented using a Tanner EDA 13.0 tool at 1.8 V nominal operating voltage.

TALBE II Experimental results of radix 4/8 dual encoder

Dual Encoder Using	No. of transistors	Power (w)	Delay (ns)
CMOS Style	86	4.515×10^{-8}	10.67
GDI Technique	46	2.543×10^{-8}	10.31

VII. CONCLUSION

A GDI radix-4/8 dual encoder architecture which is proposed in this paper is an appropriate solution for multiplier because it is both low-power and high-speed and less area. This proposed hybrid radix-4/8 GDI dual

encoder architecture dissipates 43.6% less power, and 46.51% less area and 3.3% as compared to the conventional CMOS radix-4/-8 dual encoder architecture.

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