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A Low-Quiescent Current Two- Input/Output Buffer with Class A-B Output Stage for LCD Driver

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Abstract— the evolution of compact, light-weight, low-power, and high-quality displays has caused a large demand for liquid crystal display (LCD) drivers, with features such as low cost, low power dissipation, high speed, and high resolution. we propose a low–Quiescent current Two-Input/Output buffer with class A-B output stage for LCD driver applications. The propose buffer amplifier achieve high speed driving performance, draws a small quiescent current during static operation and offer a rail to rail communication-mode input rang Two-Input/Output buffer with class A-B output stage for LCD driver. A current reuse technique is employed in the output stage of the buffer amplifier to reduce the quiescent current consumption. An experimental prototype 6-bit LCD column driver with the proposed buffer amplifiers implemented in a 0.35-µm CMOS technology demonstrates that an average value of 0.2 µA static current is consumed in one channel driver. The settling time to settle within 0.15% of the final voltage is 4 µs under a 30-KΩ- resistance and 2-pF-capacitance load. The area of this two input/ output buffer amplifier is 18 µm × 170µm.

Index Terms—Buffer Amplifier, Digital to Analog converters, LCDs column drivers, dot inversion

I. INTRODUCTION

The block diagram of the proposed column driver architecture with a dot inversion method shows in fig. 1. A charge recycler is attached to a typical column driver for low-power operation. Digital display data are presented at the RGB inputs and sampled into the input register with enable signals from the shift register. DIR, DEN1, and DEN2 are provided to select and load only one pixel data per pixel clock (CLK). A wide data latch presents one line of serially input pixel data to digital-to-analog converters (DAC's) after all pixel data in the line are loaded in the input register. In the DAC, a voltage level corresponding to a digital pixel data is selected out of all possible analog voltage levels. A resistor string is normally used to generate such analog levels by interpolating from a set of externally driven reference levels. Voltage followers made of operational amplifiers can be used to drive highly capacitive column lines fast but incur extra power dissipation. In the proposed column driver, the last block Called a charge recycler is added to an aforementioned conventional column driver, and it is the concern of this paper. Power dissipation in a conventional amplifier-based column driver is composed of three parts. One is the power dissipation of the digital part. Because its function is very simple, it is usually less than 1/10 of the power dissipation of the output driver, so it can be ignored. The second is the static

power due to dc bias current to resistor strings and amplifiers used in voltage followers. Static power dissipation also is usually much smaller than that of the output driver. Its reduction is not straightforward since it is determined by the tradeoff between settling time and bias current. The last but the most important part is the dynamic power consumed in charging capacitive outputs.

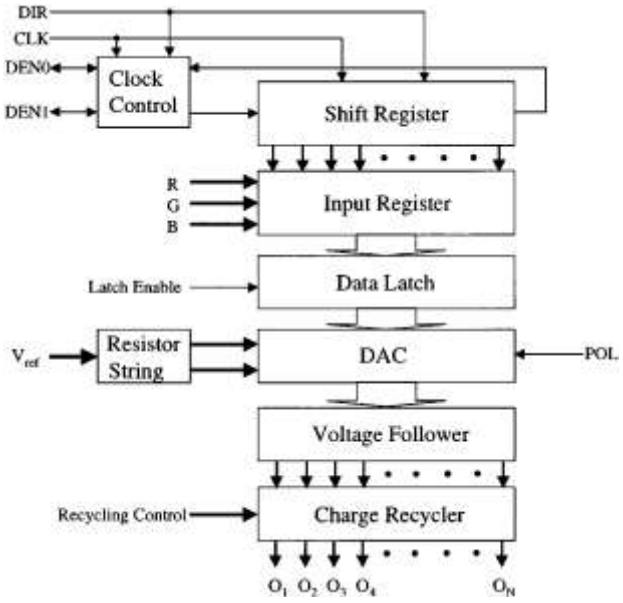

Figure 1-block diagram of the LCD column drive

II. DRIVING SCHEME OF BUFFER AMPLIFIER

Two channels of driving circuits, in which one channel takes the responsibility for driving negative polarity and the other for driving positive polarity, are grouped to drive a pair of adjacent column lines. PMOS input buffers are used to drive positive-to-negative polarity operation. NMOS input buffers are used for the transition of negative-to-positive polarity. The PMOS input buffers have a large discharge capability and vice versa for the NMOS input buffers. In this work, we combine these two buffers as a two-input/output buffer amplifier. A current reuse technique is employed in the proposed buffer amplifier to reduce the quiescent power consumption. Figure 2 shows the driving method.

The LCD output buffers are mostly realized by operational transconductance amplifiers in unity-gain configuration, and are typically used to drive the highly capacitive column lines of the display panel. Moreover, as a high open-loop gain is required to obtain a low-valued systematic offset voltage, a two-stage amplifier architecture is traditionally adopted in the LCD driver .Since the additional Miller capacitance required for frequency compensation would involve a sensible silicon area consumption, most recently proposed amplifiers achieve stability by exploiting dominant-pole compensation at the high capacitive- impedance output node. However, to

provide high speed driving capabilities to the output stage, a few additional current comparators are usually included in the basic two-stage amplifier topology, hence requiring some extra quiescent current from the power supply. This work suggests a new compact low-power class-AB buffer amplifier for large-size LCD applications. The proposed buffer provides a remarkable power efficiency improvement compared to other previously reported solutions, as both current comparators are freely incorporated into the input differential stage.

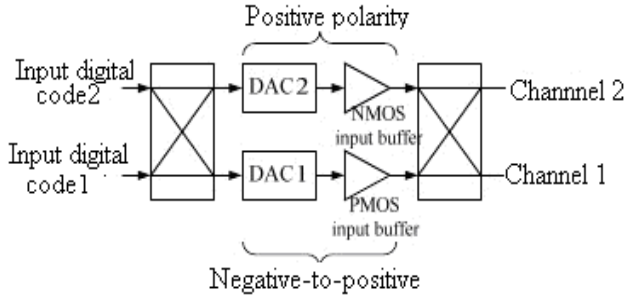

Figure 2. A rail-to-rail dot-inversion driving scheme

III. *ANALYSIS OF A TYPICAL TWO-STAGE OP AMP*

A class-AB op-amp is usually connected to a unity buffer for driving highly capacitive column lines of the display panel. Because the buffer amplifiers are required to have a high open-loop gain to obtain a low value of the systematic offset voltage, a two-stage amplifier is usually used in LCD drivers. A two-stage amplifier requires compensation for stability. Some buffer amplifiers adopt the output node as a dominant pole to achieve enough stability without a Miller capacitance [3, 6]. However, a charge conservation technique is commonly used in some LCD drivers to reduce the dynamic power dissipation [7]. Before a new scanning driving, all column lines are isolated from the buffers. Since the buffer amplifiers experience no load for a period of time, these amplifiers require the Miller compensation. Figure 3 shows an equivalent circuit of a typical two-stage op amp where gm1 and gm2 are the transconductance of the first and second stages, respectively; rO1 and rO2 are the output resistances of the first and second stages, respectively; CO1 and CO2 are the parasitic capacitances at output nodes of the first and second stages, respectively; CC is the Miller compensation capacitor; and RL and CL are resistive and capacitive loads, respectively. The open-loop transfer function, AO(s), can be obtained from Figure 3. That is:

$$A_o(s) = \frac{A_{dc}\left(1+\frac{S}{\omega_{z1}}\right)\left(1+\frac{S}{\omega_{z2}}\right)}{\left(1+\frac{S}{\omega_{p1}}\right)\left(1+\frac{S}{\omega_{p2}}\right)\left(1+\frac{S}{\omega_{p3}}\right)} \quad (1)$$

Where

$$A_{dc} = g_{m1}g_{m2}r_{o1}r_{o2} \quad (2)$$

$$\omega_{z1} = \frac{1}{C_L R_L} \quad (3)$$

$$\omega_{z2} = \frac{g_{m2}}{C_C} \quad (4)$$

$$\omega_{p1} = \frac{1}{r_{o1}r_{o2}g_{m2}+C_L r_{o2}} \quad (5)$$

$$\omega_{p2} = \frac{C_C g_{m2}+C_L/r_{o1}}{C_C C_L} \quad (6)$$

$$\omega_{p3} = \frac{1}{(C_{o1}+C_{o2})R_L} \quad (7)$$

The unity gain Frequency is

$$\omega_{p2} = \frac{g_{m1}g_{m2}}{C_C g_{m2}+C_L/r_{o1}} \quad (8)$$

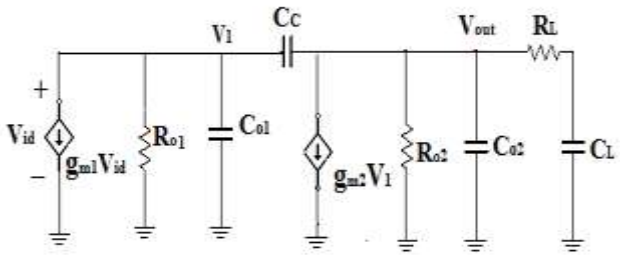

Figure 3 Equivalent circuit of a two-stage op amp.

The equivalent circuit contains three poles. However, the third pole is far away from the other poles and zeros, so it is insignificantly affect the phase margin. The zero of ω*Z1* compensates for the pole of ω*P2*. If the buffer amplifier is operated under no load, the open-loop transfer function, $A_o(s)$, can be expressed as:

$$A_o(s) = A_{dc}\frac{\left(1+\frac{S}{\omega_z}\right)}{\left(1+\frac{S}{\omega_{p1}}\right)\left(1+\frac{S}{\omega_{p2}}\right)} \quad (9)$$

Where

$$A_{dc} = g_{m1}g_{m2}r_{o1}r_{o2} \quad (10)$$

$$\omega_z = \frac{g_{m2}}{C_C} \quad (11)$$

$$\omega_{p1} = \frac{1}{r_{o1}r_{o2}g_{m2}C_C} \quad (12)$$

$$\omega_{p2} = \frac{g_{m2}}{C_{O1}+C_{O2}} \quad (13)$$

The zero of ω*Z* is a negative value, so it can not compensate for the pole of ω. The open-loop frequency characteristic of a two-stage op amp with/without *CL* and *RL* loads where the solid line and dashed line show the frequency characteristics

with and without *CL* and *RL* loads, respectively. The phase margin of the op amp can be calculated from the equations below.

IV. DRIVER ARCHITECTURE FOR LARGE-AREA PANELS

The development of improved multi domain IPS and VA pixel structures has been the key point to obtain wide viewing angles for large-area LCDs. However, every new mode of operation must provide its improvements while maintaining the same simple pixel driving scheme, with one gate line, one source line and one common line, as well as a standard timing controller.

We already know that large-size high-resolution displays cannot take advantage of the LTPS technology, because of the large spread in the electrical characteristics of individual LTPS TFTs over the substrate area and kink effect. In contrast, the same advantages deriving form the integration of Si-gate drivers could be in principle obtained also on large-area LCDs, but two main technological issues must be solved. One is the instability of a-Si-TFTs, due to bias stress from an applied-voltage bias during circuit operation, causing a change in the TFT characteristics. The other is the required large width of the- Si TFTs, extended to thousands of micrometers due to the low electrical mobility and high capacitive load of large-area panels.

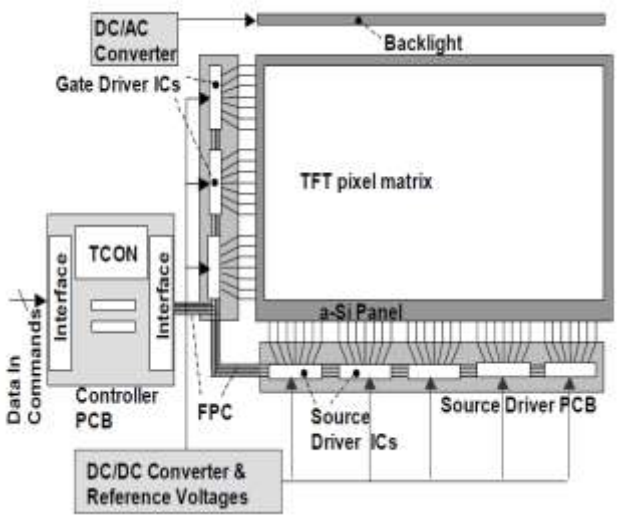

Figure 4 block diagram where a Controller Board

As already anticipated, large-area LCDs adopt typically a multi-IC driver architecture. Figure 4 shows a block diagram where a Controller Board, including I/O Interfaces, Timing Controller (TCON), DC/DC converter, and Parallel-to-Serial decoders, is connected via a parallel bus to the Gate Driver (row driver) and Source Driver (Column driver) sections without the need, as early observed, of a video RAM. The TCON PCB, Gate Driver PCB, and Source Driver PCB are connected together through a Flexible Printed Circuit (FPC).

Passive Matrix -In a passive matrix, or FSTN, display a grid of electronic control wires or lines are placed on the front and back glass. A pixel is located at the junction of each row and column control lines. Passive matrix displays use one transistor to address each row and one to address each column of pixels. Pixels are turned on when both row and column lines are energized and off when both control lines are de-energized. This addressing scheme is called multiplexing. The residual electrical current that travels down each control line can cause crosstalk at unselected pixels. Crosstalk partially darkens pixels and lowers the display's overall contrast. This usually appears on a passive matrix PowerBook display as two dark boxes, parallel to each other on the display.

Active Matrix - The active matrix or Thin-Film Transistor (TFT) display is the latest technology used in Macintosh Power Book computers. Rather than using multiplexing (row and column wires on the glass) techniques to address the matrix of crystals, the active matrix LCD includes a transistor fabricated along with each pixel. You can think of the display as one large Integrated Circuit (IC), with the transistors acting as switches to turn on individual pixels. (An IC is a slice or chip of material on which is etched or imprinted a circuit comprised of electronic components and their interconnections.) Because of the transistors, pixels can be turned on and off at a very fast rate. The transistor at each pixel eliminates the crosstalk phenomenon, which lowers contrast on an FSTN display. The TFT method eliminates the time dependency associated with multiplexed displays by directly addressing each pixel.

IV. MEASUREMENT RESULTS.

The Schematic of the Two-Input/Output buffer with class A-B output stage for LCD driver shown in figure-5. The proposed circuit was fabricated using 0.35-µm CMOS technology demonstrates that an average value of 0.2 µA static current is consumed in one channel driver. The settling time to settle within 0.15% of the final voltage is 4 µs under a 30-KΩ resistance and 2-pF capacitance load. The area of this two input/ output buffer amplifier is 18 µm × 170µm. The Two-Inputs of of the proposed buffer amplifier is shown in Fig.6. The Two-Outputs of the proposed buffer amplifier is shown in Fig.7 and the input/output voltage of Two-Input/Output buffer with class A-B output stage for LCD driver is shown in Fig.8.

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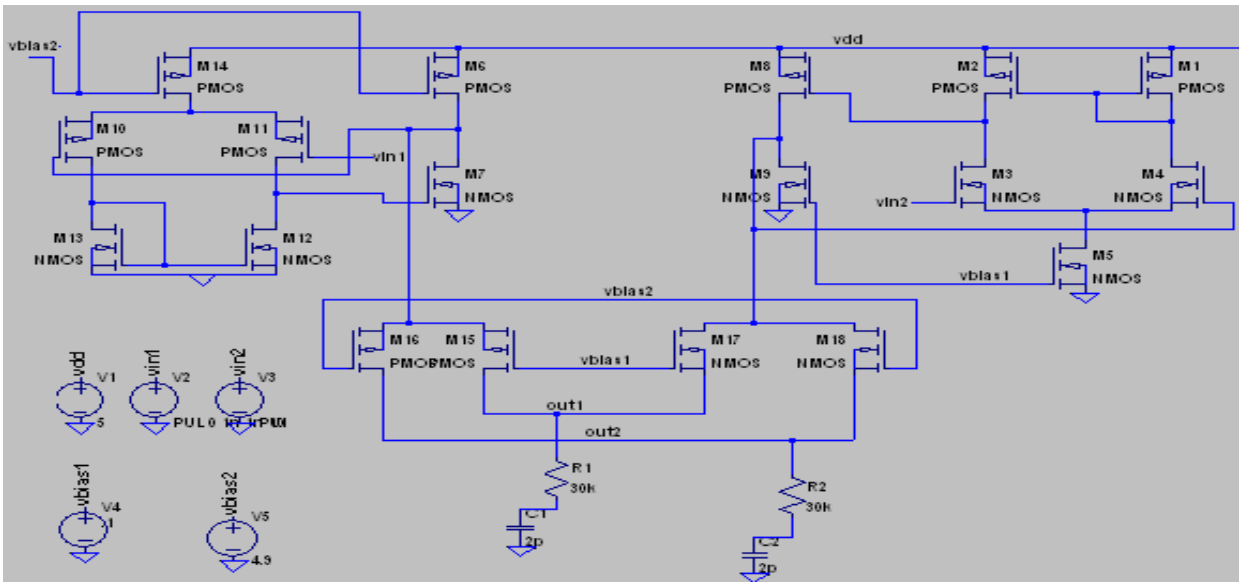

Figure 5 -Schematic of the proposed buffer amplifier.

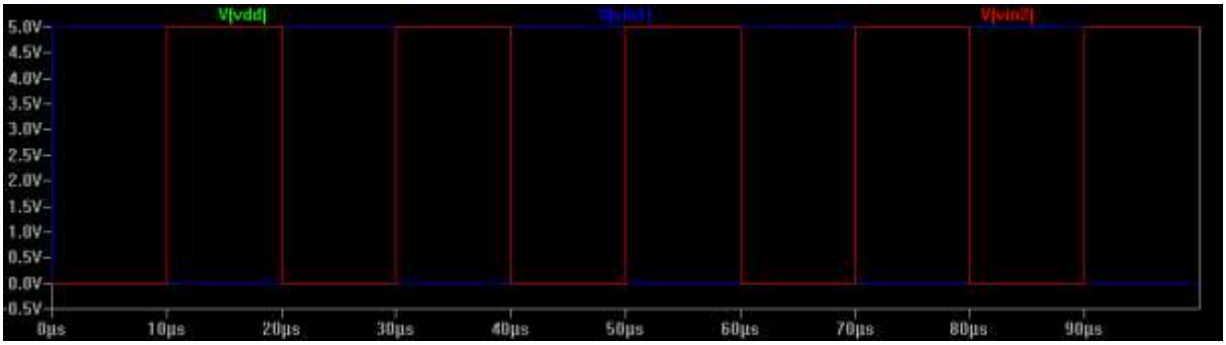

Figure 6-Two-Inputs of of the proposed buffer amplifier.

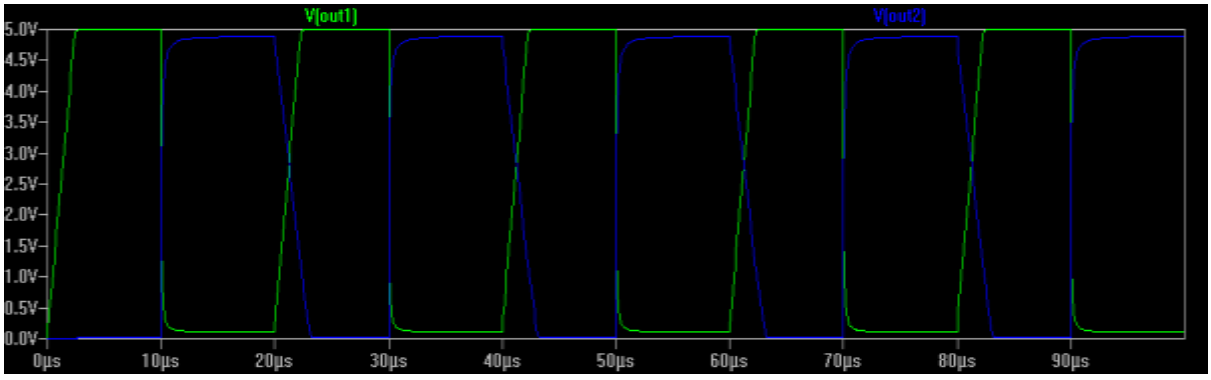

Figure 7-Two- Output of the proposed buffer amplifier.

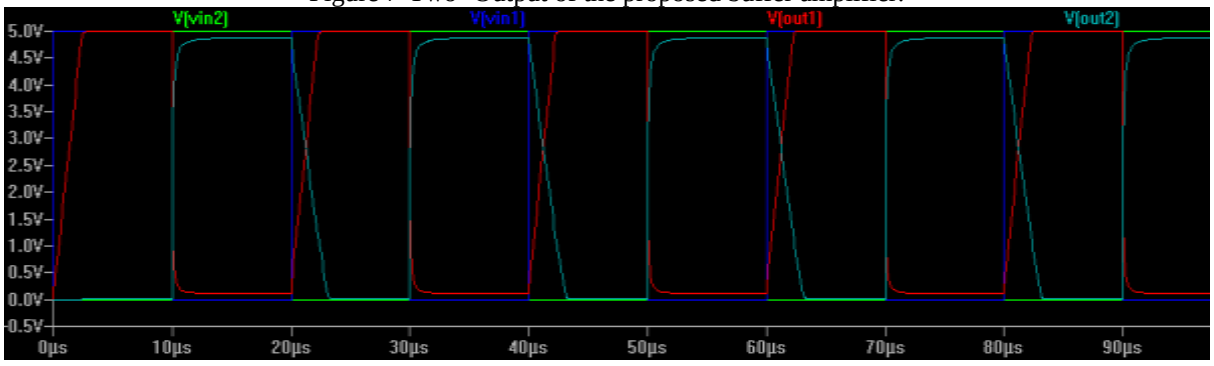

Figure 8 - Two-Input/Output of the proposed buffer amplifier

TABLE- I

Performance comparison with existing buffer amplifiers for LCD column drivers

	This work	[2]	[3]	[4]
Process tech.	0.35 µm CMOS	0.13µm CMOS	0.35-µm CMOS	0.35µm CMOS
VDD	5 V	5 V	3.3 V	5 V
Quiescent current	0.2 µA/ channel	2 µA	7.4 µA	NA
Loads	RL=30KΩ CL = 2 pF	RL=10KΩ CL=24 pF	CL= 600 pF	CL = 400 pF
Settling time	6µs (0.2%)	1.95 µs (10mV)	8 µs (0.2%)	0.95 µs
Area	18 µm ×170 µm (two channels)	100µm × 45µm	100 µm × 45µm	100µm × 45 µm

V. CONCLUSIONS

A Low-Quiescent Current Two- Input/Output Buffer with Class A-B Output Stage for LCD Driver. The Fundamental Requirements of buffer amplifier in column driver that support dot-inversion LCD column drivers were analytically define. The performance criteria and corresponding design specification for buffer amplifier for commercial state-of-the-art column driver IC was proposed. The proposed buffer amplifier was implemented in a 0.35-µm CMOS technology with 0.4µA Quiescent current and exhibit the settling time of 6µs of the finial voltage under a 30 kΩ and a 2 pF capacitance loads. The area of this two input/ output buffer amplifier is 18 µm ×170 µm.

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