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Performance Analysis of Different Parallel CMOS Adders and Effect of Channel Width at 0.18um

Akanksha Mandowara, Mukesh Maheshwari

Abstract— **This paper investigates the designs of various adders implemented using CMOS technology like Full Adder, Carry select Adder, Ripple Carry Adder and Look-Ahead Carry Adder. Simulation is done using Tanner Tool at 0.18um, Addition time is critical to the design of a CPU. Mostly adders occupy critical path in many areas of microprocessor operation. There is a necessity of Fast adders in ALUs, for computing memory addresses, and in floating point calculations. Therefore, careful optimization of the adder is of the utmost importance. This optimization can be done either in the logic or circuit level way. Circuit optimizations manipulate transistor sizes and circuit topology to optimize the speed circuit is obtained. The designs are constrained by the factors such as maximum logic stages allowed for the design of a particular adder, fan-out restrictions, regularity of the design, etc. An extensive comparison of all designs is also reported in this paper to provide guidelines for the designers of adders. In particular, comparisons are made in terms of delay and area, where time is measured in terms of gate and transistor delays and area is measured in terms of number of gates of transistors required for the implementation. The comparative analysis will help designers to a have a better understanding of design metric (Power, Speed, Area) and to choose between trade-off of design. It has also been observed that by changing the width of CMOS, the delay parameter is improved if we move towards the ideal condition, whereas increasing the width drastically increases the size of CMOS used.**

***Index Terms*—Adders, CMOS, Fan-out, Tanner EDA .**

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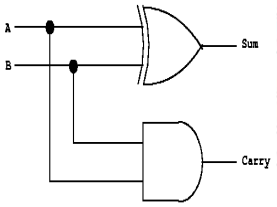
I. INTRODUCTION

Addition is the most common and often used arithmetic operation in microprocessor[1-5], digital signal processor, especially digital computers. Also, it serves as a building block for synthesis of all other arithmetic operations in the arithmetic logic unit. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. Recently different design techniques have been proposed in order to enhance the performance through different circuit design. The biggest challenge is to reduce the adder power consumption while maintaining the high performance in different types of circuit design. Up until now, the power consumption has not been of great concern because of the availability of large packages and other cooling techniques having the capability of dissipating the generated heat. However, continuously increasing density as well as the size of the chips and systems might cause to difficulty in providing adequate cooling and hence, might either add significant cost to the system or provide a limit on the amount of the functionality that can be provided [1].This arises the need of usin Area and Power efficient VLSI circuits[2,6-9] .Adder is a digital circuit or a device that performs addition of two or more binary inputs. In computers, adders reside in the arithmetic logic unit (ALU) where other arithmetic and logical operations are performed. High speed Adder cells are used in battery operated devices[10-12]The core of arithmetic logic unit is adder. Therefore a high performance adder is essential to maximize the speed of a process. Thus, there is a critical need in VLSI design methodology to improve the performance on the matrix of speed, power. In the following section, we give a brief description of the studied adder architectures. The first class consists of the Half adders and Full adders. The second class consists of the very slow Ripple-Carry adder with the smallest area. In the third class, we studied about the Carry-Select adder having small area requirements and shortened computation times[14]. From the fourth class, the Carry-look Ahead adder is studied.

1. Half & Full Adder
2. Ripple Carry Adder
3. Carry Select Adder
4. Look Ahead Carry Adder

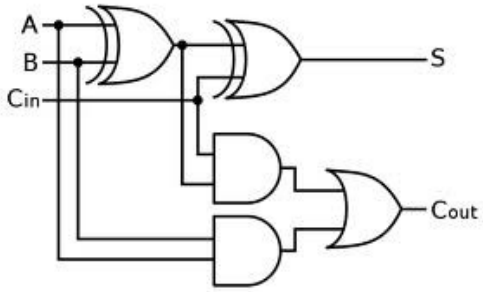
Half Adder-. Half adder is a logical circuit that performs an addition operation on two one-bit binary numbers. The half adder output is a sum of the two inputs usually represented with Carry and Sum. A half adder can add only two binary digits.



Inputs		Outputs	
A	B	Sum(S)	Carry(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 1.1 Half adder circuit and truth table

Full Adder-- Full Adder is a logic circuit that adds a pair of corresponding bits of two numbers expressed in binary form and any carry from a previous stage producing a sum and a new carry. It is also called a three input adder.



Input bit for number A	Input bit for number B	Carry bit input C_{IN}	Sum bit output S	Carry bit output C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 1.2 Full adder circuit and truth table

Ripple Adder- A simple ripple carry adder (RCA) is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain.The main problem with this type of adder is the delay needed to produce the carry out signal and the most significant bit[15].

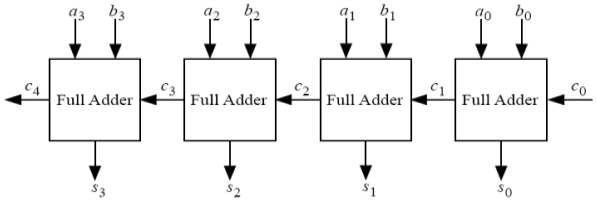


Figure 1.3 Ripple Adder

Carry Select Adder- A carry-select adder is a particular way to implement an adder, which is a logic element that computes the -bit sum of two -bit numbers. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known.

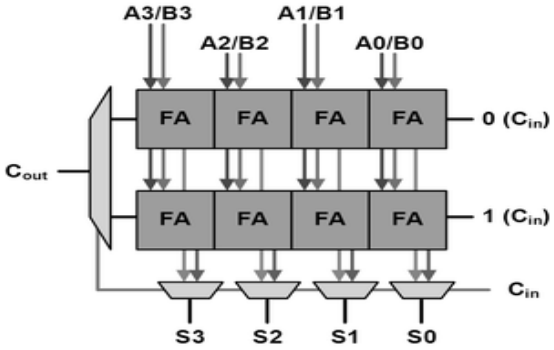


Figure 1.5 Carry Select Adder

Carry Look Ahead Adder- The carry look-ahead adder solves the carry delay problem by calculating the carry signals in advance, based on the input signals. It is based on the fact that a carry signal will be generated in two cases: (1) when both bits a and b are 1, or (2) when one of the two bits is 1 and the carry-in is 1. Thus we get theses relations[15]

$$c_{i+1} = a_i.b_i + (a_i \oplus b_i).c_i \quad (1)$$

$$S_i = (a_i \oplus b_i) \oplus c_i \quad (2)$$

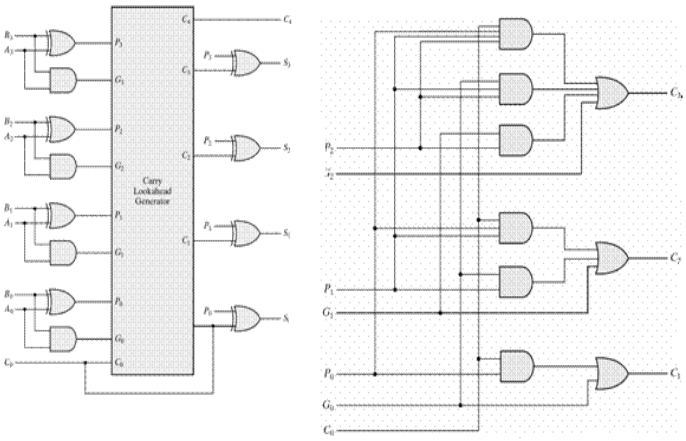


Figure 1.5 Carry Look Ahead Adder

II. Implementation & simulation

We designed different Logic gates using Tanner tool, and then after generating their symbols, different Adders are designed.

Basic Logic gates designed are the following:

NOT Gate:

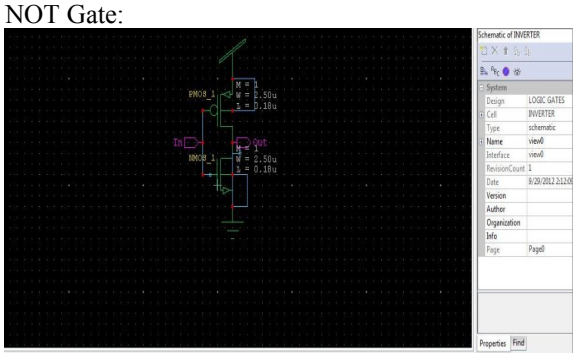


Figure 2.1(a)

AND Gate:

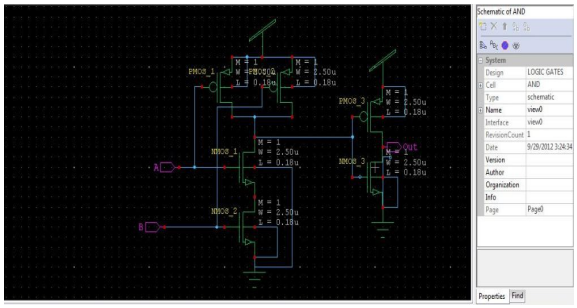


Figure 2.1(b)

OR Gate:

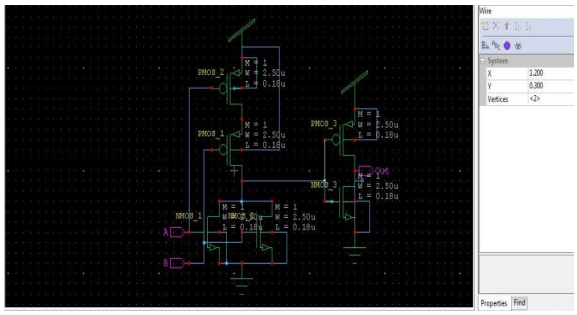


Figure 2.1(c)

XOR Gate:

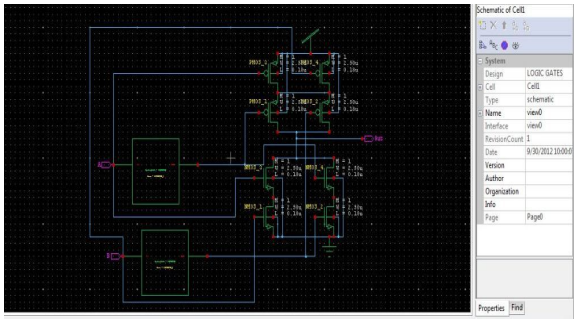


Figure 2.1(d)

Half Adder:

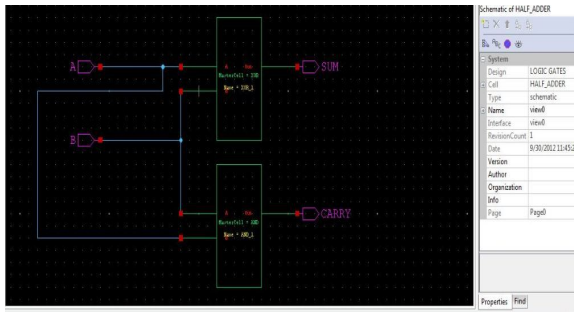


Figure 2.1(e)

Half adder: Sum= A XOR B
Carry = A AND B

Full adder: 1-Bit Full Adder logic function

Sum = A XOR B XOR C

= ABC + AB'C' + A'BC' + A'B'C

Carry_out = AB + AC + BC

Sum = ABC + (A + B + C) ·carry_out'

This alternate representation of the sum function allows the 1-bit full adder to be implemented in complex CMOS with 28 transistors, as shown below.

Full adder:

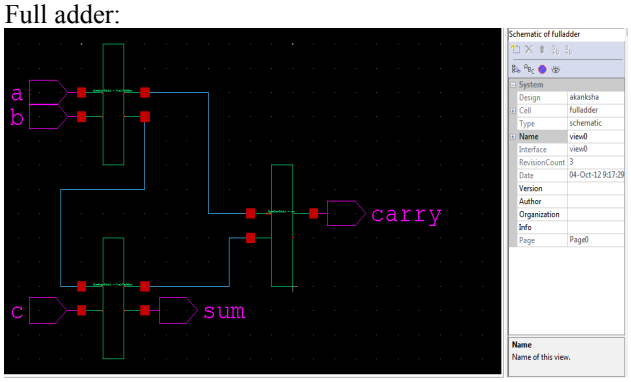


Figure 2.2 Schematic of full Adder

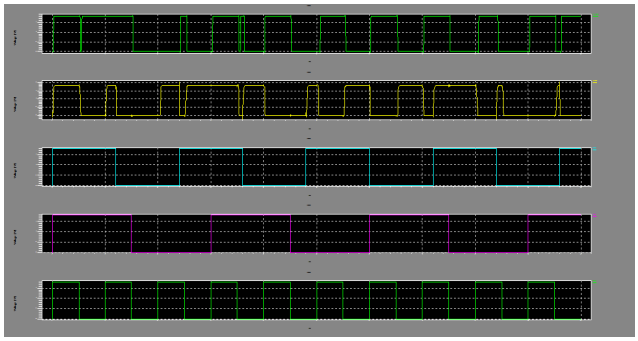


Figure 2.3 Output wave form of full Adder

Ripple carry adder:

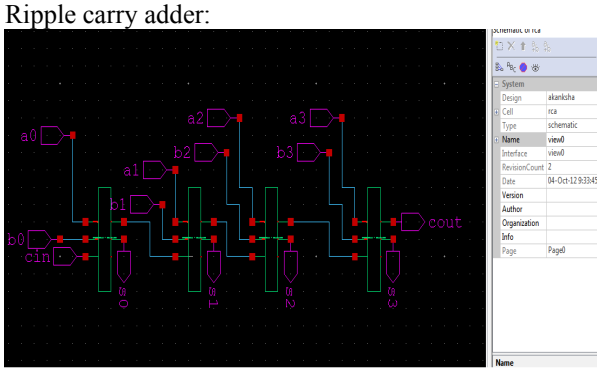


Figure 2.4 Schematic of Ripple Carry Adder

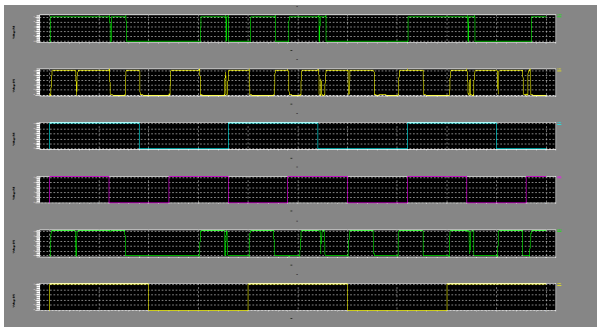


Figure 2.5 Output wave form of Ripple Carry Adder

Carry Select Adder:

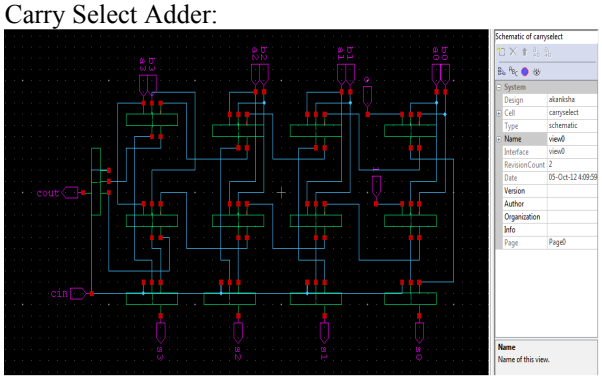


Figure 2.6 Schematic of Carry Select Adder

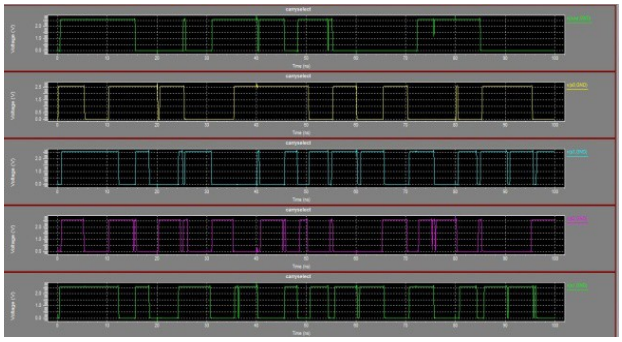
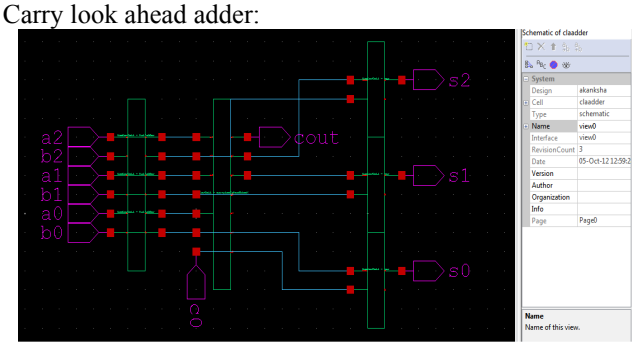


Figure 2.7 Output wave form of Carry Select Adder

Carry look ahead adder:



2.8 Schematic Carry Look Ahead Adder

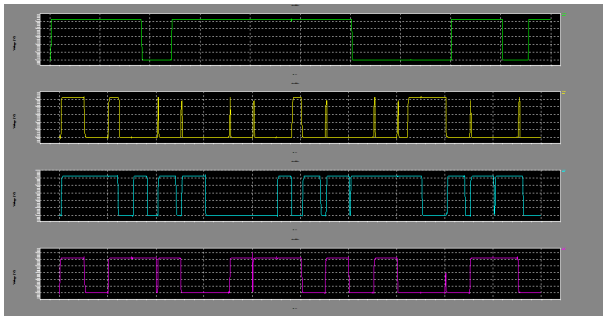


Figure 2.9 Output waveform of Carry Look Ahead Adder

III. VARIATION OF POWER DISSIPATION AND DELAY WITH RESPECT TO POWER SUPPLY IN DIFFERENT ADDER

Full Adder:

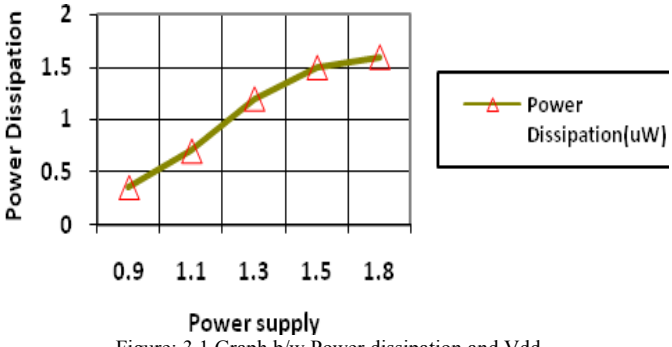


Figure: 3.1 Graph b/w Power dissipation and Vdd

Delay, PDP vs Power Supply

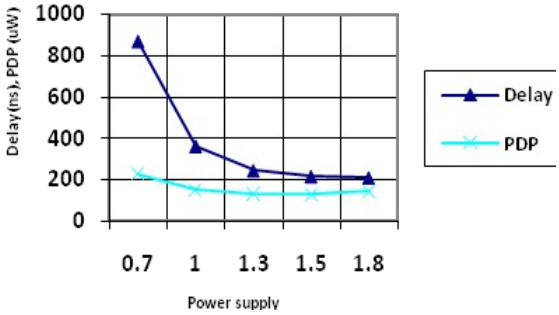


Figure: 3.2 Graph b/w Power dissipation, Delay and Vdd

Ripple Carry Adder:

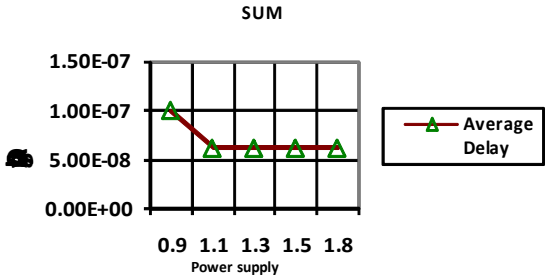


Figure: 3.3 Graph b/w Avg Delay and Vdd for sum

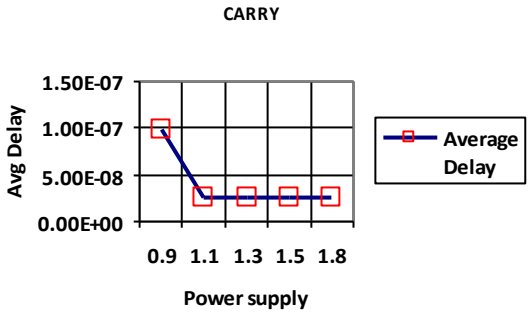


Figure: 3.4 Graph b/w Avg Delay and Vdd for carry

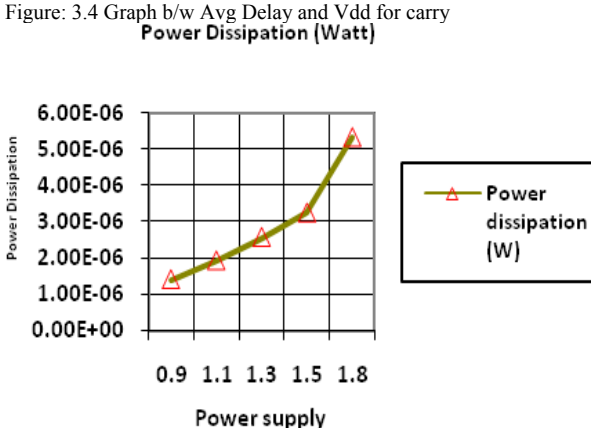


Figure: 3.5 Graph b/w Power dissipation and Vdd

Carry Select Adder :

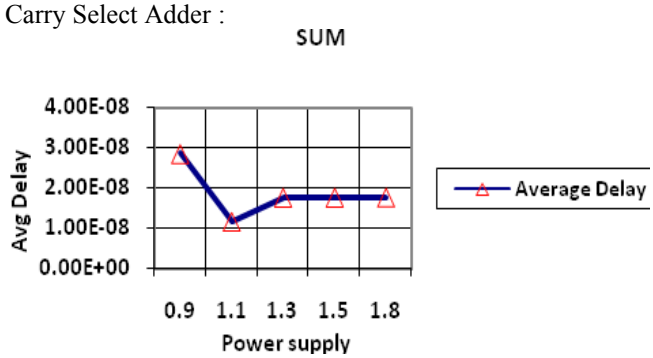


Figure: 3.5 Graph b/w Avg. Delay and Vdd for sum

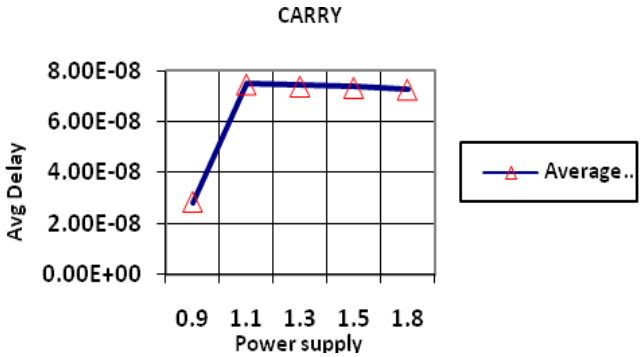


Figure: 3.6 Graph b/w Avg. Delay and Vdd for carry

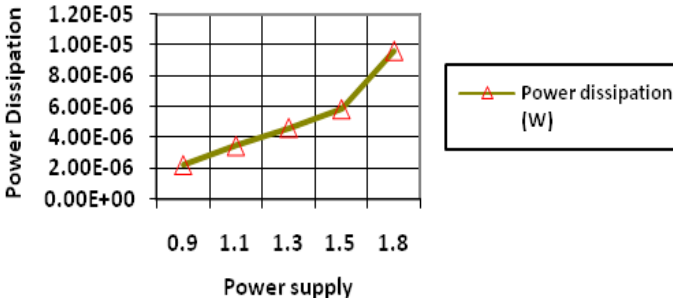


Figure: 3.7 Graph b/w Power dissipation and Vdd for carry select adder

Carry Look Ahead Adder:

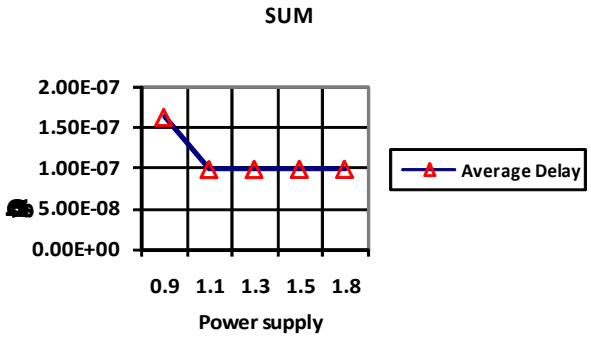


Figure: 3.8 Graph b/w Avg. Delay and Vdd for sum 1

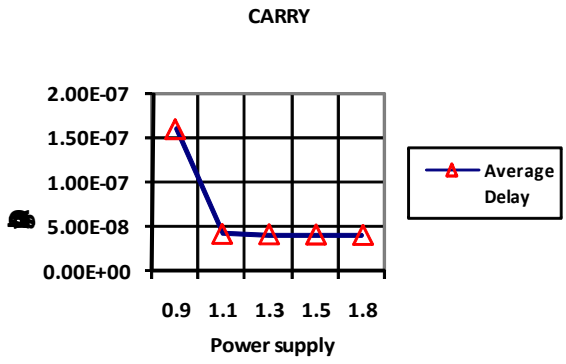


Figure: 3.9 Graph b/w Avg. Delay and Vdd for carry

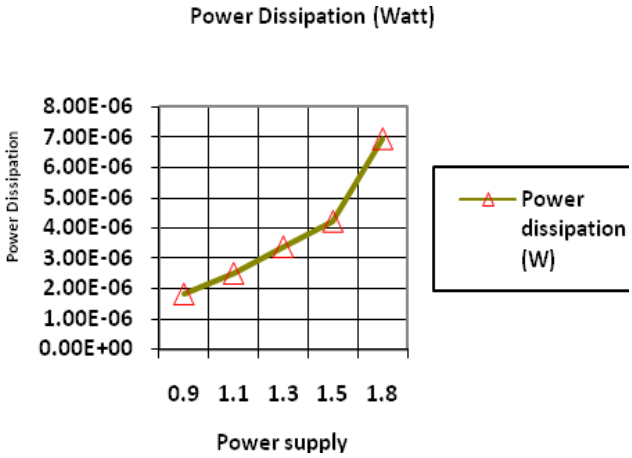


Figure: 3.10 Graph b/w Power dissipation and Vdd for CLA adder

IV. THE RIPPLE ADDER WITH SIZING

Given the power supply voltage V_{DD}, the nMOS and the pMOS transistor threshold voltages, and the desired inverter threshold voltage V_{th}, the corresponding ratio K_r can be written as:

$$\sqrt{\frac{1}{Kr}} = \frac{Vth - Vt0,n}{VDD + Vt0,p - Vth}$$

Recall that the switching threshold voltage of an ideal inverter is defined as:

$$V_{th,ideal} = \frac{1}{2} V_{DD}$$

$$K_r = (K_n / K_p)_{ideal} = \left(\frac{0.5\,VDD + Vt0,p}{0.5VDD - Vt0,n}\right)2$$

Assuming that the gate oxide thickness t_{ox}, and hence, the gate oxide capacitance C_{ox} have the same value for both nMOS and pMOS transistors. The unity ratio condition for the ideal symmetric inverter requires that

$$\frac{(W/L)n}{(\frac{W}{L})p} = \frac{\mu p}{\mu n} = \frac{\frac{280cm2}{Vs}}{580cm2/Vs}$$

Hence
$(W/L)_p = 2.5(W/L)_n$
Now we are optimizing width:
Old width NMOS: 0.27
New width NMOS: 0.54
Old width PMOS: 0 .81
New width PMOS: 1.38

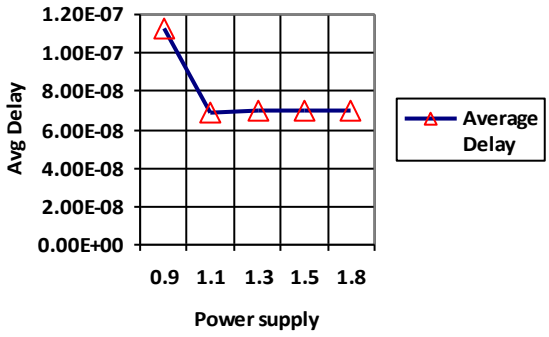


Figure: 4.1 Graph b/w Avg. Delay and Vdd for Sum

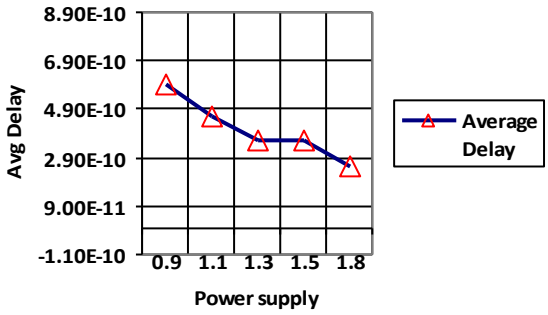


Figure: 4.2 Graph b/w Avg. Delay and Vdd for Carry

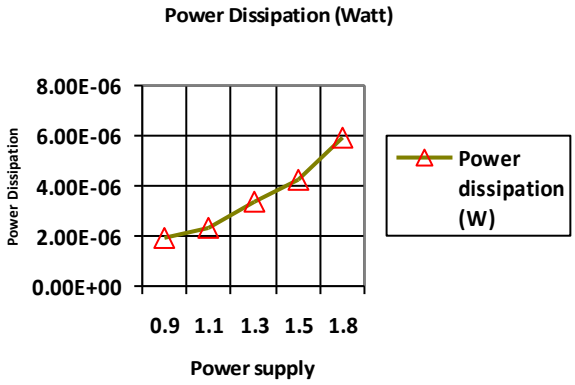


Figure: 4.3 Graph b/w Power dissipation and Vdd for resize ripple adder

V. CONCLUSION

In this paper, different type of adders (Ripple carry, Carry skip and Carry look ahead) has been designed and evaluated on power, delay and area parameter. Simulation results have been presented for the Ripple adder, Carry skip adder and Carry look ahead adder.

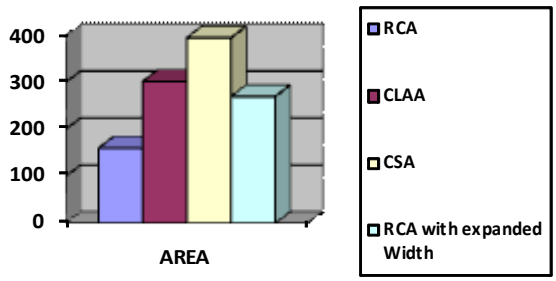


Figure: 5.1(a) Graph showing comparision among different adders in terms of Area

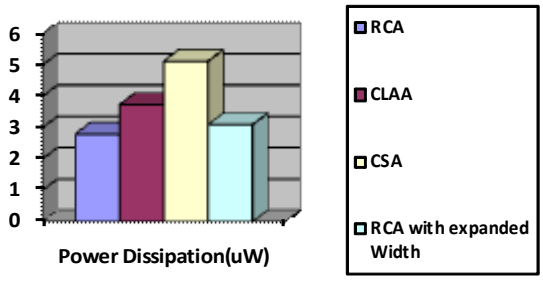


Figure: 5.1(b) Graph showing comparision among different adders in terms of Power dissipation

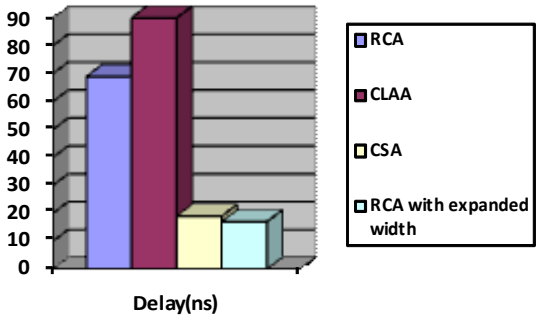


Figure: 5.1(c) Graph showing comparision among different adders in terms of Delay

As shown in the figures, Ripple carry adder consumes minimum power. Carry select adder has minimum delay. So, it is the fastest adder but takes maximum area. Carry look ahead adder consumes less power than carry select adder but more than ripple carry adder. Carry look ahead adder has maximum delay. It is the slowest adder family. Now we have achieved best possible combination by optimizing Ripple carry adder by modifying width of NMOS and PMOS.

This modified family has minimum delay among all family but at the cost of area. Every family has its merits and demerits. According to our applications, we can select different adder architecture. Area analysis is based on no. of Transistors used in one schematic. The primary uses of adders are in CPU design.

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