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Design & implementation of FPGA based digital filters

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Abstract-**Implementing hardware design in Field Programmable Gate Arrays (FPGAs) is a formidable task. There is more than one way to implement the dsp design for digital FIR filter. Based on the design specification, careful choice of implementation method and tools can save a lot of time and work. There are toolboxes available to generate VHDL (Verilog) descriptions of the filters which reduce dramatically the time required to generate a solution. Time can be spent valuating different implementation alternatives. Proper choice of the computation algorithms can help the FPGA architecture to make it efficient in terms of speed and/or area.**

Keywords-**Multiplier and accumulator, Booth algorithm, Booth Multiplier, Booth Wallace Multiplier, Adaptive Lattice Filter, Fir filter, Median filter, IIR filter.**

I. INTRODUCTION

Adaptive filters have become vastly popular in the area of digital signal processing. Adaptive direct modeling or system identification and adaptive inverse modeling or channel equalization find extensive applications in telecommunication, control system, instrumentation, power system engineering and geophysics.

Filter adds more noise to signal, the digital filter performs noiseless mathematical operations at each intermediate step in the transform. As the digital filter has merge as a strong option for removing noise, shaping spectrum, and minimizing inter-symbol interference in communication architecture. These filters have become popular because their precise reproducibility allows design engineers to achieve performance levels that are difficult to obtain with analog filters .FIR and IIR filters are the two common filter forms.

The creation and analysis of representative data can be a complex task. Most of the filter algorithms require multiplication and addition in real-time. The unit carrying out this function is called MAC (multiply accumulate). Depends on how good the MAC is, the better MAC the better performance can be obtained.

Adaptive Filter

An adaptive filter is a filter that adjusts its transfer function according to an optimizing algorithm. Because of the complexity of the optimizing algorithms, most adaptive filters are digital filters that perform digital signal processing and adapt their performance based on the input signal used [1].

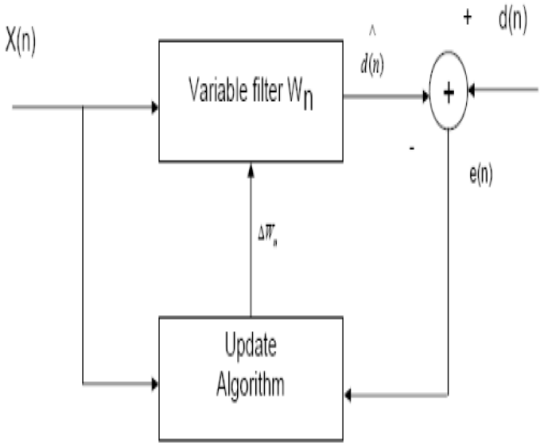


Fig 1-Block diagram of an Adaptive filter

Median filter

In, signal processing it is often desirable to be able to perform some kind of noise reduction on an image or signal. The median filter is a nonlinear digital filtering technique, often used to remove noise. Such noise reduction is a typical pre-processing step to improve the results of later processing (for example, edge detection

on an image). Median filtering is very widely used in digital image processing because, under certain conditions, it preserves edges while removing noise [9].

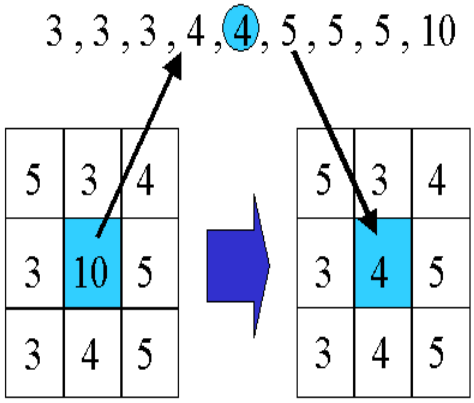


Fig 2-design of median filter

FIR filter

The Lth-order LTI FIR filter is graphically interpreted in Fig.It can be seen to consist of a collection of a "tapped delay line," adders, and multipliers. One of the operands presented to each multiplier is an FIR coefficient, often referred to as a "tap weight" for obvious reasons. Historically, the FIR filter is also known by the name "transversal filter," suggesting its "tapped delay line" structure [7].

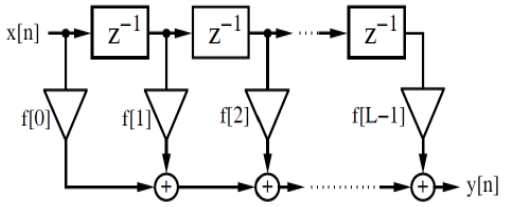


Fig 3- Design of FIR filter

Digital filters include infinite impulse response (IIR) digital filter and finite impulse response (FIR) digital filter. As the FIR system have a lot of good features, such as only zeros, the system stability, operation speed quickly, linear phase characteristics and design flexibility, so that FIR has been widely used in the digital audio, image processing, data transmission, biomedical and other areas. FIR filter has a variety of ways to achieve, with the processing of modem electronic technology, taking use of field programmable gate array FPGA for digital signal processing technology has made rapid development, FPGA with high integration, high speed and reliability advantages, FIR filter implementation using FPGA is becoming a trend.

FIR Filter Using shift register

One of the most fundamental elements for a DSP system is an FIR Filter Impulse Response – A set of FIR coefficients, which represent all possible frequencies.

Tap - A coefficient/delay pair. The number of FIR taps is an indication of the amount of memory required to implement the filter. DUE to the intensive use of FIR filters in video and communication systems, high performance in speed, area and power consumption is demanded. Basically, digital filters are used to modify the characteristic of signals in time and frequency domain and have been recognized as primary digital signal processing operations. They are typically implemented as multiply and accumulate (MAC) algorithms with the use of special DSP devices Fig. 1 shows how MAC is implemented with N multiplications and (N-1) additions per sample to compute the result.

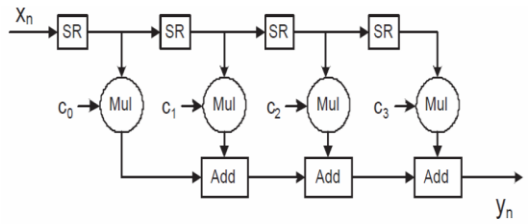


Fig 4-FIR Filter Using shift register

FIR Filter Using Distributed Arithmetic

Distributed Arithmetic (DA) is a different approach for implementing digital filters. The basic idea is to replace all multiplications and additions by a table and a shifter accumulator. DA relies on the fact that the filter coefficients are known, so multiplying c[n]x[n] becomes a multiplication with a constant Distributed Arithmetic (DA) can be used to compute sum of products. Many DSP algorithms like convolution and correlation are formulated in a sum of products (SOP) fashion.

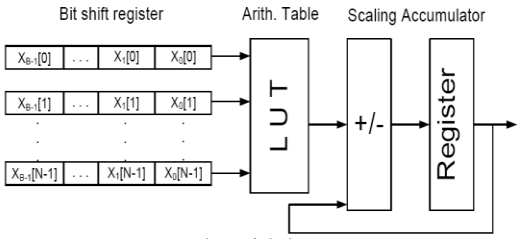


Fig 5-DA Block Diagram

Description of Flow Chart Diagram

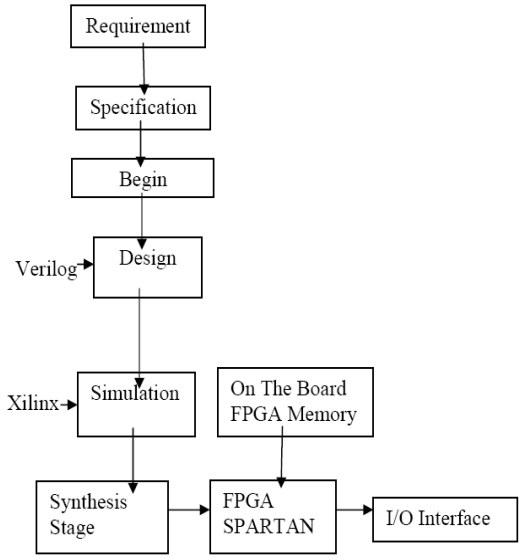


Fig 6-Flow Chart Diagram

II. RESULTS

For FIR filter using shift register approach. The direct fir filter can be implemented by using sequential process uses of adders and multipliers. The output of each tap of the tapped delay line is multiplied with the appropriately weighted binary value and the results are added.

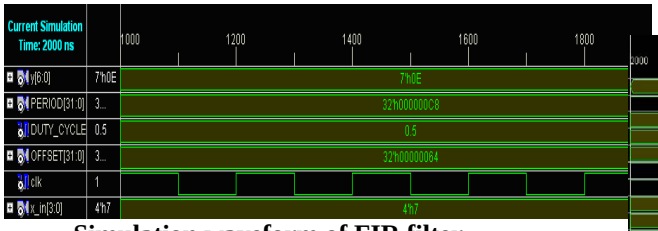
By gathering the requirements related to filters, MAC Units, Booth algorithm architecture, we would specify them accordingly the object so that we can begin the designing process for the Adaptive filter to making FIR, IIR & Median filters. Then after, synthesis stage is capable of producing a wide range of resultant outputs. And finally we can check the inputs of synthesize with the corresponding outputs of the FPGA SPARTAN.

Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	8	1,920	1%
Number of 4 input LUTs	13	1,920	1%
Logic Distribution			
Number of occupied Slices	12	960	1%
Number of Slices containing only related logic	12	12	100%
Number of Slices containing unrelated logic	0	12	0%
Total Number of 4 input LUTs	14	1,920	1%
Number used as logic	13		
Number used as Shift registers	1		
Number of bonded IOBs	7	66	10%
IOB Flip Flops	6		
Number of GCLKs	1	24	4%

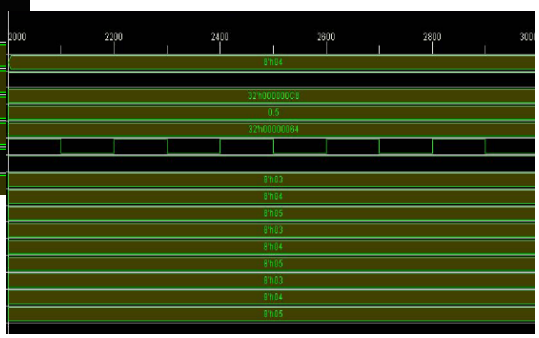
Table1: Design summary when we design FIR filter using shift register

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	8	1,536	1%	
Number of 4 input LUTs	37	1,536	2%	
Logic Distribution				
Number of occupied Slices	24	768	3%	
Number of Slices containing only related logic	24	24	100%	
Number of Slices containing unrelated logic	0	24	0%	
Total Number of 4 input LUTs	37	1,536	2%	
Number of bonded IOBs	12	63	19%	
IOB Flip Flops	11			
Number of GCLKs	1	8	12%	
Total equivalent gate count for design	406			
Additional JTAG gate count for IOBs	576			

Table2: Design summary when we design fir filter using distributed arithmetic



Simulation waveform of FIR filter



Simulation waveform of median filter

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	304	1,920	15%	
Number of 4 input LUTs	392	1,920	20%	
Logic Distribution				
Number of occupied Slices	245	960	25%	
Number of Slices containing only related logic	245	245	100%	
Number of Slices containing unrelated logic	0	245	0%	
Total Number of 4 input LUTs	433	1,920	22%	
Number used as logic	392			
Number used as Shift registers	41			
Number of bonded IOBs	66	66	125%	OVERMAPPED
IOB Flip Flops	33			
Number of GCLKs	1	24	4%	
Total equivalent gate count for design	8,131			
Additional JTAG gate count for IOBs	3,984			

Table3: Design summary when we design median filter

III. CONCLUSION

We have proposed and designed a Verilog implementation of FPGA based digital filters which produces appreciable results because of various benefits like low power consumption, higher efficiency, faster etc. in this approach we presented low area FIR filter for reduce area we using of phase architecture. It demonstrated that our approach is most effective for implementations with the constraints of low area. The proposed FIR filters have been synthesized and implemented using Xilinx ISE spartan3.

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