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Effective Estimation of Peak-Power for a Testable Digital Circuit

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Abstract*— Peak power corresponds to the highest value of instantaneous power measured during testing. The peak power generally determines the thermal and electrical limits of the circuit and the system packaging requirements. High peak power in only one clock cycle can be an issue if it results in a significant ground bounce or an IR-drop phenomenon that causes a memory element to lose its state and the test procedure to unnecessarily fail. Tools for evaluating the worst-case peak-power consumption of sequential circuits are strongly required by designers of low-power circuits. Previously proposed methods search for the initial state and the couple of vectors with maximum consumption, without exploiting the information on the reachable state set during the power estimation process. This paper shows that this can lead to significant underestimation of the maximum power consumption, and proposes an algorithm for overcoming this drawback.

Index Terms—**Peak Power, Instantaneous Power, IR-Drop, Worst-Case peak power, Test Vectors**

I.INTRODUCTION

With the advance in semiconductor manufacturing technology, a ***very-largescale-integrated*** (VLSI) device can now contain tens to hundreds of millions of transistors. Because this trend is predicted to continue at least into the 2010s perMoore's law [11], severe challenges are imposed on tools and methodologiesused to design and test complex VLSI circuits. Addressing these design andtest challenges in an efficient way is becoming increasingly difficult [8].Testing currently ranks among the most important issues in the developmentprocess of an integrated circuit. The issues that center on testing are manufacturingyield, product quality, and test cost. To address these test issues, ***designfor-testability*** (DFT) techniques[1],[2],[3]Power dissipation has become a major design objective in many application areas,such as wireless communications and high-performance computing, thus leading to the production of numerous low-power designs. In the last years, design for low-power consumption has become a widespread design paradigm, due to the continuous increase in chip density. Excessive power dissipation can cause performance degradation, untimed errors, or device destruction due to overheating. Large instantaneous power dissipation may cause local hot spots that have a negative impact on circuit reliability. With increasing demands for high reliability in modern VLSI designs, accurate estimation of the maximum power dissipation and maximum instantaneous current during the design process is becoming essential. We propose an algorithm to find a 3-tuple (S, V1, V2) which maximizes the power consumption, being S the initial state from which the couple of vectors (V1, V2) is applied.

A technique based on Genetic Algorithms is proposed, where logic simulation is extensively used to evaluate the fitness function. The technique can deal with large circuits, but is strongly approximated since it initially ignores the reachability of the initial state S during the optimization process.

Here we will analyze the behavior of this algorithm, and experimentally demonstrate that this approach can underestimate the peak-power when the number of reachable states is a small fraction of all the possible states. We will then propose a new approach, based on a Genetic Algorithm, which overcomes this drawback by exploiting the knowledge about the reachable state set during the optimization process.

Two implementations of the proposed algorithm (named ALPS, for *Analyzer of Low-Power Systems*) will be described. The former is based on symbolic computation techniques, which allow computing the complete set of reachable states for sequential circuits of small and medium size; a symbolic approach to Hamming distance computation between couples of states will also be presented. The latter implementation targets large sequential circuits, thus overcoming the limitation stemming from the symbolic computation techniques; it is based on logic simulation to approximately compute the reachable state set, and on the use of hash tables to represent sets of states and compute the Hamming distance between couples of states.

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II. DESCRIPTION

The logic built-in self-test (BIST) is a DFT technique in which a portion of thecircuit under test (CUT) is used to test itself. Because it can provide self-test ability,logic BIST is crucial in many applications, in particular, for safety-critical andmission-critical applications. One major objective of logic BIST is to obtain highfault coverage; however, a major issue is that power consumption during BIST canexceed the power rating of the chip or package. Increased average power can heatthe chip, and increased peak power can produce noise-related failures [1].Peak powercorresponds to the highest value of instantaneous power measuredduring testing. The peak power generally determines the thermal andelectrical limits of the circuit and the system packaging requirements. If thepeak power exceeds a certain limit, the circuit may be subjected to structural degradation and, in some cases, be destroyed. From a theoretical point ofview, the peak power is defined from the values of instantaneous power measuredin short time intervals (*i.e.*, the system clock period). In practice, thetime window for the definition of peak power is related to the thermal capacityof the chip, and restricting this window within just one clock period is notrealistic enough. For example, if the circuit has peak power consumptionduring only one cycle but it has power consumption within the limit of thermalcapacity of the chip for all other cycles, the circuit may not be damagedbecause the energy consumed may not be enough to elevate chip temperatureover the thermal capacity limit of the chip (unless the peak power consumptionis far higher than normal power consumption). To damage the circuit,high power consumption should last for several successive clock cycles to consumeenough energy to elevate chip temperature over the limit [10]. Onthe other hand, high peak power in only one clock cycle can be an issue if itresults in a significant ground bounce or an IR-drop phenomenon that causesa memory element to lose its state and the test procedure to unnecessarilyfail.

Heat dissipation in CMOS circuits can be effectively estimated by means of the switching activity. Dynamic power consumption coming from the application of the *i*-th vector is proportional to the circuit *weighted switching activity* (wsa^i), defined as:

$$wsa^i = \sum_g C_g NT_g^i \qquad (1)$$

Where C_g is the physical capacitance associated to gate g and NT_g^i is the number of times the output of gate g toggles due to the application of the *i*-th vector.

Different methods have been proposed to evaluate wsa^i. In this paper we exploit a unit-delay model and measure the weighted switching activity by means of a unit-delay logic simulator.

The problem addressed in this paper is to find the 3- tuple (S, V_1, V_2) which maximizes the weighted switching activity. To measure the wsa^i, we assume that the circuit is initially in state S with V_1 on the primary inputs. We force V_2 to the primary inputs and apply a clock pulse. The wsa^i for the 3-tuple (S, V_1, V_2) is measured as the activity produced in the circuit by the application of V_2 synchronously with the clock pulse.

III. TRADITIONAL ALGORITHM

The symbolic version of the Traditional algorithm is composed of two consecutive steps: reachable states set computation, and peak-power computation. The first step analyzes the circuit and, by exploiting symbolic calculation techniques, computes all the reachable states, $\chi_{reached}$. We resort to *characteristic functions* and symbolic traversal techniques to represent sets of states and to compute the reachable state set. The secondstep computes the 3-tuple (S, V_1, V_2), where S $\in \chi_{reached}$, which maximizes the power consumption.

Computation of reachable states

To efficiently compute the set of reachable states for a sequential circuit, we resort to BDDs and symbolic traversal techniques. The circuit is modeled as anFSM (Finite State Machine), and is represented by the Boolean functions δ and λ. Function δ computes the next state y from the current state s and the current input x: $y = \delta(s, x)$. Function λ computes the output z starting from the same information: $z = \lambda(s, x)$. The techniques resort to the adoption of *characteristic functions* to represent sets states $\chi_s(s)$, and the state transition relation $TR(s, y)$. The transition relation is defined as follows:

$$TR(s,y) = \left(\prod_j \delta_j(s,x) \,\overline{\oplus}\, y_j \right) \qquad (2)$$

TR is true for every couple (s,y) for which an input $x$exists that satisfies $y=\delta(s, x)$, i.e., whenever y is a valid successor to s under some input value x.

Peak-power estimation

A Genetic Algorithm has been adopted to find a 3-tuple (S, V_1, V_2) that maximizes the peak-power consumption.

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The *individual* is encoded as a single binary string containing the state S and the input vector couple. The *cross-over* operator is a uniform one: bits from the 2 parents are selected with probability 0.5 at each string position when generating the two offspring. A *mutation*operator randomly changes a limited number of bits inthe binary string. The *fitness function* is the attainedwsa^i, measured resorting to a unit-delay logic simulator.

The most critical part of the algorithm is the analysis of the initial state, S, generated in the offspring. After the cross-over and the mutation operators have been applied, the algorithm searches for S in the previously computed states set $\chi_{reached}$. If $S \notin \chi_{reached}$, it is substituted with the reachable one having minimum Hamming distance from S. The algorithm is based on the assumption that a given input sequence produces almost the same power consumption when applied starting from two different states having a low Hamming distance. In sub-section 3.3, a symbolic procedure is described to compute a state having minimum Hamming distance from a given state.

After the initial state has been analyzed, the fitness function is evaluated. It should be noted that our algorithm can be easily extended to make it able to solve similar problems: as an example, the fitness function can be modified to consider the maximum n-cycle power [3] to find the best (n+2)-tuple (S_1, V_1, …, V_{n+1}) that maximizes the average power of a contiguous sequence of *n* clock cycles.

Minimization of the Hamming distance

The problem addressed in this sub-section is how to compute one of the states within $\chi_{reached}$ having minimum Hamming distance from S. For each state $S^* \in \chi_{reached}$ we first compute the Hamming distance between S and S^*. We then select one of the states having minimum distance.

We express the reachable states in term of a new variable $W=S \oplus S^*$ where the *i*-th bit of W is 1 if and only if S and S^* differ in the *i*-th bit position:

$$\chi_{reached}(W) = \chi_{reached}(S^*) | S^* = W \oplus S \qquad (3)$$

The number of 1s in W is therefore the Hamming distance between S^* and S.

The computation of the reachable state S^* having minimum Hamming distance from S is performed by:

1. Finding the set of all the satisfying assignment inthe BDD of $\chi_{reached}(W)$ having the minimum number of 1s, $\chi_H(W)$;
2. Randomly selecting one state in the previously computed set $\chi_H(W)$.

IV. Approximated ALPS

The ALPS algorithm described in the previous Section is suitable for small and medium size circuits, only, being based on BDDs for representing the characteristic functions required by the symbolic traversal techniques and Equations 2 and 3. The reachable state set can indeed be symbolically computed for circuits having few flip-flops, only.

The hash table can be exploited to identify the set of states having low Hamming distance from a given state S. Let *n* be the number of bits over which a state S is expressed, and *k* a set of randomly selected bits, where $n < k$. The binary number expressed over the select *k* bits is the hash function *h*(S). The reachable states are stored in subsets; each state in the subset L has Hamming distance at most equal to *n*-*k* for every state in L.

Given a state S produced by the genetic operators, *h*(S) is first computed: it identifies a subset of states L. For each state in L, the Hamming distance from S is then computed. The state $S^* \in$ L for which the distance is minimum is selected. During the computation of the state S^* a sub-set of the reachable states is considered, only. The result we obtain is thus an approximation of the minimum Hamming distance, but this approach allows to address large circuits.

V. Experimental Results

A prototypical version of tool named ALPS has been written, which implements the above introduced procedures. To compare ALPS with a state-of-the art tool, we have re-implemented the algorithm proposed in [4], adopting a unit-delay model to evaluate the switching activity of the gates. Experimental results are almost the same presented in [4], we can therefore perform a fair comparison on a larger set of circuits than that published in [4].

Power is expressed in terms of Peak Switching Frequency per node (*PSF*), which is the normalized wsa^i(i.e., the weighted number of transitions on all nodes over the total number of capacitive nodes) as defined in [3]. PSF_U reports the maximum PSF without considering the reachability of the initial state; while PSF_H reports the PSF considering only reachable states. ΔPP represents the relative PSF loss between the PSF_U and the PSF_H. *FF* reports the number of flip-flops in the circuit. *H* reports the minimum Hamming distance from the ideal state and the closest reachable state; while *Dim* reports the number of reachable states having

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Hamming distance equal to *H*. *R*reports the ratio between *H* and *FF*, i.e., the percentage of the initial state bits approximated to obtain a reachable state. Finally, the CPU time requirements are reported. By observing Δ*PP* and *R*, one can observe that several circuits exist where the peakpower strongly depends on the reachability of the initial state (reported in boldface). Where a significantloss in PSF is found, the corresponding value of R is generally high: there is a strong difference between the ideal initial state and the selected reachable one.

ΔPPs measures the improvement in Peak Switching Frequency obtained by the symbolic version of ALPS over the [4] algorithm. that ALPS is able to effectively improve the peak-power computation for circuits where the power consumption of a sequence is tightly coupled with the initial state. For such circuits ALPS is directly able to find the optimal state within the reachable states set, thus improving the peak-power consumption. On the other hand, circuits exist where the impact of the initial state on the peak-power consumptionis poor. For such circuits an improvement less than1.5% has been observed, while high values of R havebeen computed. From the point of view of CPU timerequirements, the symbolic implementation of ALPS is38% slower than [4] on the average, mainly due to thetime overhead required to symbolically compute theHamming distance.

Table I. Experimental Results showing

FF	PSFu	PSFh	H	ΔPP(%) [Re Implementation]	ΔPP(%) [Symbolic ALPS]	ΔPP(%) [Approximated ALPS]
8	0.9	0.9	0	0	0	0
14	1.007	0.833	3	-17.28	0	0
15	1.556	0.307	1	-80.27	400	400
19	2.794	1.144	6	-59.06	63.99	21.50
21	0.961	0.79	6	-17.79	5.32	0

The peak power estimated by ALPS is 45% higher on the average than that computed by [4], showing the importance of the reachability analysis we exploit within the optimization process. By exploiting a hash table to manipulate large sets of states, our approach is also faster than [4] (17.5% on the average). We expected this result, since the symbolic implementation computesthe minimum Hamming distance state, while the approximated one gives a minimal solution, only. On the other hand, the difference between the two implementations has a small magnitude; we can thus conclude that the hash function-based method we exploit allows computing the minimum Hamming distance state with a good approximation.

VI. Conclusion

We described an algorithm to compute the peakpower consumption of a sequential circuit. The algorithm exploits the knowledge about the reachable states set: it is thus able to produce better results than those provided by previously proposed methods, especially when dealing with circuits where the peak-power is tightly coupled with the reachability of the initial state.

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