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Multistage Implementation of 64x Interpolator

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***Abstract*— This paper presents the design consideration and simulation of interpolator suitable for delta sigma D/A converter. The proposed structure uses the half band filer & Sinc filter using the MATLAB Tool. Experimental result shows that proposed interpolator achieves the design specification, and also has good noise rejection capabilities. The interpolator accepts the input at 44.1 kHz for applications like CD, SACD & DVD audio. The interpolation filter can be applied to the delta sigma DAC and is fully functional. To reduce the hardware requirement in terms of multiplier we used the Sinc filter whose structure is cascaded integration & combination (Multiplier free). The filter coefficients were generated with the help of MATLAB & the MATLAB generated (HDL Coder) VHDL code is synthesized in Xilinx ISE 13.1 for the Xilinx VERTEX6 FPGA chip. The achieved frequency of operation for the multistage 64x interpolator is 26.112 MHz. The experiment includes the simulation of the proposed interpolator for the sinusoidal signal with random noise.**

Keywords: Interpolator; OSR; Halfband filter; Comb Filter

I. INTRODUCTION

The number of portable digital audio products is increasing day by day. The main parameter while the designing of any portable device is their cost and power consumption.

Interpolator is an integral part of digital audio DAC which is used to relax the stringent design requirements for analog filters [5], [7]. A general block diagram for a sigma-delta D/A converter is depicted in Figure 1. It consists of four functionally different parts. In the first phase, the sampling rate of the input discrete-time signal is increased using an interpolator filter. In the second phase, the noise shaper converts an n-bit input data stream into a 1-bit data stream. This data stream is converted in the third phase into an analog signal using a 1-bit D/A converter. The role of the noise sharper is to keep the noise generated by the quantization as low as possible in the baseband by shaping and moving this noise out of the baseband. The final phase consists of removing the out-of-band noise using an analog low pass filter.

Fig. 1 shows the system architecture of the audio DAC. It consists of three blocks, namely, the interpolator, the sigma-delta modulator and the 1-bit DAC.

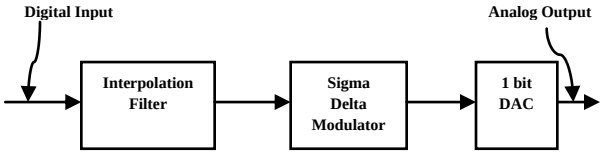

Fig. 1 Block Diagram of Sigma Delta DAC

The audio DAC accepts PCM input data at sampling rates of 44.1 kHz. The interpolation ratio of the interpolator can be configured to 64x. For 44.1 kHz input signals, the interpolator gives the output data rate of 2.8224 MHz by setting the interpolation ratio as 64x.

In this paper, we present an interpolator structure with its implementation in MATLAB. The Synthesis part is done for XILINX SPARTAN 6 chip.

II. INTERPOLATOR ARCHITECTURE

The function of interpolation filter in sigma delta DAC is to raise the sampling frequency to oversampling rate (OSR * fs) and to suppress the spectral replicas centered at fs, 2fs, …, (OSR-1) fs. Due to the high sampling rate, the pass-band and transition band are extremely narrow compared to the Nyquist bandwidth of the output signal, which means a single stage FIR filter to achieve 64x OSR has to be of exceedingly high order, so a multi-stage structure is preferred to reduce the computation complexity [1], [2].

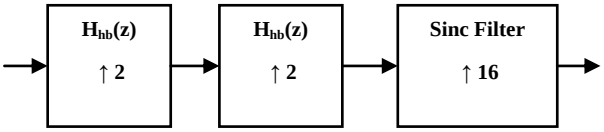

Fig. 2 Interpolation Filter

The architecture of the 64x interpolation filter is shown in Fig. 2. It is a multi-stage filter. The first two half-band filters increase the sampling rate of the signal by four times. The last stage is comb filter to provide 16 times sampling rate for input signals leading to overall interpolation ratio as 64x.

A. *Half Band Filter*

In the design of sharp cutoff FIR filters, a multistage design based on half-band filters is very efficient. The efficiency of half band filters derives from the fact that about 50 % of the filter coefficients are zero thus cutting down the implementation cost.

Half band filters can be used for signal oversampling by 2 (x2). The resulting signal contains the original samples and the interpolated point between the original samples is the original samples filtered by the non-zero coefficients.

Half-cost filters have also been used in multirate filter bank applications, either directly or indirectly [4].

Let H(z) denote the transfer function of a (linear-phase, FIR) half-band filter of order N-1.

$$H(z) = \sum_{n=0}^{N-1} h(n)z^{-n}, \; h(n)real \qquad (1)$$

B. *Sinc Filter*

A comb filter provides the remaining factor of 16 in the sampling rate. The advantage of comb filter is their simple structure, which does not require any multiplier or coefficient storage, as compared with traditional FIR filters [3]. Cascaded integrator-comb (CIC) digital filters are computationally efficient implementations of narrowband lowpass filters and are often embedded in hardware implementations of decimation and interpolation in modern communications systems.

The comb filter has the transfer function of

$$T_{sinc}(z) = \frac{1}{M^N}\left(\frac{1-z^{-RM}}{1-z^{-1}}\right)^N, \qquad (2)$$

Where R = decimation or interpolation ratio, M= number of samples per stage, N = number of sections in filter.
The CIC filter's difference equation is:

$$y(n) = x(n) - x(n-D) + y(n-1), \qquad (3)$$

Usually a SincL+1 filter are used to filter out the quantization noise of an Lth order modulator.

A CIC interpolator would be N cascaded comb stages running at fs/R, followed by a zero-stuffer, followed by N cascaded integrator stages running at fs, where N represents the No. of sections (No. of Integrator Sections = No. of Integrator Section) [6].

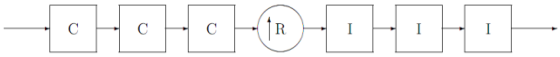

Fig. 4 Comb Filter Structure having three sections

III. IMPLEMENTATION

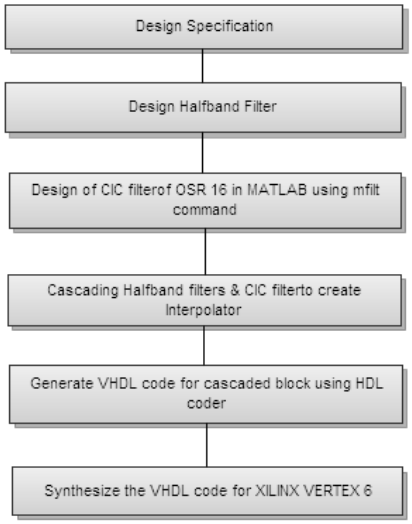

Fig. 5 Flow Diagram of our work

In the implementation of the multistage interpolation we chose the specification as per Table I. Designing of the first & second stage Half Band filter is done with the mfilt of MATLAB. Similarly the CIC filter of the OSR 16 is achieved with the mfilt command. The three filters is then cascaded and the relevant VHDL code is generated with the generateHDL (HDL Coder) in MATLAB.

The VHDL code is exported to the Xilinx ISE 13.1 where the code is synthesized to get the hardware requirement for the proposed 64x interpolator.

Table I Specification of Sub Blocks

Stage	Type of filter	OSR	Sampling Frequency / kHz	Stop-band attenuation / dB
1	Half-band	2	44.1	80
2	Half-band	2	88.2	80
3	Comb/ Sinc	16	2,822.4	65

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IV. EXPERIMENTAL RESULTS

The complete design has been prepared with MATLAB & Xilinx ISE 13.1. The Coefficients generation of each filter is generated using the MATLAB and then the VHDL code is generated with the help of HDL Coder. Generated VHDL code is synthesized for the XILINX VERTEX6.

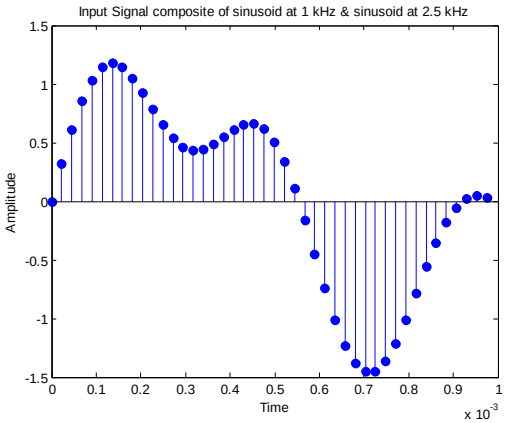

Fig. 6 Input Signal to the 64x Interpolator

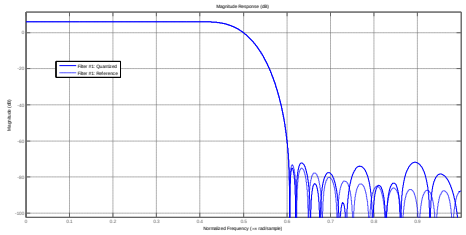

Fig. 7 Magnitude Response of Halfband Filter

Fig. 7 & 8 shows the Magnitude & impulse response for the first & second stage of the Interpolator. Fig. 9 depicts the Signals at input of the HBF1 & at the output of HBF1 & HB2.

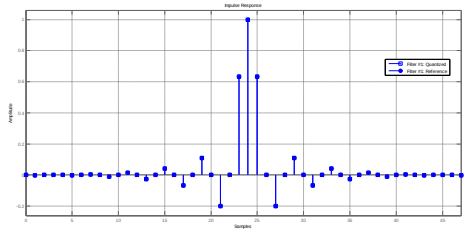

Fig. 8 Impulse Response of Halfband Filter

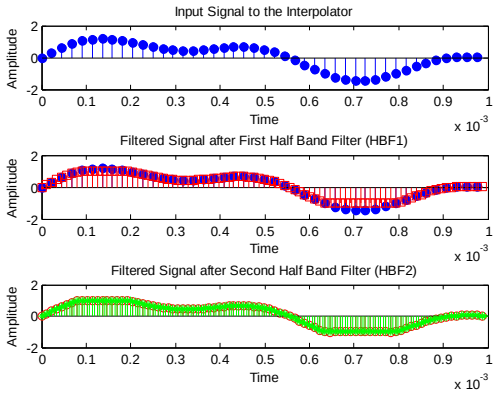

Fig. 9 Signals at the input of Interpolator & at the output of HB1 & HB2

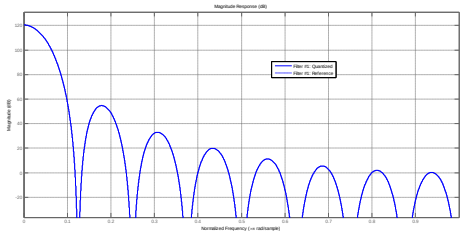

Fig. 10 Magnitude Response of Comb/Sinc Filter

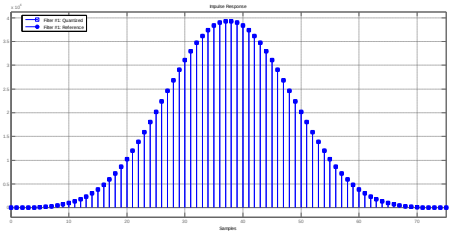

Fig. 11 Impulse Response of Comb/Sinc Filter

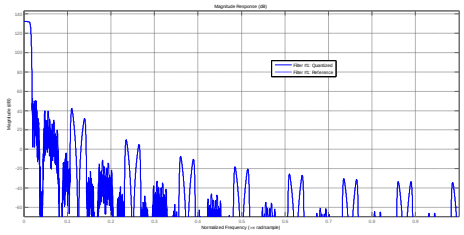

Fig. 12 Magnitude Response of Interpolator

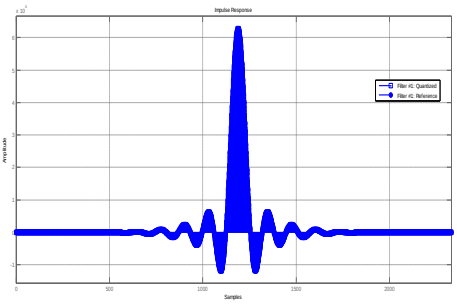

Fig. 13 Impulse Response of Comb/Sinc Filter

Fig. 10, 11, 12, & 13 shows the Magnitude & impulse response for the third stage- Sinc filter & Interpolator respectively. Fig. 14 depicts the Signals at output of the interpolator.

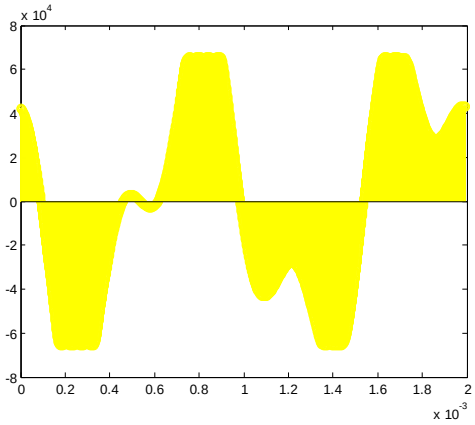

Fig. 14 Output Signal of 64x Interpolator

Table II shows the implementation details of our design. Each row of the table shows the hardware cost of each stage of Interpolator as per specification mentioned in Table 1. The last row shows the hardware implementation cost of the interpolator. The maximum achievable frequency of operation for the interpolator is 26.112 MHz.

Table 2 Synthesis Result of Blocks for XILINX VERTEX6

Design	Slices	Max. Clock (MHz)	No. of Multiplier	No. of Adder	No. of Registers
Stage I	405	332.969	24	24	25
Stage II	405	332.969	24	24	25
Stage III	256	170.841	-	11	13
Cascade Design	1033	26.112	48	61	63

V. CONCLUSION & FUTURE SCOPE

Multistage method to construct the interpolation filter of Sigma Delta Audio DAC is presented in this paper. Cascade halfband filter and a sinc filter comprise the interpolation filter. Multirate filtering & HDL Coder feature of the MATLAB is utilized to achieve the design.

The optimization can be performed so that the overall interpolator contains no general multipliers. This is achieved by using hardware efficient FIR filters in a tapped cascaded interconnection of identical sub-filters, which requires no multipliers. Further area optimization is achieved by the multiplier less CSD encoding.

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