

Device Parameter Optimization of Scaled Si-Ge Heterojunction Bipolar Transistor

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Abstract:

The immense demand for communication systems worldwide has created an enormous market for semiconductor devices (SiGe HBTs) in varied applications. Nowadays SiGe HBTs are surpassing even the fastest III-V production devices in the GHz speed orbit. Scaling has been the prime source of supremacy behind the successful technology innovations. The design and optimization of un-scaled and scaled SiGe HBTs for the key performance parameter which affect the speed parameter in GHz frequency range has been explored extensively using appropriate scaling technique, which have recently emerged as a tough competitor for RF and mixed-signal applications. In this paper, the dynamic performance of un-scaled and scaled SiGe HBTs in terms of the cut off frequency, the maximum frequency of oscillation is investigated in a faultless approach with the help of Y-parameter by ATLAS software from SILVACO. Both vertical and lateral scaling affect the device parameters. The impact of lateral scaling on cut off frequency is not as prominent as vertical scaling, but a certain level of lateral scaling needs to go along with vertical scaling. Since maximum frequency of oscillation is absolutely associated to cut off frequency, the remuneration of vertical scaling on cut off frequency also apply to maximum frequency of oscillation, although the impact level is comparatively lower. However, maximum frequency of oscillation depends on R_B and C_{CB} , too, which are truly degraded by vertical scaling. As a result, the impact of vertical scaling on maximum frequency of oscillation is thorny, depending on structural details of the given device. On the other hand, lateral scaling, which has only some degree of influence on cut off frequency, plays a major role on maximum frequency of oscillation. The simulated results of un-scaled and scaled SiGe HBT are compared and contrasted.

Keywords: SiGe HBT, performance parameter (intrinsic & extrinsic), Speed Parameter, scaling, ATLAS.

1. INTRODUCTION

While the initiative of using SiGe alloys to band gap-engineer Si devices dates to the 1960's, the amalgamation of defect-free SiGe films proved somewhat difficult, and device-quality SiGe films were not productively produced until the early to mid 1980's. While Si and Ge can be united to produce a chemically stable alloy (Si Ge or simply "SiGe"), their lattice constants fluctuate by roughly 4% and, thus, SiGe alloys full-fledged on Si substrates are compressively strained. (This is referred to as "pseudo orphic" growth of SiGe on Si, with the SiGe film adopting the primary Si lattice constant.) These

SiGe stressed layers are subject to an essential stability criterion [1], [2], limiting their thickness for a given Ge concentration. For a manufacturable SiGe technology, it is obviously key that the SiGe films linger stable after processing.

Silicon-Germanium (SiGe) technology is the inspiration behind the explosion in low-cost, lightweight, personal communications devices like digital wireless handsets, as well as other amusement and information technologies akin to digital set-top boxes, Direct Broadcast Satellite (DBS), automobile collision avoidance systems, and personal digital assistants. SiGe extends the verve of wireless phone batteries, and allows smaller and more sturdy communication devices. Products combining the capabilities of cellular phones, global positioning, and Internet access in single package, are being designed via SiGe technology. These multifunction, low-cost, mobile client devices skilled of communicating over voice and data networks signify a key element of the future of computing.

The spirit of SiGe technology is a SiGe heterojunction bipolar transistor (HBT), which offers compensation over both conventional silicon bipolar and silicon CMOS for accomplishment of communications circuits. SiGe HBTs combines the speed and performance of many III-V technologies with Si-processing compatibility acquiescent a high-performance device that is readily commercially available. Since the first SiGe HBT revelation over 20 years ago, SiGe HBT technology has shown an almost exponential intensification both in terms of performance and number of commercial facilities [4][5].

In addition to maintaining high performance and high reliability, it is clear that achieving low power, small size, light weight, and low cost are indispensable requirements for next generation communication front-ends and radar modules. Freshly, an alternative integrated circuit (IC) technology based on silicon-germanium (SiGe) alloys has shown the potential to accomplish these requirements [4].

The concert of semiconductor devices tends to enliven as the device dimensions minimize. This simple approach of scaling has been the key to the radiant success of semiconductor industry over the past half-century. It has worked for virtually all types of transistors, including the Si-based bipolar transistor. Scaling has sprint into evident hard limits multiple times in the track of bipolar technology progression, which have been prolifically overcome with help

from material and structural innovations, such as the self-aligned base, poly emitter, epitaxial base and most freshly the SiGe base.

As the impediment of the integrated circuits increases, scalable device models are becoming essential for the most favorable circuit design. Scaling of bipolar transistor models is significantly more involving due to current flow in both vertical and lateral directions. Moreover, the geometry scaling strategy of bipolar devices generally depend on the layout pattern, device cross-section and fabrication succession details. As a result, the geometry scalable bipolar transistor models and the consequent parameter drawing out procedures are not generally available and usually exist as a familial proprietary. The physical quantities in a bipolar transistor that scales with geometry can be estranged into three categories: (1) current and charge, (2) ratio of current and charge and (3) parasitic and thermal resistance.

Even though there is a number of work done on the optimization of the performance parameter of the SiGe HBT but the results are not unswerving. We searched the consequence of scaled device as well as Ge concentration on the performance parameter which affect the speed parameter of Si_{1-x}Ge_x HBT here. In this paper, current gain, cut off frequency, maximum oscillation frequency, C_{BC} , C_i and transit time delay of scaled and un-scaled device are calculated for different Ge concentrations. In this paper, Raje's scaling technique has been taken with scaling factor as 1.25. It is shown that the scaling, both vertical and lateral, has mainly beneficial effects on speed performances of SiGe HBT. Following this motivation, in the next two section, we address model of Si_{1-x}Ge_x HBT and SiGe operation with device scaling. In the next section, an extraction technique of performance parameter has been given for un-scaled and scaled SiGe HBT which is based on small signal analysis. In Section-V & VI, we discuss the results and concluded with common projections and observations based on ATLAS.

2. MODEL

The energy-band diagram of resultant device is the dominant mean to depict a range of consequences of introducing Ge into the base region of SiGe HBT by comparing it to Si. The graded base induces a drift field across the unbiased base that is allied in a direction (from collector to emitter). This causes an hastening of induced minority electrons across the base. Accordingly, this large drift field component is a domino effect for electron transport phenomenon. Hence, by efficiently speeding up the diffusive transport of the minority carriers a decrement in the base transit time occurs. Though the band offsets in SiGe HBTs are generally small in comparison to the band offsets of III-V technology standards, the large electric fields are translated by the Ge grading over the petite distance of neutral base and this electric field is plenty to speed up the electrons to near saturation velocity. In comparison to SiGe HBT, the base transit time characteristically limits the frequency response of the Si BJT. Therefore it could be conventional that the frequency response

should be enhanced appreciably by the Ge- induced drift field [6]. The cross-section of the un-scaled and scaled SiGe HBT base is shown in Fig. 3&4. The band-gap of SiGe HBT is given by [7],

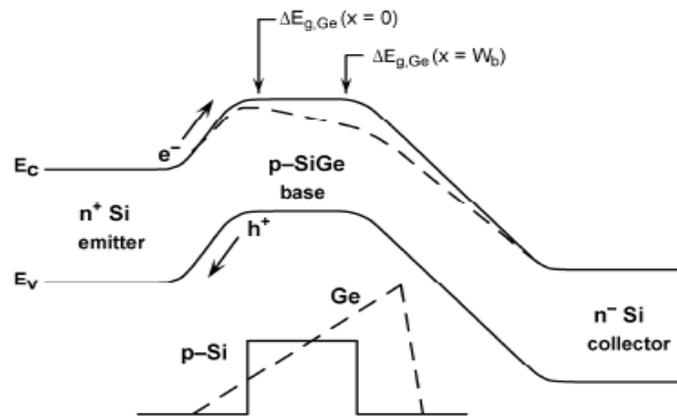


Figure 1: Energy band diagram for a Si BJT and graded-base SiGe HBT, both biased in forward active mode at low injection

$$E_g^{SiGe} = E_g^{Si} \cdot (1 - x) + E_g^{Ge} \cdot x + C_g \cdot (1 - x) \cdot x \quad (1)$$

Where x is Ge conc. and $C_g = -0.4$ eV is a bowing parameter. Ge is compositionally graded from the emitter-base (EB) junction with inferior concentration to the collector-base (CB) junction with superior concentration and it is shown as dashed line in Figure (1). Due to this collision, the SiGe HBT consists of a finite band offset at the EB junction and a larger band offset at the CB junction. Band gap grading is effortlessly used for position confidence of the band offset with respect to Si. An electric field is produced by such position confidence in the Ge induced band offset in the neutral base region. This effect aids the transportation of minority carriers (electrons) from emitter to collector, which in turn advance the frequency response [8-11].

Thus we can say actually from Figure (1) that the Ge-induced diminution in base band gap takes place at the EB edge of the quasi-neutral base $\Delta E_{g,Ge}(x=0)$ along with the CB edge of the quasi-neutral base $\Delta E_{g,Ge}(x=W_b)$. Thus the graded band gap is agreed by equation as [12],

$$\Delta E_{g,Ge}(graded) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0) \quad (2)$$

Such Ge grading crossways the neutral base induces a built-in-quasi drift field ξ .

3. SiGe HBT OPERATIONS WITH DEVICE SCALING

The indispensable assistance of a SiGe HBT over Si BJT is that we can diminish the band gap E_g by introducing Ge in the base. The result is an exponential augment of the effective intrinsic carrier concentration, and hence the minority carrier

density. By scheming the Ge profile, an accelerating electric field can be established in the base, which favors minority electron transport for an *npn* transistor, and thus helps condense base transit time τ_B . Another benefit of using a SiGe base is that the low base sheet resistance, high β and low τ_B can be achieved all together.

Excellent speed performance is privileged for most practical semiconductor applications of today. The competence of information processing muscularly depends on the speed of devices that compose the system. The speed of a device can be represented by a variety of measures and equivalent speed parameters. Although some alternatives have been proposed [13], the most widely used speed parameters for transistors are the cutoff frequency and the maximum oscillation frequency, which are defined as the frequency point where the current gain and the power gain become unity, correspondingly.

3.1. CUT-OFF FREQUENCY AND DEVICE SCALING

The effect of device scaling on the cutoff frequency f_T , a figure-of-merit for device speed, can be more effectively viewed through a parameter τ_f and τ_t , defined as the reciprocal of multiplied by a factor of 2π , which can be expressed in terms of bipolar device parameters as

$$\frac{1}{2\pi f_T} = \tau_f + \tau_t \quad (3)$$

$$\tau_f = \tau_E + \tau_B + \tau_{CSCR} \quad (4)$$

$$\tau_t = \frac{V_{th}}{J_C} (C_{te} + C_{tc}) \quad (5)$$

τ_f is the forward transit time attributable to electron diffusion for an *npn* SiGe HBT. τ_t is the depletion capacitance charging time related with EB junction (C_{te}) and CB junction (C_{tc}). V_{th} is the thermal voltage and J_C is the collector current density. τ_f includes the emitter transit time τ_E , the base transit time τ_B , and the collector space charge region transit time τ_{CSCR} . For an *npn* bipolar transistor with steady base doping and Ge profile, τ_E and τ_B can be uttered as

$$\tau_B = \frac{w_B^2}{2D_n} \quad (6)$$

$$\tau_E = \frac{1}{\beta} \frac{w_E^2}{2D_p} \quad (7)$$

w_E and w_B are the quasi-neutral emitter and base width, β is the current gain, D_p is the minority hole diffusivity in the emitter and D_n is the minority electron diffusivity in the base.

τ_E can be abridged appreciably through increasing β . Depending on the emitter and base design, a sufficient β is mandatory to make τ_E negligible. A main characteristic of scaled SiGe HBT is the significantly reduced base width w_B . Once the emitter and base are scaled down, τ_{CSCR} becomes the restricted access for speed. Generally, τ_{CSCR} can be expressed as [14]

$$\tau_{CSCR} = \frac{1}{X_{CSCR}} \int_0^{X_{CSCR}} \frac{X_{CSCR} - x}{v(x)} dx. \quad (8)$$

where X_{CSCR} is the space charge region width, and $v(x)$ is the local carrier velocity. For balance transport, where the electron velocity saturates at V_{sat} in the collector SCR, the right side of (8) equals " $X_{CSCR}/2V_{sat}$ ". Using first-order approximations [15]

$$X_{CSCR} \propto \frac{1}{\sqrt{N_C}} \quad (9)$$

Therefore, to fully assistance from base scaling, the collector doping N_C needs to be increased to reduce τ_{CSCR} .

3.2. $J_{C, peak}$ AND DEVICE SCALING

Observing (3) - (5), at the same J_C , f_T can be enhanced through the τ_f and junction capacitance diminution. Fascinatingly, however, when N_C is increased to reduce collector transit time τ_{CSCR} , the Kirk effect is belated simultaneously. The reason is that the current density $J_{C, peak}$ at which base push out occurs [16] is comparative to N_C . As a result, not only does the peak f_T value increase, but also it happens at higher J_C . f_T rolls off when $J_C > J_{C, peak}$. $J_{C, peak}$ has augmented from 3 mA/ μm^2 to 23 mA/ μm^2 as technology increases from 50 GHz to 375 GHz [17].

The concerns with the higher J_C are the probable device degradations associated with electro migration and self-heating, both of which are addressed by scattering current and power over an gradually more narrow emitter. Copper-interconnection and appropriate emitter layout can get rid of the electro migration. For device self-heating, it has been confirmed in [17] that when the emitter width is scaled down proportionally to the increased $J_{C, peak}$, and the device perimeter is maintained constant, self-heating can be controlled to guarantee steadfast device operation.

3.3. MAXIMUM OSCILLATION FREQUENCY AND DEVICE SCALING

f_{max} of bipolar transistors can be approximated as follows:

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{CB} R_B}} \quad (10)$$

seeing as f_{max} is positively interconnected to f_T , as indicated by the expression (10), the compensation of vertical scaling on f_T also apply to f_{max} , although the impact level is comparatively lower. However, f_{max} depends on R_B and C_{CB} too which are actually degraded by vertical scaling as temporarily described earlier. As a result, the impact of vertical scaling on f_{max} is convoluted and may turn out either positive or negative, depending on structural details of the given device. On the other hand, lateral scaling, which has only imperfect persuade on f_T , plays a major role on f_{max} . Base current is abounding laterally to the intrinsic device, nothing like emitter or collector currents, and lateral scaling reduces the resistive current path for base, ensuing in R_B reduction. B-C junction area decreases with lateral scaling, too, leading to a diminution in C_{CB} . As f_{max} has a direct involvement with R_B and C_{CB} , it greatly benefits from lateral scaling [18].

As discussed above, through vertical scaling, f_T can be enhanced dramatically. R_B and C_{CB} can be reduced by lateral scaling and device structure innovations as well. Moreover, the shallow-trench-isolation (STI) and selective-implanted-collector (SIC) structures can also help diminish extrinsic CB capacitance. Recall (10) that a reduction of C_{CB} is desired to improve f_{max} . Overall, f_{max} has been augmented from 65 GHz to 300 GHz for modern SiGe HBTs.

4. HF MODELING AND PERFORMANCE FACTORS

In this section we develop a novel and straightforward extraction method for discussing the transistor RF performance along with procedures to find out the parameters of un-scaled and scaled SiGe HBT by means of small-signal Π topology alike circuits of this HBT. The algorithm is helpful for extracting both intrinsic plus extrinsic (parasitic) elements. If we determine previously the extrinsic elements of the HBT then predictable methods derived from simple bias measurements work very sound. Throughout different procedures for example DC, cut-off measurements, or optimization can be used for this approach. Since the typical DC and cut-off techniques present poor concert for Silicon Germanium HBT devices that's why it is frequently very hard to accurately determine the values of parasitic elements of the HBT. An pioneering technique has been developed to avoid this problem and in this technique only scattering (S)-parameters and then y-parameters at different biases are measured. For fitting the measured S parameters appropriately, linear models by way of a Π topology have been practiced. We have deserted emitter resistance, the collector resistance, along with the output resistance due to Early effect for simplicity [19].

This method is an extension to the HBT devices of Shirakawa's and Ooi's work on metal semiconductor field-effect transistors (MESFETs) and high-electron mobility transistors (HEMTs), respectively. The major difference between the MESFET/ HEMT loom and this new scheme is that the MESFET/HEMT method uses nine different biases to assess the frequency behavior of the intrinsic elements to properly compute the set of parasitic elements. On the other hand, the method takes the fitting of some significant figures of merit of the device into explanation. A noteworthy reduction of the comparative error function between modeled and measured S-parameters is obtained by using the previously mentioned premises [20].

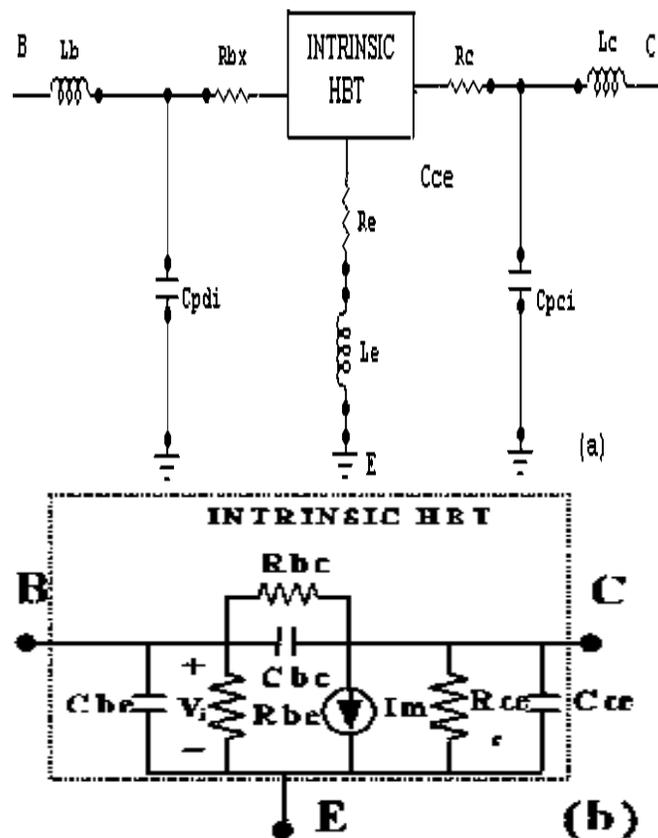


Figure 2: A small-signal π equivalent circuit of an HBT device (a) contains intrinsic and extrinsic circuit elements. The intrinsic elements (b) can be determined from the admittance parameters of the device at a number of different bias points.

The projected circuit topology of the small-signal model shows a dashed box that contains the intrinsic part of the device (Fig. 2b). The expected values of the pad parasitic capacitances C_{pbi} and C_{pci} do not surpass hundredths of femto Farads (fF) for a number of different devices weathered. The remaining extrinsic parameters (L_b , L_c , L_e , R_b , R_c , and R_e) in

Fig. 2a can be determined easily by an optimization process at the same bias point where intrinsic elements were computed.

After a conservative de-embedding process to take the effect of scrounging elements into account, it is possible to attain the intrinsic elements from the admittance parameters (y-parameters) of the un-scaled and scaled HBT device for each bias point. The relationship between the current source, I_m , and the intrinsic transconductance, g_m , is provided by the following equation:

$$I_m = G_m \times V_i \quad (11)$$

Where,

$$G_m = g_m \cdot e^{-j\omega\tau} \quad (12)$$

Taking the real and imaginary parts of these admittance parameters (y-parameters) it is comparatively easy to attain a set of equations with unknowns. This process supports the computation of C_{be} , R_m , R_{be} , R_{bc} , C_{bc} , g_m , τ , R_{ce} , C_i and C_{ce} , values by using the following expressions [20]:

$$C_{bc} = \frac{-Im[Y_{12}]}{\omega_i} \quad (13)$$

$$C_{be} = \frac{Im[Y_{11}] + Im[Y_{12}]}{\omega_i} \quad (14)$$

$$C_{ce} = \frac{Im[Y_{22}] + Im[Y_{12}]}{\omega_i} \quad (15)$$

$$R_{be} = \frac{-1}{Re[Y_{12}]} \quad (16)$$

$$R_{ce} = \frac{1}{Re[Y_{12}] + Re[Y_{22}]} \quad (17)$$

$$R_{be} = \frac{1}{Re[Y_{12}] + Re[Y_{11}]} \quad (18)$$

$$g_m = 2\pi C_i f_T = \frac{qkT}{I_c} \quad (19)$$

$$C_i = C_{be} + C_{bc} = C_{te} + g_m \tau \quad (20)$$

$$\tau = \frac{1}{2\pi f_T} \quad (21)$$

where: R_e and I_m = the real and imaginary parts, respectively, ω = the angular frequency, and $i = 1 \dots N$ = the number of frequency sampling points.

5. RESULTS & DISCUSSION

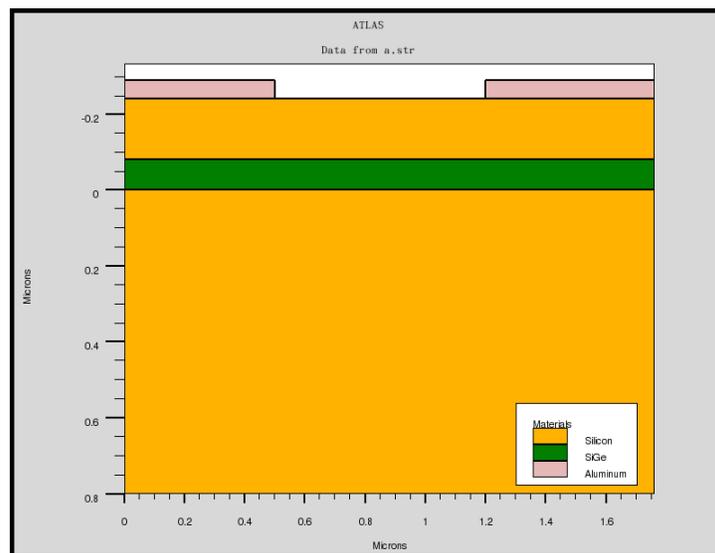


Figure 3: scaled device

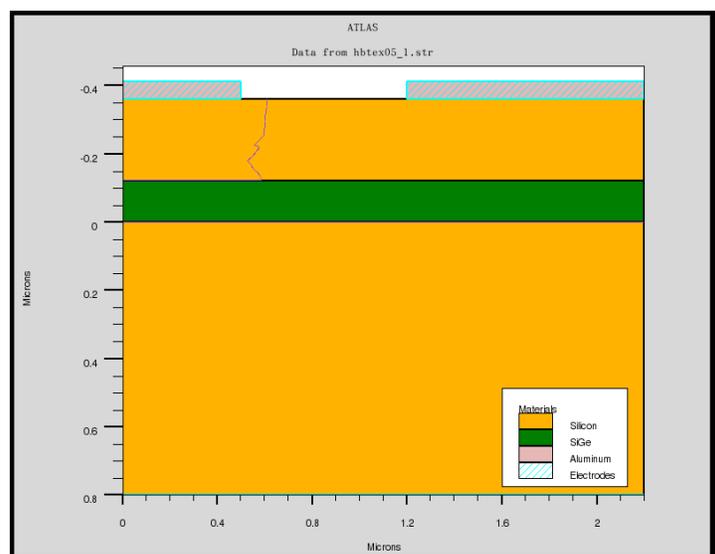


Figure 4: un-scaled device

Based on the above model the values of f_{max}/f_T and a variety of intrinsic as well as extrinsic elements are calculated for n-p-n un-scaled and scaled SiGe HBT at different Ge concentrations. For this purpose ATLAS from SILVACO is used. The un-scaled HBT considered in this paper has the base

width of $0.1\mu\text{m}$. the appropriate scaling techniques used to scale the device was taken as Raje's scaling techniques. Average Ge concentration in this base region considered in our calculations is varied from 5%-30% as higher to this are not supported by present epitaxial technologies and beyond it the enhancement associated with Ge seizes may be due to lattice constant mismatch. ATLAS simulation of un-scaled and scaled SiGe HBT is performed to prove precision. The structure of the un-scaled and scaled SiGe HBT is given in figure 3&4. Figure 4 shows the structure of un-scaled device which has length of emitter, base and collector of $2.2\mu\text{m}$. The un-scaled device has emitter width of $0.2\mu\text{m}$, collector width of $0.8\mu\text{m}$ and base width of $0.1\mu\text{m}$. Figure 3 shows the scaled SiGe HBT. Scaling is done using appropriate scaling technique such as Raje's scaling technique taking scaling factor as 1.25. Scaled SiGe HBT has emitter, base and collector length of $1.76\mu\text{m}$. Scaled device has emitter width of $0.16\mu\text{m}$, base width of $0.08\mu\text{m}$ and collector width of $0.8\mu\text{m}$.

The Gummel plot of un-scaled and scaled SiGe HBT for this model at 1V forward bias is plotted in Figure 5. The plot in Figure 5 shows the variation of collector current and base current w.r.t. bias voltage of un-scaled and scaled SiGe HBT.

Parameter	Base Model	Raje's Scaled Model
Cutt-off freq: f_T (GHz)	21.34	28.5
Max. Osl. Freq: F_{max} (GHz)	25.10	34.214
Transit Time Delay: τ (ps)	9.05	5.34
Transconductance: gm	0.0274	0.0255
B-C Junc. Capacitance: (f/ μ)	9.012e-12	5.69e-12
$C_i = C_{be} + C_{bc}$: (f/ μ)	5.45e-13	1.33e-13
Current Density: J ($\text{A}/\mu\text{m}$)	2.013e-19	1.019e-16

This plot indicates to the significant dc consequence of adding Ge into the base of SiGe HBT, however, lies with the collector current density [6]. Bodily, the barrier to electron injection at the EB junction is reduced by introducing Ge into the base,

yielding more charge transfer from emitter-to collector for a given applied EB bias. Observe from Figure (1) that in this linearly graded base design, the emitter region of the SiGe HBT and Si BJT comparison are fundamentally identical, implying that the resultant base current density of the two transistors will be roughly the same.

Table 1:

The net result is that the introduction of Ge increases the current gain of the transistor ($\beta = \text{collector current density} / \text{base current density}$). From a more device-physics slanting viewpoint, the Ge-induced band offset exponentially decreases the intrinsic carrier density in the base which, in turn, decreases the base Gummel number and, hence, increases collector current density. Important in this context is the Ge-induced improvement in β over a comparably constructed Si BJT [6]. On scaling the device with appropriate scaling technique like Raje's scaling technique, the current gain of the transistor increases as shown in the fig. 5.

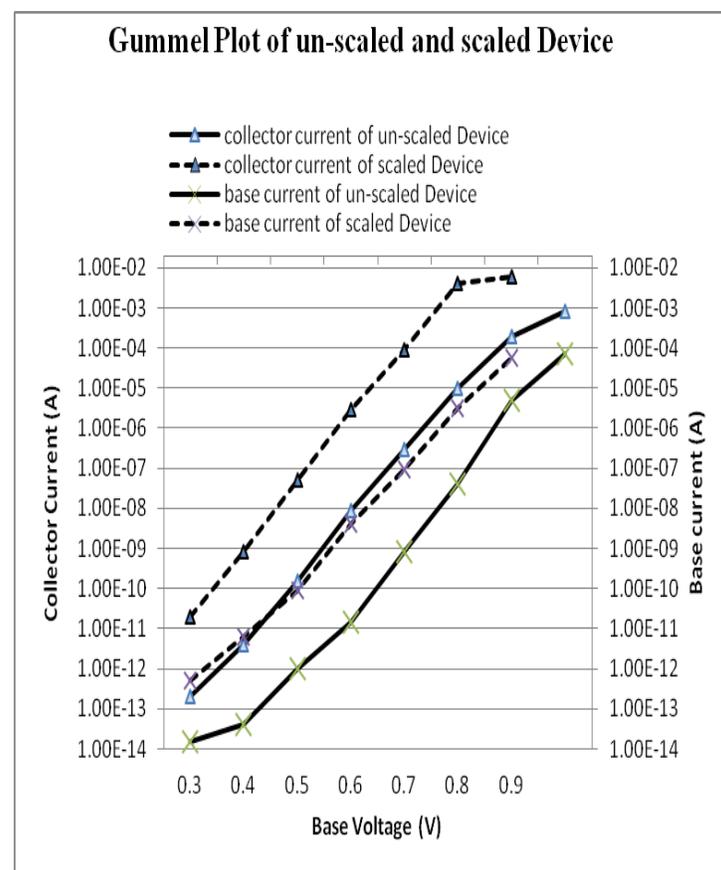


Figure 5: Gummel Plot of un-scaled and scaled Device

Different parameter of un-scaled and scaled SiGe Heterojunction Bipolar Transistor at 20% Ge concentration is

given in table 1. In the table base model's parameter is the parameter of un-scaled SiGe HBT and Raje's scaled model's parameter is the parameter of scaled SiGe HBT. Cut-off frequency of base model is 21.34 GHz and of the scaled model is 28.5 GHz at 20% Ge concentration. Maximum oscillation frequency of un-scaled and scaled SiGe HBT is 25.10 GHz and 34.214 GHz respectively. The transit time delay of un-scaled and scaled model is 9.05 ps and 5.34 ps. From the table it is clear that current density of un-scaled SiGe HBT and scaled SiGe HBT is 2.013×10^{-19} A/ μm and 1.019×10^{-16} A/ μm respectively. Transconductance of base model and scaled model is 0.0274 and 0.0255.

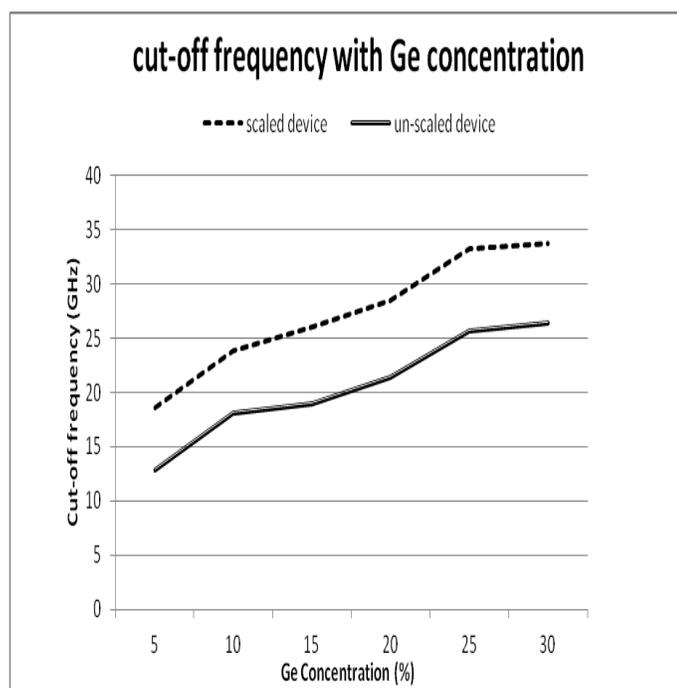


Figure 6: variation of cut-off frequency with Ge concentration

Fig.6 shows the variation of cut-off frequency of un-scaled and scaled SiGe HBT with respect to Ge concentration present in the base of SiGe HBT. Average Ge concentration in this base region considered in our calculations is varied from 5%-30% as higher to this are not supported by present epitaxial technologies and beyond it the enhancement associated with Ge seizes may be due to lattice constant mismatch. ATLAS simulation of un-scaled and scaled SiGe HBT is performed to prove precision. At 5% Ge concentration the cut-off frequency of un-scaled SiGe HBT and scaled SiGe HBT is 12.89 GHz and 18.547 GHz respectively. On increasing the Ge

concentration from 5% to 30% in the base region, the cut-off frequency of un-scaled and scaled device increases to 26.43 GHz and 33.689 GHz respectively.

Fig.7 shows the variation of maximum oscillation frequency of un-scaled SiGe HBT and scaled SiGe HBT with respect to Ge concentration present in the base of SiGe HBT. At 5% Ge concentration present in the base of device, the maximum oscillation frequency of un-scaled SiGe HBT and scaled SiGe HBT is 10.974 GHz and 22.102 GHz respectively. At 25% Ge concentration, the maximum oscillation frequency of un-scaled and scaled SiGe HBT increases to 30.343 GHz and 38.241 GHz respectively.

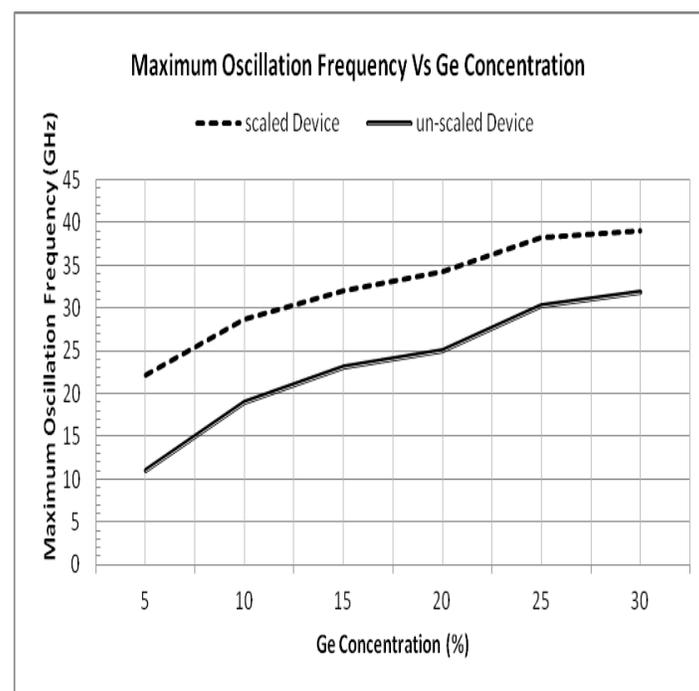


Figure 7: variation of maximum oscillation frequency with Ge concentration

Table 2 shows the variation of current density and transit time delay of scaled SiGe Heterojunction Bipolar Transistor with respect to Ge concentration present in the base region. In my calculation Ge concentration range is from 5% to 30% in the base region because beyond this are not supported by present epitaxial technologies and beyond it the enhancement associated with Ge seizes may be due to lattice constant mismatch. At 5% Ge concentration current density of scaled model is 1.034×10^{-21} A/ μm , at 20% Ge concentration current density is 1.019×10^{-16} A/ μm and at 30% Ge concentration the current density of scaled model increases to 2.80×10^{-14} A/ μm . It is clear

from the above numerical data that on increasing the presence of Ge concentration in the base of SiGe HBT, current density

increases. At 5% transit time delay of scaled SiGe HBT is 9.51

Table 2:

Current Density: J (A/ μm)	1.034e-21	8.298e-19	7.012e-17	1.019e-16	3.91e-15	2.801e-14
Transit Time Delay: τ (ps)	9.51	8.23	7.49	5.34	4.95	4.01
Ge Concentration: (%)	5	10	15	20	25	30

ps, at 15% Ge concentration present in the base of SiGe HBT transit time delay is 7.49 ps and at 30% Ge concentration in the base transit time delay is 4.01 ps. From the above extracted numerical data, it is clear that on increasing the Ge concentration in the base region, the transit time delay of scaled SiGe HBT decrease and device becomes faster than un-scaled SiGe HBT.

fig. 8 shows the variation of transit time delay of un-scaled and scaled SiGe HBT w.r.t. Ge concentration. At 5% Ge concentration the value of transit time delay of un-scaled and scaled SiGe HBT is 9.51 ps and 13.56 ps respectively. At 30% Ge concentration the value of transit time delay of un-scaled and scaled SiGe HBT is 4.01 ps and 6.39 ps respectively. It is clear from the fig.8 that on increasing the Ge concentration from 5% to 30%, the transit time delay of un-scaled and scaled SiGe HBT decreases.

summation of B-E junction capacitance and B-C junction capacitance which is shown in equation (20). Right vertical axis of Fig. 9 shows the value of B-C junction capacitance of un-scaled and scaled SiGe HBT is $1.05\text{e-}11$ f/ μ and $3.03\text{e-}11$ f/ μ respectively at 5% Ge concentration in the base of SiGe HBT. On increasing the Ge concentration from 5% to 30% in the base of SiGe HBT, B-C junction capacitance of un-scaled and scaled SiGe HBT decreases to $3.91\text{e-}12$ f/ μ and $6.91\text{e-}12$ f/ μ respectively. So, it is clear from this axis that on increasing the Ge concentration, B-C junction capacitance decreases. Left vertical axis of Fig.9 shows the value of C_i of un-scaled and scaled SiGe HBT at 5% Ge concentration, which is $5.82\text{e-}13$ f/ μ and $8.50\text{e-}13$ f/ μ respectively. At 20% Ge concentration in the base of SiGe HBT, the value of C_i of un-scaled and scaled SiGe HBT reaches to $1.33\text{e-}13$ f/ μ and $5.45\text{e-}13$ f/ μ respectively. From this axis also, it is clear that on increasing the Ge concentration, the value of C_i decreases of un-scaled and scaled SiGe HBT.

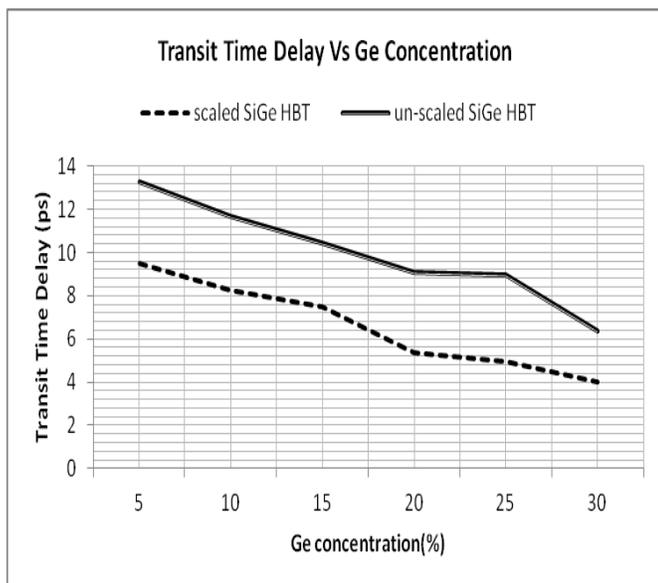


Figure 8: Transit Time Delay Vs Ge Concentration

Fig.9 shows the variation of B-C junction capacitance and C_i ($C_{BE}+C_{BC}$) of un-scaled and scaled SiGe HBT with respect to Ge concentration in the base of SiGe HBT. C_i is the

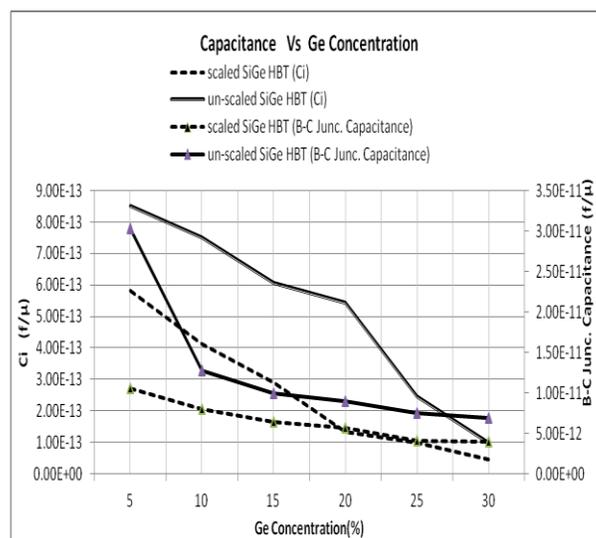


Figure 9: Capacitance Vs Ge Concentration

6. CONCLUSION

In this paper, a detailed investigation has been made to study the impact of scaling and Ge content in the SiGe-HBT base on the performance parameter of SiGe HBT. An electric field is produced by position in the impartial base region. This effect aids the transportation of minority carriers (electrons) from emitter to collector, which in turn perk up the frequency response. High frequency devices are characterized by extracted y parameters. Y-parameters are measured by means of a small signal measurement. In this paper, we develop a novel and straightforward extraction method for discussing the respectively with comparison to un-scaled device. Based on simulation results of un-scaled SiGe HBT and scaled SiGe HBT, it is confirmed that applied scaling technique is effective to obtain better performances of the scaled device. This model is also used to realize microwave power amplification at GHz frequency range using these devices has been verified to be viable.

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impacts of appropriate scaling technique on the transistor's RF performance along with procedures to find out the parameters of SiGe HBT by means of small signal Π topology equivalent circuits of this HBT. Further the parameters like C_{BC} , C_i and transit time delay which strongly affect the f_{max}/f_T are calculated of un-scaled and scaled SiGe HBT. The scaling of the device and base-region optimizations can effectively improve the power-gain values of Si_{1-x}Ge_x HBTs in a wide frequency (GHz) range. It can be concluded that on scaling the device with appropriate scaling technique, the transit time delay decreases. From (3) and (10) it is clear that on the

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