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LOW POWER MULTIPLEXER BASED FULL ADDER USING PASS TRANSISTOR LOGIC

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***Abstract*- The efficiency of a system mainly depends on the performance of the internal components present in the system. So, the internal components must be designed in such a way that they should consume less power with increase in speed. Full adder is one of the major components in the design of many sophisticated hardware circuits. Perhaps it is one of the essential components in the design of a wide variety of processors also. In this paper several multiplexer based pass transistor full adder topologies are presented. The main idea is to introduce the design of high performance and low power mutiplexer based pass transistor full adders which acquires less area and transistor count. . The high performance multiplexer based pass transistor low power full adder circuit is designed and the simulation has been carried out on Mentor Graphics tool. The result shows that the proposed full adder is an efficient full adder cell with least MOS transistor count that reduces the high power consumption and increases the speed.**

***Keywords*- Full adder, nmos, pmos, cmos, speed, low power, delay, less transistor count, efficiency.**

I. INTRODUCTION

Full adder is one of the basic building blocks of many of the digital VLSI circuits. Several refinements has been made regarding its structure since its invention. The main aim of those modifications is to reduce the number of transistors to be used to perform the required logic, reduce the power consumption and increase the speed of operation. One of the major advantages in reducing the number of transistors is to put more devices on a single silicon chip there by reducing the total area.

In the recent days the use of portable electronic devices like cellular devices, laptops has been increased exponentially. The main requirement of these portable devices is reduced power consumption, small area and high speed of operation. To achieve these requirements research efforts in the field of low power VLSI (very large scale integration) have increased many folds. As the number of transistors on a single silicon chip increases, the package density also increases. With the rise in chip density, power consumption of VLSI systems is also increasing and this further, adds to reliability and packaging problems. Packaging and cooling cost of VLSI systems also goes up with high power dissipation. So, the low power consumption along with minimum delay and area requirements is one of important design consideration for IC designers in designing portable electronic devices and many sophisticated hardware circuits.

A basic full adder has three inputs and two outputs which are sum and carry. The logic circuit of this full adder can be implemented with the help of XOR gate, AND gates and OR gates. The logic for sum requires XOR gate while the logic for carry requires requires AND and OR gates. The basic equations for sum and carry of a full adder are

$$Sum = A \oplus B \oplus C \quad (1)$$

$$Carry = AB + BC + CA \quad (2)$$

The basic logic diagram for full adder using its boolean equations with basic gates can be represented as shown below

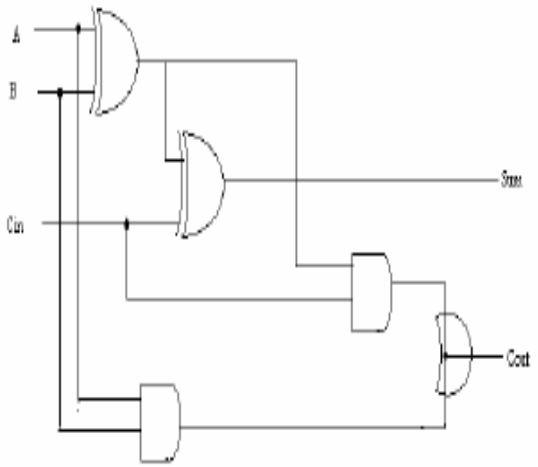

Figure 1: Logic circuit for Full Adder

The XOR gate is the basic building block of the full adder circuit. The performance of the full adder can be improved by enhancing the performance of the XOR gate. Several refinements has been made in its structure in terms of transistors to increase the performance of full adder. The early designs of XOR gates were based on eight transistors or six transistors that are conventionally used in most designs. The main intention of reducing this transistor count is to reduce the size of XOR gate so that large number of devices can be configured on a single silicon chip thereby reducing the area and delay. In the proposed work the XOR gate is implemented with only two transistors which reduces the area to a large extent and power consumption.

The full adder design in static CMOS using complementary pull up pMOS network and pull down

nMOS network is the most conventional one, and it also has the advantage of very low power consumption. However, it has as many as 28transistors and thus requires considerable chip area for its implementation. The full adder design based on CMOS transmission gates and CMOS inverters uses 20 transistors. The circuit can operate with full output voltage swing. The designs were further reduced to only 16 transistors while maintaining the full output voltage swing operation. To further minimize the number of transistors, pass transistor logic can be used in lieu of transmission gate. Pass transistor logic based XOR and XNOR circuits were used and as a result the full adder design consists of only 14transistors. In this design, an inverter is employed to generate the function AΘB. The full adder can be implemented in terms of two half adders. It can be represented in the form of modules as

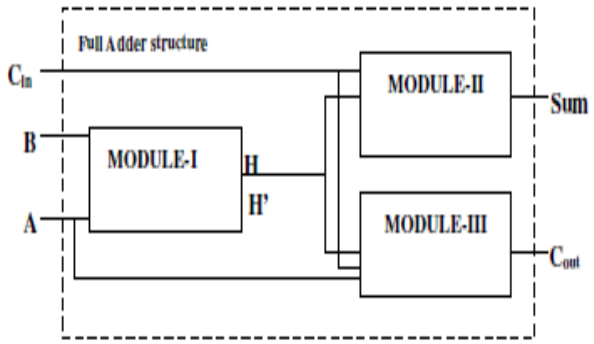

Figure 2: Structure of full adder

In the present paper the full adder is implemented by using multipler based pass transistor logic that uses MOSFETs as its basic components. Further the logic is implemented seperately for pmos transistors, nmos transistors and cmos transistors.

II. IMPLEMENTATION OF PASS TRANSISTOR BASED MULTIPLEXER

Pass transistor logic is used to improve the performance of arithmetic and logic circuits. This logic can be used to reduce the power dissipation in the system and to increase the speed of operation of the processor. By using pass transistor logic the number of transistor count can also be reduced when compared to static CMOS design in realizing th complex systems. When the number of transistor are decreased the area of the chip decreases in parallel.When the number of transistors is reduced, we can decrease the number of layout elements and parasitic capacitances. Several parasitic capacitances are charging and discharging during signal propagation, and some current is consumed. Therefore, PTL design can be used to remove some transistors, and, it may be important to reduce the current consumption. However, some electrical problems must be addressed. There are situations in which the input signal of a PTL gate is passed to the output node, but the output signal sometimes can be degraded. For instance, the 1 input logic value when transmitted through a NMOS transistor cannot charge the output parasitic capacitance to Vdd level. The maximum voltage stored by the output capacitance is Vdd-Vth. Vth is the threshold voltage of theNMOS transistor. The same happens when a PMOS transistor is being considered. In this case the 0 input logic value when transmitted is not totally propagated, and a Vth voltage remains stored in the output capacitance.

In the present paper, the logic for multiplexer is realized using pass transistor logic. The number of transistor count can be decreased by implementing pass transistor logic in the multiplexers. Further, the pass transistor logic is implemented in multiplexer for pmos, nmos and cmos transistors separately.

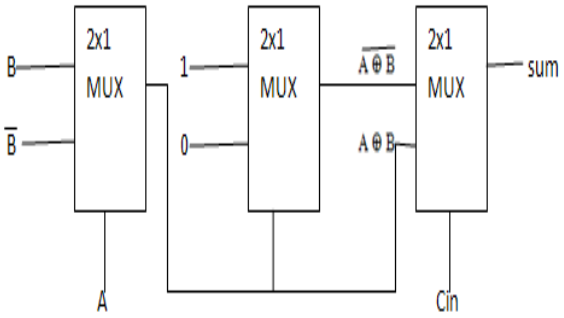

Figure 3: Block diagram of Sum using pass transistor logic based multiplexer.

The figure shows the logic for generating sum in the full adder circuit using multiplexers with pass transistor logic as its basic building logic. The logic is implemented using three 2x1 multiplexers which has two inputs and one output for each multiplexer with a selecet line in its structure. The output is generated depending on the selection line only. B bar can be implemented by basic using inverter circuit. It can be generated either by using NMOS or PMOS transistors.

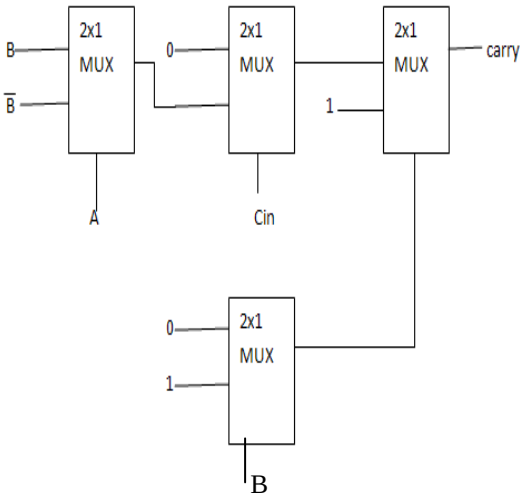

Figure 4: Block diagram of Carry using pass transistor logic based multiplexer.

The figure shows the logic for generating carry in the full adder circuit using multiplexers with pass transistor logic as its basic building logic. The logic is implemented using four 2x1 multiplexers which has two inputs and one

output for each multiplexer with a selecet line in its structure. The output is generated depending on the selection line only. When compared to sum circuit, it requires one extra multiplexer. It can be generated either by using PMOS transistors or NMOs transistors.

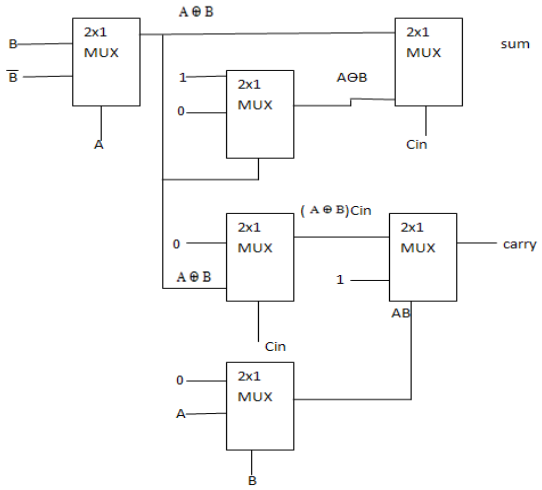

Figure 5: Block diagram of full adder using pass transistor logic based multiplexer.

The figure shows the block diagram for the design of full adder using multiplexers that uses pass transistor logic as its basic building logic. The logic is implemented using six 2x1 multiplexers which has two inputs and one output for each multiplexer with a selecet line in its structure. The output is generated depending on the selection line only. These multiplexers can be designed with the help of pass transistor logic that uses both PMOS and NMOS transistors.

III. PROPOSED PMOS BASED FULL ADDER

In the proposed logic the multiplexer based full adder is implemented using PMOS transistors only. For the design of full adder, the logic for both sum and carry is realized seperately. The PMOS transistor enters into ON state when its gate input is logic 0, and it enters into OFF sate when its gate input is logic 1, i.e., for a PMOS transistor, the output is logic HIGH for a logic 0 input and logic LOW for a logic 1 input.

By using PMOS transistors only, the power dissipation is reduced to a great extent. The power dissipation in carry generation is less than the power dissipation in sum generation. Because of this feature it ca be used in many of the low power applications.

The circuits for sum and carry of full adder are

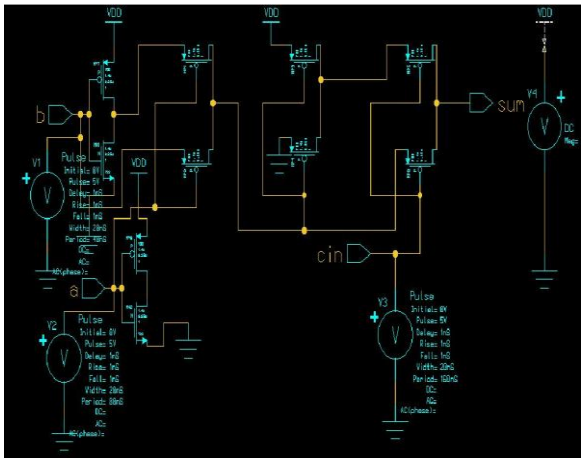

Figure 6: Design of sum using PMOS transistors

The figure shows the circuit for the generation of sum in the full adder circuit using PMOS transistors only. It uses a maximum of ten PMOS transistors in its construction.

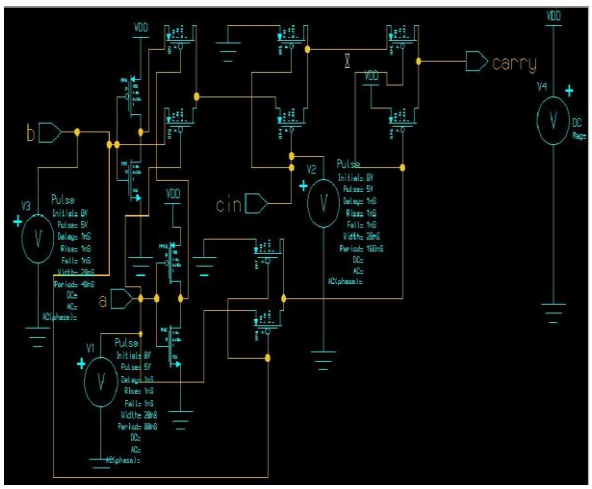

Figure 7: Design of carry using PMOS transistors

The figure shows the circuit for the generation of carry in the full adder circuit using PMOS transistors only. It uses a maximum of twelve PMOS transistors which uses two extra transistors compared to sum circuit.

IV. PROPOSED NMOS BASED FULL ADDER

In the proposed logic the multiplexer based full adder is implemented using NMOS transistors only. For the design of full adder, the logic for both sum and carry is realized seperately. The NMOS transistor enters into ON state when its gate input is logic 1, and it enters into OFF sate when its gate input is logic 0, i.e., for an NMOS transistor, the output is logic HIGH for a logic 1 input and logic LOW for a logic 0 input.

By using PMOS transistors only, the power dissipation is reduced to a great extent. The power dissipation is approximately same for both carry and sum generations. Because of this feature it ca be used in many of the low power and high speed applications.

The circuits for sum and carry of full adder are

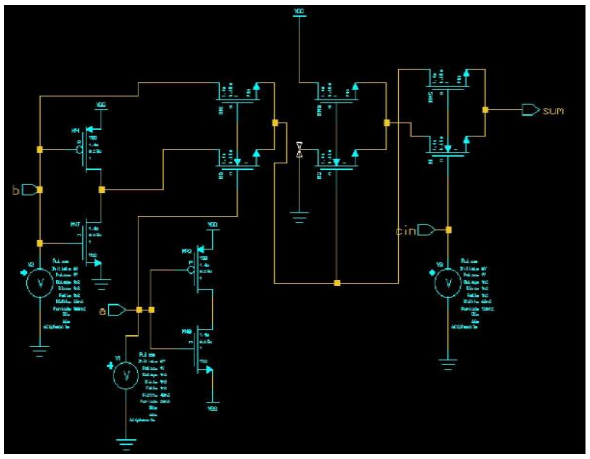

Figure 8: Design of sum using NMOS transistors

The figure shows the circuit for the generation of sum in the full adder circuit using NMOS transistors only. It uses a maximum of ten NMOS transistors in its construction which is similar to PMOS sum circuit.

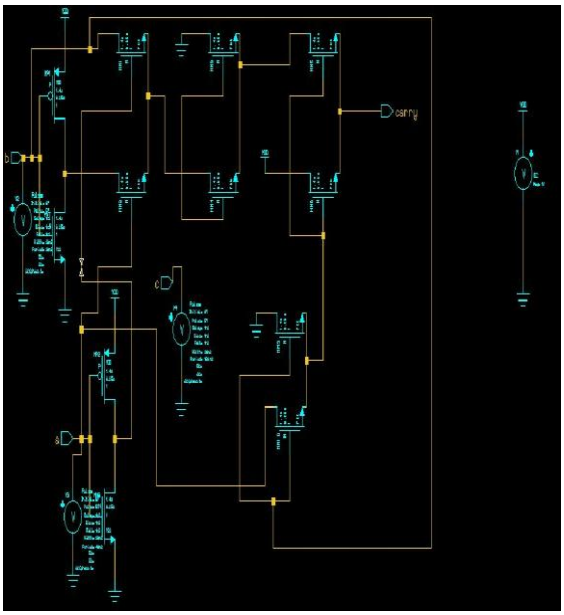

Figure 9: Design of carry using NMOS transistors

The figure shows the circuit for the generation of carry in the full adder circuit using NMOS transistors only. It uses a maximum of twelve NMOS transistors similar to PMOS carry circuit and uses an extra two transistors compared to sum circuit.

V. PROPOSED MIXED CMOS BASED FULL ADDER

Full adder is the most widely used element in many of the arithmetic operations. A basic full adder circuit has three inputs and two outputs and the two outputs are sum and carry. Further full adder is the basic element in many of the low power VLSI devices where low power and less area is the primary requirement. To reduce the area of the overall chip the elements inside the chip are to be designed as small as possible. The size of the individual elements inside the chips can be minimized by modifying their basic logical representation in a meaning full manner so that the desired logic can be obtained with less size.

In the proposed paper we are concentrating mainly on full adder implementation as it finds use in many of the low power applications. A basic full adder can be implemented with XOR gate, AND gates and OR gate. The logic for sum can be realized using XOR gate whereas the logic for carry can be realized using AND and OR gates. It shows that the entire full adder logic is based on its sum and carry outputs. Reducing the transistor counts in sum and carry logic may reduce the size of the full adder. For that purpose a mixed CMOS based full adder circuit is proposed in the present paper.

A mixed CMOS based full adder is realized as a combination of both NMOS transistors and PMOS transistors. By using pass transistor logic in the multiplexers, the number of transistor count is reduced to a great extent when compared to the static CMOS full adder circuit. As it requires less power to perform the required logic it can be used in many of the low power applications. By using this logic the signal propagation delay can also be reduced which makes the proposed logic used for high speed applications. As the logic requires less number of transistors, it requires less silicon area.

The circuit diagram of mixed CMOS based full adder is

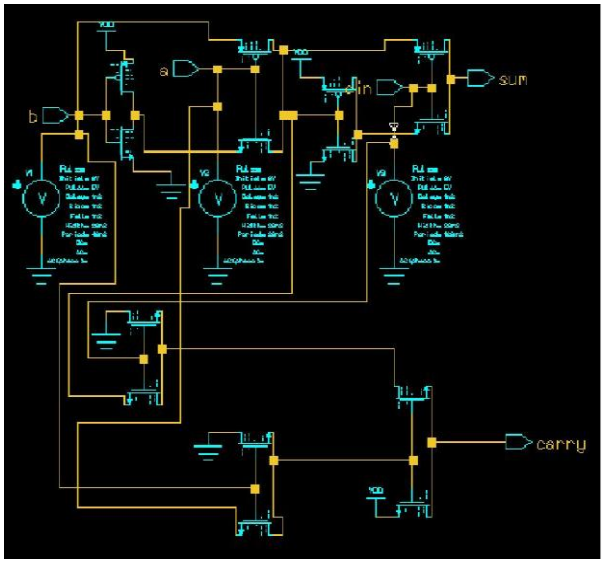

Figure 10. Design of Mixed CMOS based full adder

The figure shows the design of multiplexer based full adder that uses mixed CMOS pass transistor logic. It uses only 16 transistors when compared to the conventional static CMOS that uses 54 transistors. This shows that by using the proposed logic the area of the chip can be reduced to a great extent.

VI. SIMULATION RESULTS

The simulation results for the proposed logic are

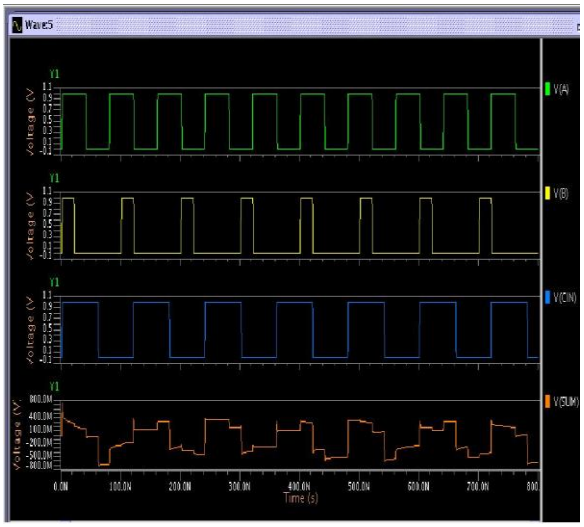

Figure 11. Simulation results for the generation of sum using PMOS transistors

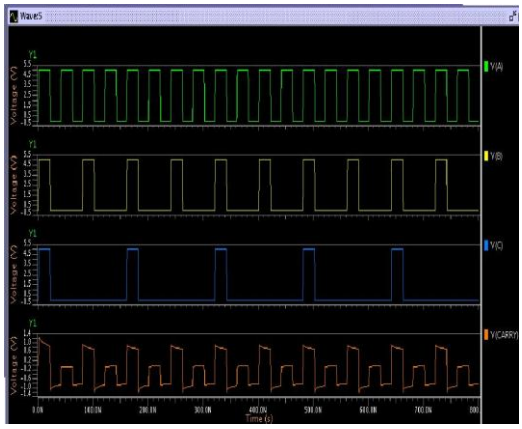

Figure 12: Simulation results for the generation of carry using PMOS transistors

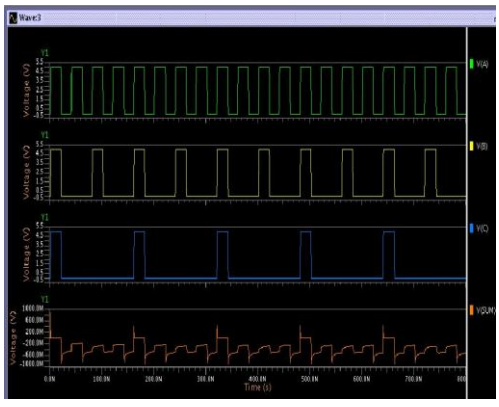

Figure 13: Simulation results for the genaration of sum using NMOS transistors

The above figures shows the simulation results for the proposed design of full adder. The post layout simulation of proposed full adder has been carried out with all combinations of inputs. Each circuit is simulated with the same testing conditions. Since a circuit responds differently to different input combinations, so the output is verified for all eight possible input combinations. Some degradations may occur in the output waveforms which may be reduced completely by careful designing of interconnection between the Mos devices. The results were simulated using Mentor Graphics tool.

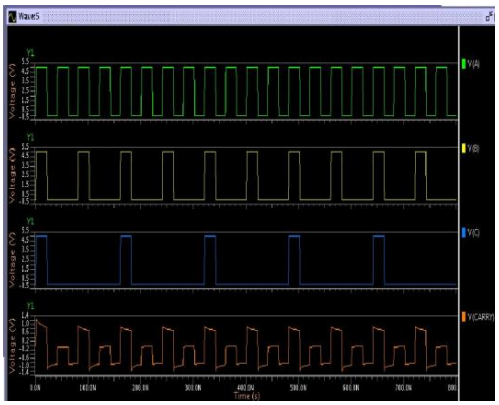

Figure 14: Simulation results for the generation of carry using NMOS transistors

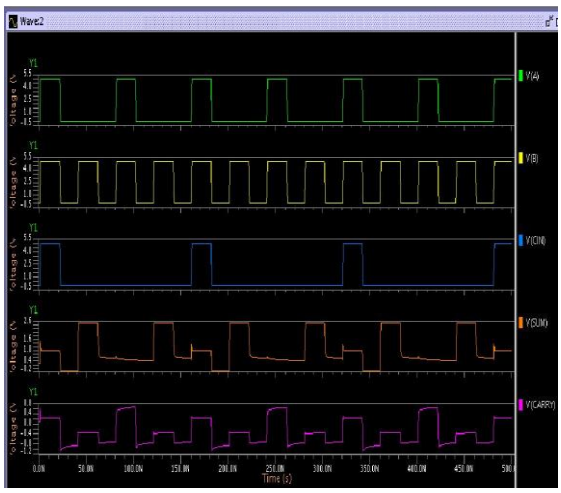

Figure 15: Simulation results for the proposed mixed CMOS based full adder

The following table shows the comparison of performance parameters of different designs for the proposed full adder.

Table 1: Performance parameters of proposed full adders

Parameter	Memory space(bytes)	Power dissipation(watts)	Latency	Average number of iterations	Number of transistors
Mixed CMOS	43405312	393.9778P	0.0000%	3.067720	14
PMOS(sum)	43405312	3.1933U	0.0000%	2.985185	10
PMOS(carry)	43405312	638.2011N	0.0000%	3.362069	12
NMOS(sum)	43405312	9.0434P	0.0000%	3.223065	10
NMOS(carry)	43405312	9.0434P	0.0000%	3.223065	12

From table 1, it can be observed that the power dissipation of mixed CMOS full adder is less comared to PMOS full adder and NMOS full adder circuits. Because of these advantages it can be used in many of the low power applications which is considered to be an important feature in portable devices.

VII. CONCLUSION

In the present work, the full adder design is realized in three different ways with the help of PMOS, NMOS and CMOS transistors. Further the design is implemented by using pass transistor logic in 2x1 multiplexers. The number of transistors required for realizing mixed CMOS design of full adeer is less than the number of transistors required in realizing the design of full adder using PMOS and NMOS transistors independently. So , the required logic can be realized within a small area when compared to the conventional static CMOS ull adder design. Simulation result shows that this proposed full adder achieves better power reduction when compared with other commonly used full adders.

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