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A Novel Low power and Area efficient Carry Look Ahead Adder Using GDI Technique

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Abstract—A full adder is one of the essential component in digital circuit design, many improvements have been made to reduce the architecture of a full adder. The proposed method aims on Gate diffusion input (GDI) which is a low power technique to design any digital system. Mostly 90% of the power consumption is due to of dynamic behavior of the circuit. Dynamic component of power is reduced in GDI technique as the source of PMOS is not permanently connected to Vdd, and it also reduces the latency of the circuit .In this paper we introduce a novel low power and Area efficient Carry Look Ahead Adder using refined full adder. The results shows that the designed adders have superior performance compared with the existing adders in terms of power dissipation and transistor count. The design is simulated using Mentor graphics tool with a supply voltage of 5V.

***Keywords*- FullAdder, GDI Technique, Low Power, Power-Delay-Product (PDP**).

I. INTRODUCTION

Moore's[10] law explains the requirement of the transistors for VLSI design it gives the empirical observation that transistor density and performance of integrated circuits, doubles every year, which was then revised to doubling every two years[11]. Unfortunately, such performance improvements have been accompanied by an increase in power[2] and energy dissipation of the systems. Higher power and energy dissipation[6] in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation[5] of high-performance systems will be a critical design constraint. To reduce the power and area requirements of the computational complexities, the size of transistors are shrunk into the deep sub-micron region[12] and predominantly handled by process engineering. Many design architecture and techniques have been developed to reduce power dissipation complementary logic, Pseudo NMOS[1], Dynamic CMOS[14], Clocked CMOS logic (C2MOS), CMOS Domino logic[1], Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL)[4] have been proposed. Among the various building blocks in digital designs one of the most complex and power consuming is the

Adders[8]. Although several Adder designs have been proposed to reduce power consumption[15], they are not suitable for operation in the sub-threshold region. In addition these designs require a large number of transistors, resulting in a large area, not suitable for small, low-priced systems. The power consumption of a CMOS[4] circuit can be decomposed into two basic classes: static and dynamic.
The steady state power dissipation[12] of a circuit is expressed by the following relation

$$P_{stat} = I_{stat} V_{DD} \text{ ----------(1)}$$

The dynamic[12] component of power dissipation is due to its transient switching behavior of the CMOS device

$$P_{dyn} = \alpha C V_{DD}^{2} f \text{ ……..(2)}$$

This paper is organized as following. Section II reviews previous work. Section III introduces implementation of carry look ahead adder. Simulation and results are shown in Section IV, followed by the conclusion in Section V.

II. PRINCIPLE OF GDI TECHNIQUE

Gate Diffusion Input(GDI)[3] is a new technique of low power digital circuit design. This technique is used to reduce power dissipation, propagation delay and transistor count of digital circuits while maintaining low complexity of circuit design. The GDI method is based on the use of a simple cell as shown in Fig. 1. Basically, the basic cell is seems to be like a standard CMOS inverter, but there are some important differences. The GDI cell contains three inputs: (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are connected to N or P respectively, so it can be arbitrarily biased at contrast with a CMOS inverter.

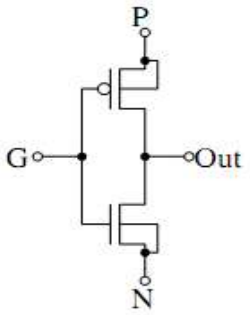

Fig. 1. Basic Gate-Diffusion Input Cell

TABLE I
TRUTH TABLE OF THE BASIC GDI CELL

N	P	G	Out	Function
'0'	B	A	$\overline{A}B$	F1
B	'1'	A	$\overline{A}+B$	F2
'1'	B	A	$A+B$	OR
B	'0'	A	AB	AND
C	B	A	$\overline{A}B+AC$	MUX
'0'	'1'	A	$\overline{A}$	NOT

A.Conventional Static[9] CMOS full adder[16]:

The conventional CMOS logic gate full adder[16] is shown as Fig. 2 while the equation of a full adder are present as equation(1) - (4) [6].

$x + y + C_{in} = 2C_{out} + Sum$ ----------(3)

$C_{out} = (y(x \oplus y)) + (C_{in}(x \oplus y))$ ----(4)

$Sum = x \oplus y \oplus C_{in}$ ----------(5)

The first full adder structure in this section consists of 10 transistors[5][7]. This full adder is implemented with the help of 2-XOR cell .The advantage of this cell is better performance and less silicon area. The fig 2 and fig 3 is as shown below:

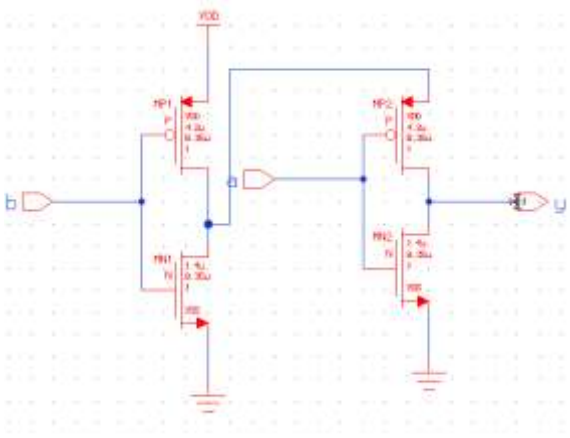

Fig. 2. XOR cell with the GDI technique

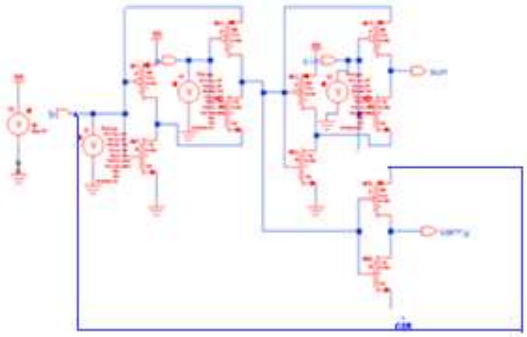

Fig. 3. 10T Full adder cell with the GDI technique

III. IMPLEMENTATION OF CARRY LOOK AHEAD ADDER

The ripple-carry adder, its limiting factor is the time it takes to propagate the carry. The carry look-ahead adder(CLA adder)[13] solves this problem by calculating the carry signals in advance, based on the input values. The result is a reduced carry propagation time.To be able to understand how the carry look-ahead adder works, we have to manipulate the Boolean expression dealing with the full adder. The Propagate P and generate G in a full-adder, is given as:

$Pi = Ai \oplus Bi$ --------(6)Carry propagate

$Gi = Ai \cdot Bi$ ------- (7)Carry generate

Notice that both propagate and generate signals depend only on the input bits and thus will be valid after one gate delay.

The new expressions for the output sum and the carryout are given by:

$S_i = P_i \oplus C_{i-1}$--------(8)

$C_{i+1} = G_i + P_iC_i$ ------(9)

These equations show that a carry signal will be generated in two cases:

1) if both bits Ai and Bi are 1

2) if either Ai or Bi is 1 and the carry-in Ci is 1.

Let's apply these equations for a 4-bit adder:

$C_1 = G_0 + P_0C_0$----------(10)

$C_2 = G_1 + P_1C_1 = G_1 + P_1(G_0 + P_0C_0) = G1 + P_1G_0 + P_1P_0C_0$----------(11)

$C_3 = G_2 + P_2C_2 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$----------(12)

$C_4 = G_3 + P_3C_3 =$

$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$----------(13)

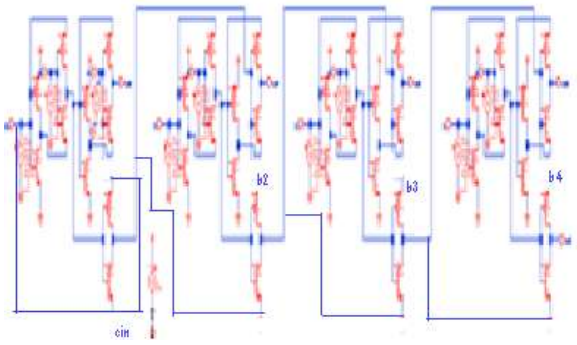

Fig. 4. Carry Look ahead adder using GDI technique

IV. RESULTS AND DISCUSSION

The full adder operates in 100 MHz range. In fact, in addition to normal transistors, circuits are tested in corner cases with fast and slow transistors and their combinations too. The difference in this stage is in consumption power and falling and rising times so this subject looks simple due to the difference in NMOS and PMOS transistors speed .After the simulation, the layout of circuit is drawn. By the post simulation result along with a few corrections have achieved in sizes that the circuit has an accurate operation. Simulation results are performed by Mentor graphics tool. The waveforms of proposed design at 5v is as shown in figure 5 - 7.

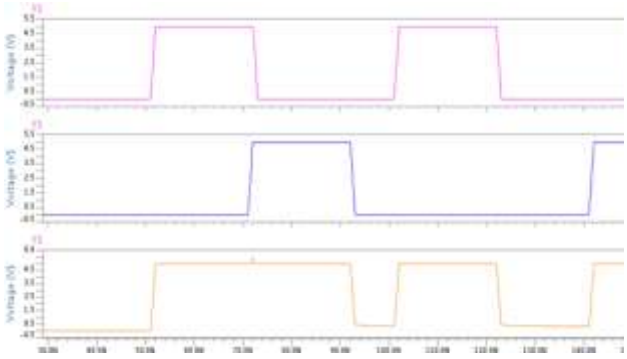

Fig.5. waveforms at 5v and 100MHZ of XOR

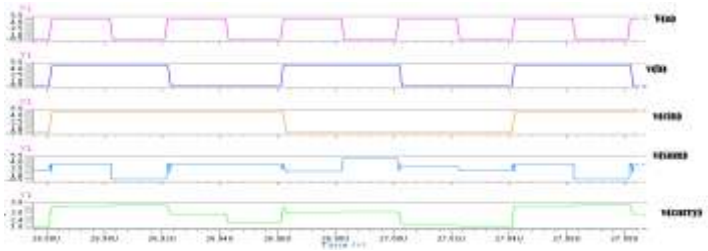

Fig.6.waveforms at 5v and 100MHZ of Full Adder.

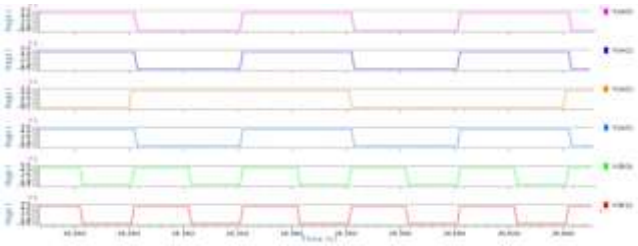

Fig.7. waveforms at 5v and 100MHZ of Carry Look Adder.

Table.2.Comparison of existed full adders with proposed one in terms of transistor count and power dissipation.

Strucures	Transistors count	Power (µw)
14T	14	6.4
CPL	18	2.5
TFA	16	12
TGA	20	-
C2MOS	28	-
HYBRID	26	2.22
FA24T	24	1.66
BRIDGE	26	1.66
N-CELL	14	1.62
DPL	24	2.35
MOD2F	26	2.23
HPSC	22	0.25
TSAC	26	-
Proposed full adder	**10**	**1.13**
CLA adder	**40**	**9.568**

V. CONCLUSION

In this paper different CMOS logic design families has been reviewed and evaluated based on the performance metrics like area, power, delay and transistor count. But the proposed techniques have the disadvantages of transistor count, delay and power dissipation. So a new technique, Gate-Diffusion-Input (GDI) technique has been adopted for reducing the transistor count with full swing. The GDI technique has been implemented in Full Adder and the comparison results have been shown.

The implementation of Carry Look Ahead Adder has been presented in GDI technique and can be extended to higher bit adders.The future research activities may include integration of the proposed Carry Look Ahead Adder in complex digital systems, combining sequential and combinational logic.

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