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Design of WLAN RF front end LNA for Noise & Gain Improvement

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Abstract—***The design of a Low Noise Amplifier (LNA) in Radio Frequency (RF) circuit requires the trade-off many importance characteristics such as gain, Noise Figure (NF), stability, power consumption and complexity).In this paper the aim is to design and simulate a single stage LNA circuit with high gain and low noise using MOSFET(NMOS) for frequency 2.4 GHz. A single ended LNA has successfully designed with 18.8-19.2 dB forward gain and 1.986 dB noise figure, reverse isolation more than 28 dB at the frequency of 2.4 GHz.***

Keywords— **Low Noise Amplifier, Noise Figure, Gain, Stability.**

I. INTRODUCTION

In first stage of each microwave receiver there is Low Noise Amplifier (LNA), this stage has important rule in quality factor of the receiver. A low noise amplifier (LNA) is utilized in various aspects of wireless communications, including cellular communications, wireless LANs and satellite communications. An LNA provides a steady gain [1] over a specified frequency bandwidth. One common application is the use of a LNA as the input stage of a receiving circuit, such as in a cellular mobile communication device. The LNA must be able to provide enough amplification with minimal noise added to the system in order to improve SNR. It also should be linear enough to tolerate spurious interferers coming from the wireless channel. Inductive source degenerated LNA is used for high linearity and low thermal noise.

The design of an LNA imposes many challenges first of all the signal strength can be tens of millions times lower than the in-band interferers[1]. The pre select filter, which is mandatory between the antenna and the LNA, selects the required band of interest. The presence of the desired weak signal along with strong interferers at the input of the LNA enhances the non-linear effect of the LNA. Due to the non linearity[6], the gain of the LNA becomes a decreasing function of the "1–dB compression point" where the gain falls by 1 – dB below its ideal value. Also the interferers can be capable of "desensitizing and blocking" the desired signal may experience a vanishingly small gain due to the reduction of the average gain by the strong interferer. One more consequence of the nonlinearity is the "cross modulation" which results the transfer of modulation from one carrier to the other. Another important affect of these blocking signals is the "Inter-modulation"[9]. If the signal is nearer to two strong interferers then their third order Inter-modulation product falls in the frequency band of the desired signal and corrupts the signal of interest. This defines the IIP3 (3rd order inter intercept point)[10]. The RF input signal to the LNA is coming from the pre select filter, which is the RF source here [3]. So the LNA must present good "power matching" for maximum power to be transferred from the RF source. In addition to power matching the LNA should have proper "noise matching" to minimize the noise figure[6]. One more constraint in the design of the LNA is the "power dissipation". In battery operated systems like mobile transceivers [5] the power consumption should be as low as possible to increase the battery time. The "gain" of the LNA should be large enough to decrease the noise contribution of the following stages in the receiver and it should be small enough not to saturate the following stages in the receiver chain.

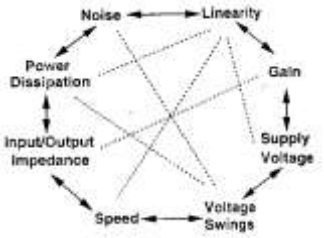

Figure 1.RF Design Octagon

II. PROPOSED DESIGN FOR INDUCTIVE LNA

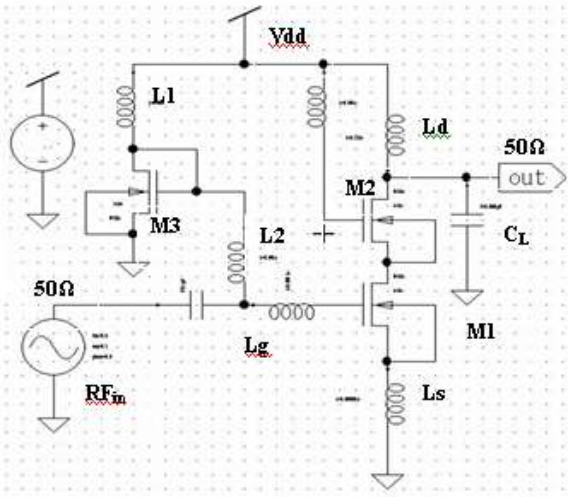

Figure 2: Proposed LNA schematic design with inductors replacing all resistive components for reduction of thermal noise .

III. LNA CIRCUIT DESIGN

The complete schematic of LNA is shown in figure 1. Lg, Ls and Ld are implemented by using spiral inductors. The method employed here is cascode source inductive degeneration. Cascoding transistor M2 is used to reduce the interaction of the tuned output with the tuned input (for improved reverse isolation), and to reduce the effect of the gate-drain capacitance Cgd of M1. Use of common gate stage in cascoding provides high output impedance. The inductors Lg and Ls are chosen to provide the desired input resistance.Ld and the capacitance of the transistors M2 form a tank circuit to tune the LNA to 2.4GHz.M3, L1and L2form a bias circuit. Transistor M3 essentially forms a current mirror with M1, where its width is a small fraction of the width of M1's in order to minimize the power overhead of the bias circuit. Cin and Cout are DC blocking capacitors. The load Ld is tuned to manage the tradeoff between gain, output matching, and power dissipation of LNA. Both input and output are matched to 50Ω.

Due to the limited choice of inductor and capacitor values in the technology we choose, the matching network becomes very challenging. With the comprehensive consideration of the chip size and different performance trade-off, Cin and Cout play important roles in input and out-put matching respectively. The load L3 is tuned to manage the tradeoff between gain, output matching, and power dissipation of LNA. Both input and output are matched to 50Ω.

We choose the same variation for Lg, Ls, and Ld, then we Calculate ΔL/L, and Δgain/gain[3]. The gain is in an absolute value, not in dB.

The overall stage transconductance Gm is

$Gm=gm1Qin = gm1/\omega 0Cgs\ (Rs+\omega TLs)$

Where $\omega 0 =1/\ [(Lg) +Ls\ Cgs]^{1/2}$

The gain of LNA is $Av =Gm\ Z_L$.

It shows that the gain is determined by transistor size, Lg, Ls, and load impedance Z_L.

IV. LNA DESIGN CONSIDERATIONS

1. Limitation on the Gain: Friis' Equation [11] says that the gain of the LNA (1st stage) as high as possible for minimum Noise Figure.

$F_{Total}=F_1+F_2-1/G_1+\ldots\ldots..+F_N-1/\prod_{i=1}^{N} Gi$

2. Non Linearity Effects: The input-output relationship of non linear active devices can be modeled as:

$y(t) =\alpha_1 x(t)+ \alpha_2 x^2(t)+ \alpha_3 x^3(t).$

In Analog IC design the non linearity is not that much severe as in the case of RF IC design because in RF the strong interferers cause the nonlinear terms (x^2 and x^3 terms) to have significant magnitude.

3. Matching (Impedance, Power and Noise Matching):

The matching designed at the input of the LNA to achieve the minimum NF is called as Noise Matching.

Impedance Matching requires Z source = Z termination = Z in (LNA)

Power Matching requires, Z source = Z *termination = Z * in (LNA)

Noise Matching requires source is such that it minimizes the Noise Figure.

4. Noise: The two noise sources are related by the correlation admittance. The noise factor, *F*, is described by Equation;

$$F = 1 + \frac{R_{sg} + R_g}{R_S} + \left(\frac{\omega}{\omega_t}\right)^2 \gamma_{gs01} AB + \frac{4\gamma g_{d03}\left(1-\omega^2 L_{12} C_{gs3}\right)^2}{g_{m1}^2 \omega_t^2 L_{12}^2} A,$$

Where,

$$A = \frac{\left[(R_S + \omega_t L_s)^2 + \left(\omega L_s + \omega L_g - \frac{1}{\omega C_{gs1}}\right)^2\right]}{R_S},$$

$$L_{12} = \frac{L_1 L_2}{L_1 + L_2},$$

$$B = \left|\frac{1}{1 + \frac{\omega_t L_s}{R_S + j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs1}}}}\right|^2,$$

[3]

$$F_{=1+} \frac{\overline{i^2_{n,D}} R_L^2}{\overline{V^2_{n,RS}} Q_{in}^2 g_m^2 R_L^2}, \quad \overline{i^2_{n,D}} = 4KT\gamma g_m, \quad \overline{V^2_{n,RS}} = 4KT R_s$$

$$F_{min,p} = 1 + 5.6\frac{\omega}{\omega_T} \qquad [8]$$

Resistors R_g & $R_{Lg\ represent}$ the resistances of the transistor M1 gate and the inductor Lg.Since their values are negligible in regards to source resistance Rs. their contribution to the total noise figure is mostly ignored.

IV. SETTING DC BIAS VOLTAGE

Before applying the AC signal to the device we have to check the dc bias operating point for amplifier.

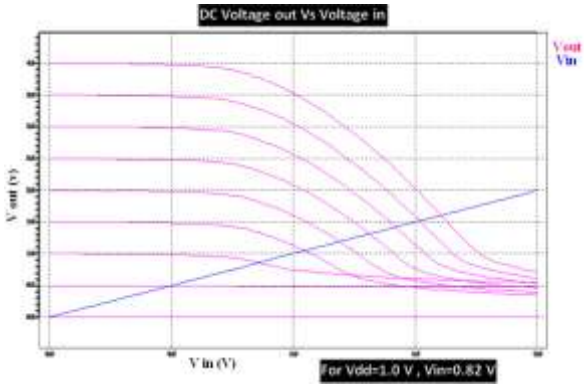

Figure 6: DC Bias operating point

V. OUTPUT VOLTAGE SWING

The amplifier swing is one of the important parameters, because application of large signal AC to the gate may cause transistor to change its region i.e. out of saturation.

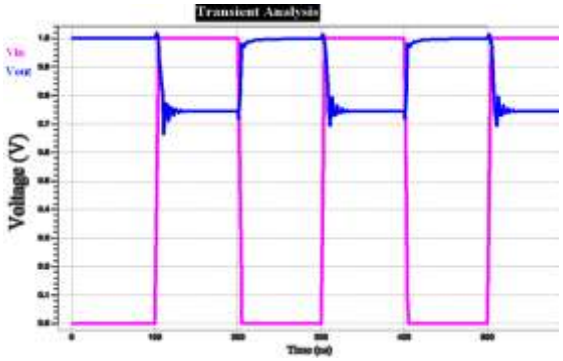

Figure 7: LNA output voltage swing

VI. LNA STABILITY ANALYSIS

In the presence of feedback paths from the output to the input, the circuit might become unstable for certain combinations of source and load impedances. An LNA design that is normally stable might oscillate at the extremes of the manufacturing or voltage variations [1], and perhaps at unexpectedly high or low frequencies [3].

The Stern stability factor characterizes circuit stability as in Equation:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|}$$

$$|\Delta| = |S_{11}S_{22} - S_{21}S_{12}| < 1$$

K > 1& Δ < 1, means our amplifier is stable.

For NMOS in saturation: Vds>Vgs-Vth.(For Each NMOS)

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VII. IMPLEMENTATION OF PROPOSED WORK

Step - 1:

$I_1 = I_2 = 5mA$ (Low Power consumption)

Step - 2:

$$W_{M1} = \frac{1}{3WL_{eff}C_{ox}R_s}$$

$$W_{M1} = \frac{1}{3\times 0.35\mu\times 4.6m\times 50\times \omega_o} \quad \begin{Bmatrix} R_s = 50\Omega, C_{ox} = 4.6mF/m^2, \\ \mu_n C_{ox} = 170\mu A/V, L_{eff} = 0.35\mu m, \\ \omega_o = 2\pi f_o, f_o = 2.4GHz \end{Bmatrix}$$

$$W_{M1} = 3.9\times 10^{-4}$$

$$W_{M1} = 3.9\times 10^{-4} = 390\mu m$$

Step - 3:

$$C_{gs1} = \frac{2}{3}W_{M1}L_{eff}C_{ox}$$

$$C_{gs1} = \frac{2}{3}\times 390\mu\times 0.35\mu\times 4.6m = 0.41pF$$

$$g_{m1} = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} I_{DM1}}$$

$$g_{m1} = \sqrt{2\times 170\mu\times\left(\frac{390}{0.35}\right)\times 5m} = 43mA/V$$

$$\omega_T \approx \frac{g_{m1}}{C_{gs1}} = \frac{43mA/V}{0.41pF} = 104Grad/Sec$$

Assuming $\gamma = 2$

Now $F_{min} = 1 + 5.6\frac{\omega_o}{\omega_T}$

$$F_{min} = 1 + 5.6\frac{2\pi 2.4G}{104G} \approx 2.55dB$$

$NF \approx 2.55dB$

Step - 4:

Source and gate inductance such that they cancel C_{gs} and set 50Ω input impedance

$\omega_o = 2\pi f_o = 2\pi 2.4 = 15Grad/Sec$

From previous problem

$$R_s = R_{Transformed} = g_m\frac{L_s}{C_{gs}} = L_s\omega_T$$

$$L_s = \frac{R_s}{\omega_T} = \frac{50}{100G} \cong 0.5nH$$

$L_s = 0.5nH$ can be implemented using Band wire.

Now $L_g + L_s = \frac{1}{(\omega_o^2 C_{gs1})}$

$$L_g + L_s = \frac{1}{(15G)^2\times 0.41pF} = 10.81nH$$

$L_g \approx 10nH$

Step - 5:

$$L_d = \frac{1}{\omega_o^2 C_L} \qquad \because C_L = 1pF$$

$$L_d = \frac{1}{(15G)^2\times 1pF} \cong 4.4nH$$

$L_d = 4.4nH$

Step - 6:

Size of M3 is chosen to minimize power consumption

$W_{M3} = 70\mu m,\ R_{REF} = 2K\Omega \Rightarrow I_3 = 0.6mA$

$R_{BIAS} = 2K\Omega$ (Large enough so that it's equivalent current noise can be neglected)

$C_B = 10pF$ ($X_C \approx 6.6\Omega$ so good value @ 2.4G $X_B = \frac{1}{2\pi f_o C_B} = 6.6\Omega$)

Step - 7:

Size M2 = M3

So that they can have shared Drain Area..

[12]

VIII. SIMULATION RESULTS

All the simulations are done using input signal of 1.0 volts for different outputs of 2.4 GHz Low Noise Amplifier for wireless networks using TSMC 0.18um technology.

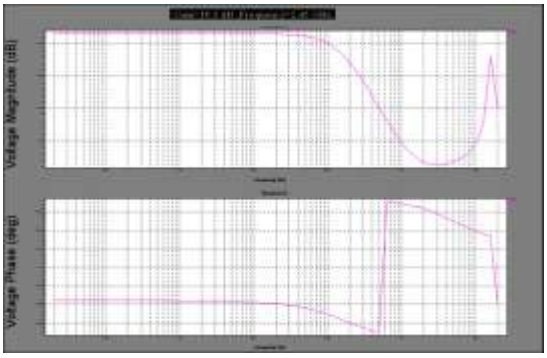

Figure 8: Voltage magnitude (19.1dB) and Phase magnitude (deg) at 2.4 GHz.

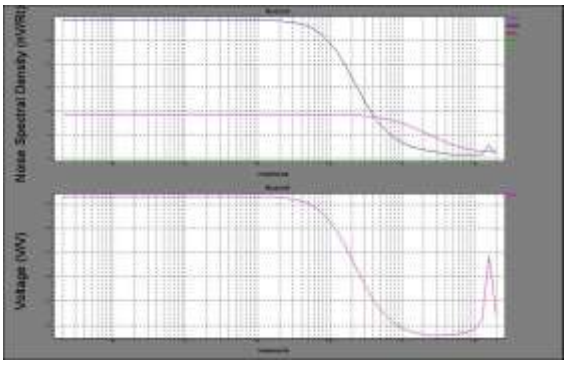

Figure 9: Noise spectral density (nV/Rt) and voltage at 2.4GHz.

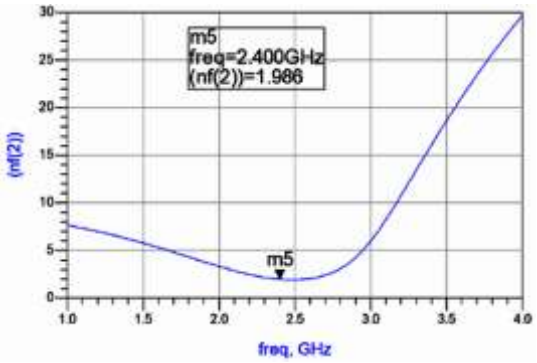

Figure10: Noise figure of the LNA (Minimum Noise Figure is 1.986 dB at 2.4 GHz)

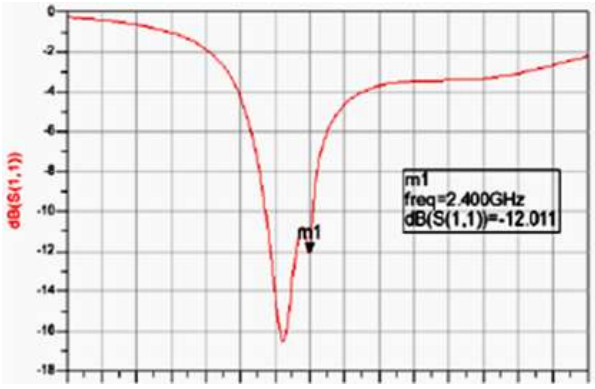

Figure 11: Reverse isolation of LNA (More than -12 dB)

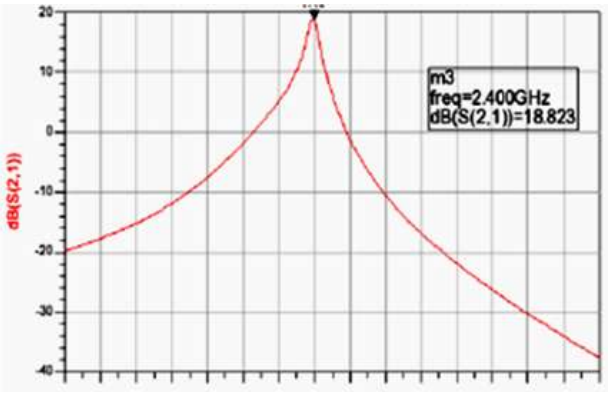

Figure 12: LNA Forward Voltage Gain 18.82 dB (S21)

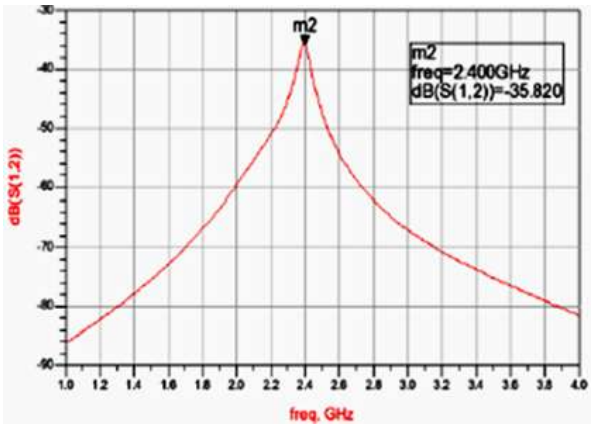

Figure 13: Reverse Isolation of more than - 35 dB.

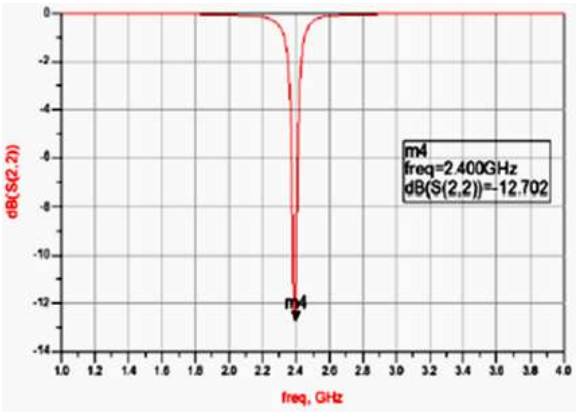

Figure 14: S22 Output Reflection Coefficient -13 dB

IX. CONCLUSION

In this paper a 1.2 volt 2.4 GHz low noise amplifier with inductive design for wireless communication is proposed for low noise and low power consumption for improvement the battery life and improved distance of WLAN applications, using TSMC 0.18um technology [10]. Tanner EDA and Agilent ADS software tools are used to simulate the proposed design.

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