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Ultra Wideband Low Noise Power Amplifier

Gauri P. Borkhade
Department of electronics and telecommunication
Government college of Engineering,
email -gborkhade@gmail.com,
Amravati,India.09766937639

Dr.D. S. Chaudhari
Department of electronics and telecommunication
Government college of Engineering,
Amravati,India
email -ddsscc@gmail.com

Abstract **- A modified CMOS realization of ultra wideband low noise power amplifier is proposed in this paper. A method is presented for design of high frequency power amplifier using 45nm CMOS technology. Techniques including single stage amplifier with passive load, differential amplifier and operational trans-resistance are used. The goal is to highlight the efficient power amplifier architecture for achieving low power dissipation, noise at low power supply voltage. The unique behaviour of MOS transistors in sub threshold region allowed a designer to work at low input bias current with low voltage. Simulation result shows that power amplifier provides amplification up to 5GHz.Power consumption is 0.023mW with 1v supply.**

Index Terms **: Power amplifier, Ultra wideband, low noise, CMOS technology**

INTRODUCTION

In ultra wideband (UWB) systems, the power level from the UWB transmitter should be small enough not to interfere with the existing communication systems. As a result, UWB systems need not require large transistors as part of the power amplifier circuit and this ultimately translates to lower power consumption. Achieving a high gain and good impedance match over the entire frequency band makes the design a challenging task. Power Amplifiers (PA) are a key part of the RF front-end in any transmitter. It is a very power-starving block and usually the last stage of the transmitter end. Power amplifiers boost the signal power high enough such that it can propagate the essential distance over the wireless medium. Typically, this power is delivered to an antenna which acts like a load. The output power level from a PA is determined by the application it is designed for. It can range from a few milli-watt for home networks to hundreds of watts at base stations. In a narrowband application, the PA is designed for a particular frequency range and all the parameters are measured at that frequency. However, the frequency range to be covered for UWB is of the order of several GHz. So the PAs considered in this research target the 3.1 to 5 GHz range. Techniques used to design wide band trans-receiver have become essential in recent years mainly because of emerging applications. Traditional techniques used for design narrowband low noise amplifier such as adding an inductor at the load to generate resonance at a certain frequency are not suitable for wideband amplifiers. While maintaining low power consumption to meet requirements across wide bandwidth various topologies have been used. The goal of amplifier is to multiply the input signal by significant factor. According to several authors power amplifiers are designed by using different techniques such as distributed **Dr**, differential, push-pull and operational amplifiers. Interest has been devoted to the design Power Amplifier by using concept of the operational trans-resistance amplifiers and push-pull amplifier.

The Aim is to achieve the low power consumption, high stability for amplifier block used in trans-receivers. Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. Hence to have very low power consumption, this work is decided to implement using CMOS technology. The microelectronics has achieved a phenomenal development, due to the rapid advances in integration technologies. The number of applications of integrated circuits in telecommunications, high-performance computing and consumer electronics has been rising. Typically, the required computational power of these applications is the motivation for the fast development of this field.

This development is expected to maintain, with important implications on VLSI and systems design. One of the most important characteristics of information services is their need for very high processing power and bandwidth. The devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility. More composite functions are required in different data processing and telecommunications devices; the need to integrate these functions in a small package is increasing. The levels of integration measured by the number of logic gates in a monolithic chip has been progressively rising for about three decades, mainly due to the speedy progress in processing technology and interconnect technology. The important significance here is that the logic complexity per chip has been rising exponentially. This work investigates the design of a CMOS Power Amplifier for UWB applications. Due to the advantage and current demand in communication technology, the effort has been taken to design proposed Power Amplifier using 45 nm CMOS technology.

PRINCIPLE

The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The effective gate length required for 45 nm technology is 25nm. The ever-growing popularity of CMOS devices has made the main stream technology for designing complex monolithic systems with dense design, low power dissipation, low supply voltage and highly automated synthesis. Proposed work is aimed at to design Low Power, Low noise, High performance, power amplifier using VLSI technology. The 45nm transistor can switch on and off approximately 300 billion times a second. A beam of light travels less than a tenth of an inch during the time it takes the 45nm transistor to switch on and off [5].

Interest has been devoted to the design Power Amplifier by using concept of the operational trans-resistance amplifiers (OTRA) and push-pull amplifier. The OTRA is not slew limited like voltage op-amps. High bandwidth is providing which is independent of the gain. Hence, it does not suffer from constant gain bandwidth product like voltage op-amps circuits. The OTRA is a three-terminal analog building block that is defined by the following three equations:

$$V+ = 0*[I+] + 0*[I-] + 0*[Io]$$

$$=> \quad Rm=0$$

$$V\_ = 0*[I+] + 0*[I-] + 0*[Io]$$

$$=> \quad Rm=0$$

$$V\,o = Rm*[I+] + [-Rm]*[I-] + 0*[Io]$$

Where *Rm* is the trans-resistance

The input terminals are virtually grounded, leading to circuits that are in sensitive to stray capacitances. The trans-resistance gain *Rm* approaches infinity and applying external negative feedback will force the two input currents, *I*+ and *I*– to be equal[10].

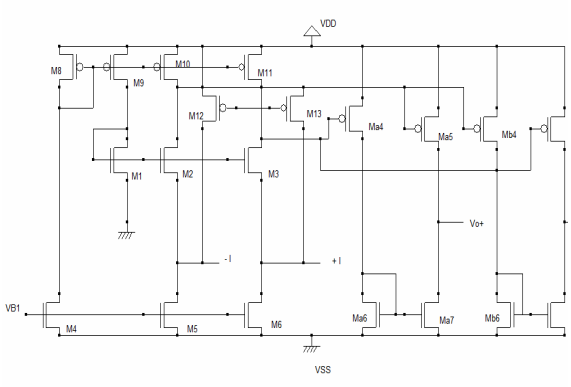

Figure 1 : Low noise power amplifier with differential pairs

Figure 1 shows schematic of power amplifier. The CMOS realization of the proposed high open loop gain power amplifier consist 20 PMOS. These transistors are designed with large widths in order to lower the output resistance. Design is necessary when a high current drive is required the antenna dipole for radio-frequency emission, high output capacitor. It is based on the same input stage of the Mustafa and Soliman OTRA proposed while a differential gain stage is used in its place of the single common source amplifier. The transistors Ma4–Ma7 produce the non-inverting output, while the transistors Mb4–Mb7 produce the inverting output. In this structure second stage is mirror image of first stage. The DC off- set current and increased the DC open loop trans-resistance gain reduces by adding the differential gain stage. Width and length of each transistor in circuit provide in table 1.

Transistors	*W* (µm)	*L* (µm)
M1-M3	1	0.04
M4	1	0.04
M5-M6	1	0.04
M8-M11	0.2	0.04
M12-M13	0.2	0.04
Ma4-Ma5	0.2	0.04
Mb4-Mb5	1	0.04
Ma6,Ma7,Mb6 and Mb7	1	0.04

Table 1 Transistor aspect ratio of circuit

LAYOUT

The layout of power amplifier circuit shown in Figure [2] is done using professional software microwind 3.1. The layout has area 0.0084 mm2 , which is fairly small as compared to other power amplifiers. Parasitic extraction and Post simulation is performed successfully.

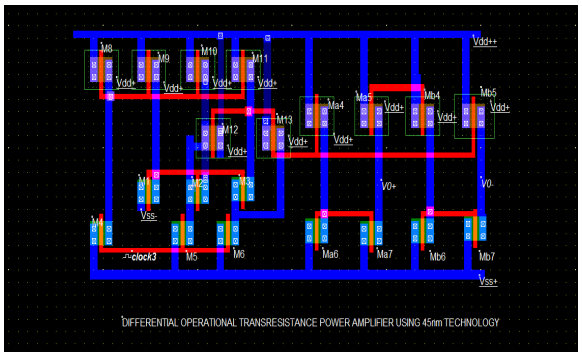

Figure 2 Layout of Power Amplifier using 45nm technology

SIMULATION RESULT

Simulations at the schematic level were performed using microwind 3.1 tool. Power consumption can be calculated from DC simulations. Simulated output voltage wave forms of differential trans-resistance power amplifier shown in figure 3.Output voltages vo+ & vo-are amplified voltage of difference between two input voltage with 1v operating voltage given by clock3. Figure 4 shows simulated voltage and current wave forms of power amplifier. It is evidence that current depends on the input clock of power amplifier.

Static response between output voltage and input clock of power amplifier shown in figure 5.It is obtained between vo- and clock 3. Linearity and output power levels can be estimated from these simulations. Figure 6 illustrates simulated frequency waveforms of power amplifier. Clock of 5GHz frequency applied to amplifier which gives smooth output voltages without interfering noise and fluctuations. It is found that this circuit amplified the signal at 5GHz frequency with power consumption of 0.197mW. Three diamentional view for this layout shown in figure 7.

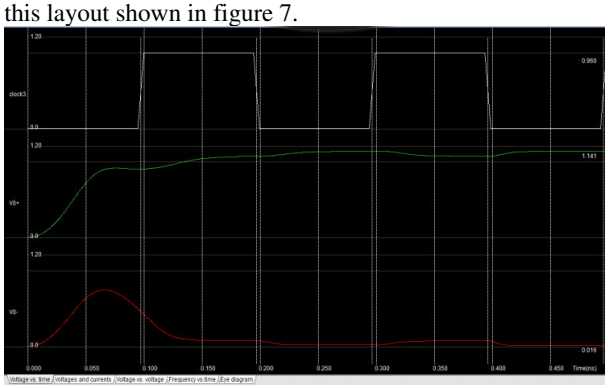

Figure 3 Simulated output voltage wave forms of power amplifier for two different input voltages.

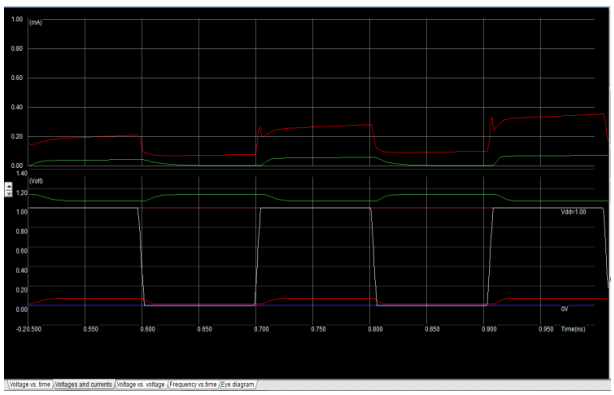

Figure 4 Simulated voltage and current wave forms of power amplifier.

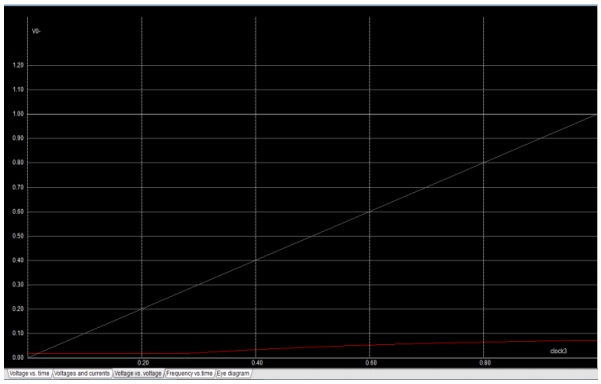

Figure 5 Static response between output voltage and input clock of power amplifier

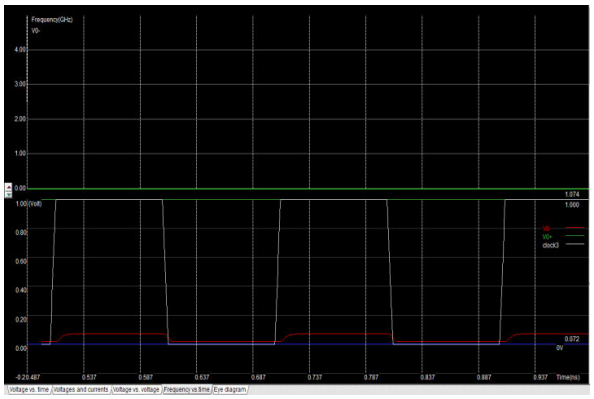

Figure 6 Simulated frequency versus time wave forms of power amplifier.

Following data shows the analysis of power dissipation variation of voltage from 0v to 1v.

For clock 3	**Clock 3 (V)**	**Power (mW)**
	0.000	0.102
	0.200	0.117
	0.400	0.172
	0.600	0.229
	0.800	0.262
	1.000	0.291
For Vo+	**Vo + (V)**	**Power (mW)**
	0.000	0.255
	0.200	0.249
	0.300	0.242
	0.600	0.233
	0.800	0.219
	1.000	0.197

Above data shows that, from parametric analysis of designed ultra wideband low noise power amplifier .The power dissipation vary for different voltage level. Power dissipation for clock3 increases with increase in voltage, at 1V is found to be 0.291mW and power dissipation measured for Vo+ at 1v is found to be 0.197mW, which show that power consumption is very low. In this way very high efficient, optimum area chip is design with low power of 0.182mW and two outputs with stability.

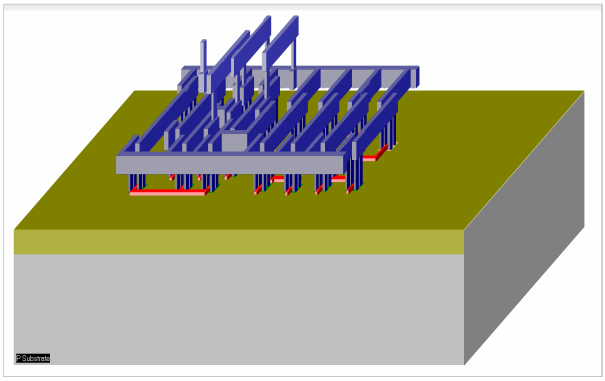

Figure 7 Three dimensional view of differential operational trans-resistance amplifier

Three dimentional view of differential operational trans-resistance amplifier obtained after simulation shown in figure 6. Which shows P-substrate (gray colour), n-diffusion (green colour), metal layer (blue colour), poly-silicon material (red colour).

CONCLUSION

This paper provides layout design architectures for differential operational trans-resistance power amplifier along with simulation results. From simulation result of push-pull power amplifier frequency curve shows operating time 0.45 ns. Speed of amplification is high for high frequency. It is found that this circuit amplified the signal at 5GHz frequency with power consumption of 0.197mW. Simulation of differential operational trans-resistance power amplifier shows the power dissipation vary for different voltage levels. This ultra wideband power amplifier simulate at 5GHz.

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Gauri P. Borkhade received the B.E. degree in Electronics and Telecommunication Engineering from Sant Gadage Baba Amravati University, Amravati in 2008, and currently pursuing the M. Tech. degree in Electronic System and Communication (ESC) at Government College of Engineering Amravati. She presented papers in international conferences ICECE and IEEE. Her interests are in Micro Electronic System Design using VLSI Technology.

Devendra S. Chaudhari obtained BE, ME, from Marathwada University, Aurangabad and PhD from Indian Institute of Technology, Bombay, Powai, Mumbai. He has been engaged in teaching, research for period of about 25 years and worked on DST-SERC sponsored Fast Track Project for Young Scientists. He has worked as Head Electronics and Telecommunication, Instrumentation, Electrical, Research and in charge Principal at Government Engineering Colleges. Presently he is working as Head, Department of Electronics and Telecommunication Engineering at Government College of Engineering, Amravati.

Dr. Chaudhari published research papers and presented papers in international conferences abroad at Seattle, USA and Austria, Europe. He worked as Chairman / Expert Member on different committees of All India Council for Technical Education, Directorate of Technical Education for Approval, Graduation, Inspection, Variation of Intake of diploma and degree Engineering Institutions. As a university recognized PhD research supervisor in Electronics and Computer Science Engineering he has been supervising research work since 2001. One research scholar received PhD under his supervision.

He has worked as Chairman / Member on different university and college level committees like Examination, Academic, Senate, Board of Studies, etc. he chaired one of the Technical sessions of International Conference held at Nagpur. He is fellow of IE, IETE and life member of ISTE, BMESI and member of IEEE (2007). He is recipient of Best Engineering College Teacher Award of ISTE, New Delhi, Gold Medal Award of IETE, New Delhi, Engineering Achievement Award of IE (I), Nashik. He has organized various Continuing Education Programmes and delivered Expert Lectures on research at different places. He has also worked as ISTE Visiting Professor and visiting faculty member at Asian Institute of Technology, Bangkok, Thailand. His present research and teaching interests are in the field of Biomedical Engineering, Digital Signal Processing and Analogue Integrated Circuits.