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Low-power Full Adder array-based Multiplier with Domino Logic

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ABSTRACT

A circuit design for a low-power full adder array-based multiplier in domino logic is proposed. It is based on Wallace tree technique. Clocked architecture results in lower power dissipation and improvements in power-delay product. The proposed technique is general and can be used in all domino logic circuit designs. Higher order multipliers like 16x16, 32x32 may also be implemented using 4x4 bit multiplier and hence a modular design is presented by constructing an 8x8 multiplier using multiple 4x4 multipliers. Average power and TannerTool report for 8x8 Multiplier is as follows, Device and node counts: MOSFETs – 2572, MOSFET geometries - 2 Measurement result summary Average Power found to be 0.11108 microwatt

1. INTRODUCTION

Multiplier plays a significant role in high speed digital signal processing. It's the most important part of the Arithmetic Logic Unit (ALU), FPU and ASIC's where high processing speed is required. Currently, the importance of low power design increases rapidly due to the increasing demand for portable and mobile systems.

Many different types of low power multipliers are proposed, and fabricated as benchmarks for demonstrating various high-speed technologies in many applications [1-3].

Low power design techniques require special attention to avoid significant increment of the circuit's area or sacrifice in the speed performance of the systems. In CMOS technology power consumption can be reduced by decreasing the nodal capacitance, decreasing the power supply voltage or through architecture refinements, where the total power may be reduced by eliminating unnecessary transistors [4]. Dynamic logic and especially domino logic could play an important role in -the future integrated circuits. Domino logic circuits have many advantages such as high speed of operation, minimum used area, low noise margins, and the most important of all, they offer potential power consumption savings since the overall gate capacitance is smaller than their static counterparts [4-7]. For this reason circuit design using domino logic tends to be a very attractive method for high performance, low-power designs.

The potential of domino logic in designing low power circuits is investigated in this paper. As an example, the popular array multiplier is employed, which is based on a Wallace tree diagram technique. In this paper, we introduce a modular multiplier implementation using domino logic. The organization of this paper is as follows. In section *2* the basic structure of the domino logic is presented. The basic circuits used in multiplication using domino logic circuits is explained in section 3. Implementation of multiplier is presented in section 4. Section 5 gives the simulation results obtained in SPICE.

2. STRUCTURE OF THE DOMINO LOGIC

The basic structure of domino logic is shown in Fig. 1. It is a non-inverting structure, and consists of a nMOS transistor network, which implements the required logic function, two transistors (an *nMOS* and a PMOS) where the clock signal is applied and synchronizes the operation of the circuit, and a static CMOS inverter which provides the circuit's output.

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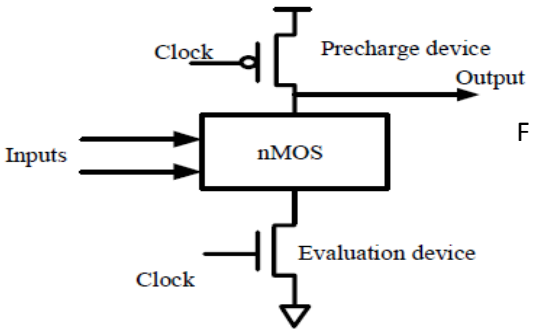

Fig.1 Basic structure of Domino Logic

The period where CLK is low is called the precharge phase. In this phase the internal node, F is charged to power supply voltage while the output node, F, is discharged to ground. The period where CLK is high is called the evaluation phase. In this phase the values of the inputs determine the discharge (F = 0) or not (F = 1) of the internal node The inverter in the output of a domino logic circuit is included for several reasons. First, it is required for proper operation of a chain of domino gates. Second, the internal node F is a weak node, when the clock is high, the high value on that node is not driven [8].

III. Basic Circuits for Constructing Multiplier

Design of Full Adder and AND gate is presented in this section. The full adder is divided into two subcircuits. One is the circuit for SUM operation[9], and the other is the circuit for CARRYOUT operation. *A. The Circuit for SUM Operation* Fig. 2 shows the schematic of the SUM circuit. The SUM circuit is composed of two XOR gates. The XOR gate is modified from the cross-coupled version by replacing the NMOS portion with a clock gated NMOS. In this circuit, the PMOS transistors receive the input signal *A*, *B*, and *Cin*. The operation of this circuit can be divided into two phases: the IDLE PHASE and the EVALUATING PHASE. In the IDLE PHASE, the clock signal *CLK* is 'logic 1', and the output signal *SUM* will be 'logic 0'. In the EVALUATING PHASE, the clock signal *CLK* is 'logic 0', and the corresponding output signal *SUM* will be evaluated according to the input signals *A*, *B*, and *Cin*.

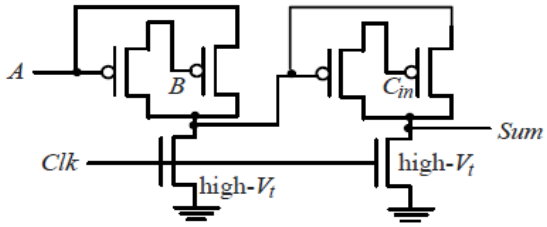

Fig 2. SUM Circuit

B. The Circuit for CARRYOUT Operation
Fig. 3 shows the schematic of the CARRYOUT circuit. The core of this circuit is the domino logic that implements the function of CARRYOUT[9]. This circuit will stay in standby phase when the clock signal *CLK* is 'logic 1'. It will turn in the evaluating phase if the clock signal *CLK* is 'logic 0'. For the high-speed operation, the inverter *I*1 is designed in multi-threshold methodology where a low-*Vt* PMOS transistor is connected with a high-*Vt* NMOS transistor such that the 'logic 0' can pass the inverter at a higher speed.

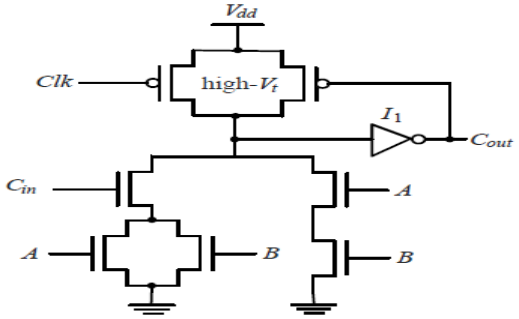

Fig.3: CARRYOUT Circuit

Domino Logic AND Gate

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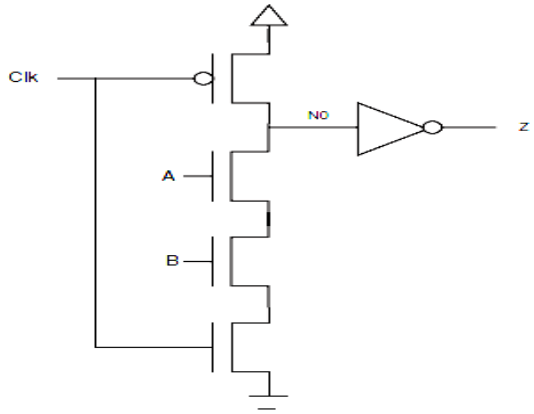
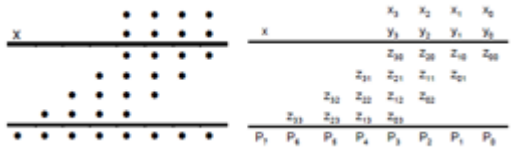


Fig.4: 2 input AND Gate using Domino Logic

IV Implementation of Multiplier

A 4x4 bit Array multiplier is constructed as the basic building block for higher order multipliers. In Fig. 5 the block diagram of the multiplier architecture is shown. Let *1* be the word length of multiplicand, and *k* be the word length of the multiplier [10]. A full adder array based multiplier contains *l x k* AND gates and *1 x (k - I)* 1-bit full adders. To show the characteristics improvement achieved by the proposed technique, a 4 *x* 4 bit multiplier has been implemented, by using the conventional domino logic. As an example, a 0.5pm CMOS technology with power supply voltage *Vdd = 5V,* and threshold voltage *VTN = 0.65V* was used.

Following is the dot notation for the Wallace tree multiplication and partial product matrix for two 4 bit numbers X and Y.



Where $Z_{ij} = X_i Y_j$

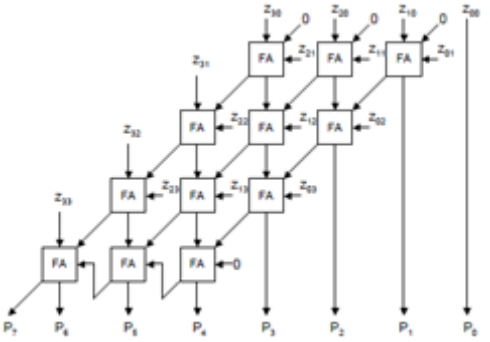


Fig.5 : 4x4 Array Multiplier

The simulation results for 4x4 multiplier is shown in next section.

For modular design a 8x8 multiplier is constructed using multiple blocks of 4x4 multipliers using the structure show below.

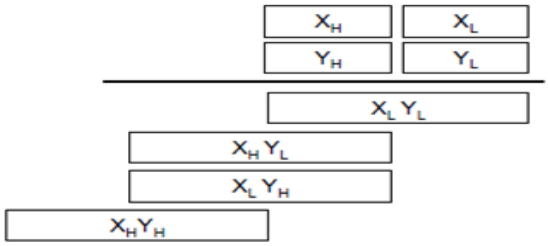


Fig.6: 8x8 Multiplier using 4x4 Multipliers

In this case the numbers X and Y are first split into two parts as XH-XL and YH-YL. The products XL*YL, XH*YL, XL*YH and XH*YH are then calculated in parallel using 4 array multipliers. These products are then added to get the final product P15-P0.

V Simulation Results

All the circuits in section 3 and 4x4 array multiplier in section IV are tested for verification of functionality by applying sample inputs and observing outputs. The average power of the 8x8 Multiplier block is calculated in TannerTools T-SPICE and is presented in this section at the end.

Part A: Verification

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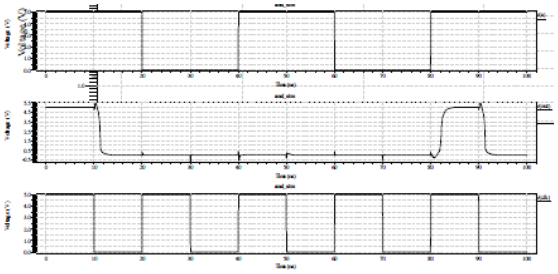

Fig.7 Simulation Result for AND gate

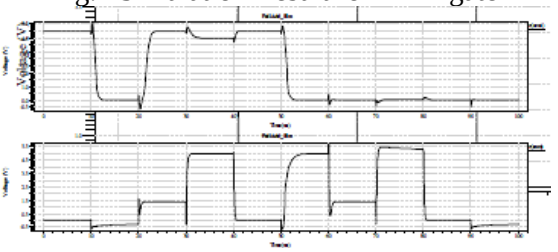

Fig.8 Simulation result for 1 bit full adder

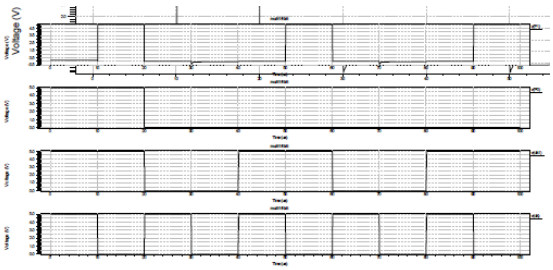

Fig.9: Simulation result for 4x4 Array Multiplier

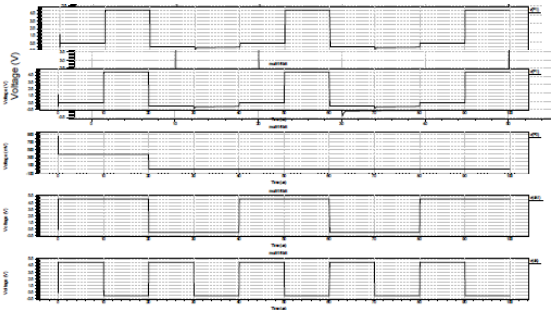

Fig.10 Simulation result for 8x8 Multiplier

Average power and TannerTool report for 8x8 Multiplier is as follows,

Device and node counts:

MOSFETs - 2572 MOSFET geometries - 2

Measurement result summary

avgpower = 1.1108e-007

Implemented in Tanner-13, for low power microwatts and high speed in GB

CONCUSIONS

In this paper a new modular multiplier using domino logic has been proposed. Significant power savings can be achieved while a trade off between power and delay can be adjusted for meeting the circuit design specifications. This is achieved by the efficient way of the realization multiplier using array of 1 bit full adder.

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