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Development of FPGA Based Embedded Web Server Using a Soft-core Processor

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Abstract— **Recent development of softcore processors on Field Programmable Gate Arrays (FPGAs) provide customization of processor to the needs of target application over traditional pre-fabricated processors. Softcore processors are available in the form of softwares whose architecture and behavior are fully described by pre-designed and pre-tested intellectual properties (IP's), these can be synthesized on FPGAs. They provide several advantages such as reduced cost, reduction in components, flexibility in choosing specific peripheral etc. Embedded systems are hardware and software components working together to perform a specific function. Now a day, designing an embedded system has become quite difficult due to tight constraints on area, power consumption, cost and size. Therefore, use of softcore processor is an ideal choice for the embedded system design. In this project, a soft processor (Microblaze) based embedded system is developed with RS-232 serial interface, Ethernet interface, 32MB SDRAM, 4MB PROM (platform flash), 16x2 LCD interface, 8 digital inputs and 8 digital outputs. The embedded systems is connected to the internet and remotely controlled and monitored. The TCP/IP stack is ported on Microblaze and Embedded Webserver is developed on FPGA board using HTTP communication protocol. Ethernet connectivity is tested between Embedded Web server on Microblaze and Web client on PC. Messages sent from the client side can be displayed over LCD on Webserver. Client can send commands to board for controlling IO's, for reading from RAM and for writing on RAM. Status check command sent by the client computer to Webserver updates the browser on PC to show status of IO's. It can also be used as slave processor to provide Ethernet connectivity to any 8- bit, 16-bit and 32- bit processors.**

TFTP server is also deployed in the Embedded Webserver Card so as to provide file transfer access to/from the client (Computer / Other Processor) with Barrel Shifter enabled in the Microblaze hardware.

Index Terms—**Embedded Webserver, Ethernet, FPGA, Intellectual Property (IP), Microblaze, Soft-core Processor and TFTP Server.**

I. INTRODUCTION

Embedded systems are specialized computer systems designed and optimized to perform a particular task. Usually they are a part of a larger system or a machine. Modern embedded systems are able to connect to the internet and can be remotely maintained and diagnosed. M2M (Machine to machine) communication is growing with a considerable rate. The possibility to connect two or more embedded systems enables developers to build more powerful distributed systems such as networked embedded systems. Remote maintenance is performed by different communication protocols. The most common communication protocol is HTTP which enables remote system control and monitoring. A web server is a computer program that implements HTTP protocol. It accepts HTTP requests from clients like web browsers and serves HTTP responses which are usually HTML pages with linked objects. There are many web servers available, and a number of them are free, like Apache, AOL, and Roxen. Internet Information Services, Sun Java System web Server are some of the most common commercial web servers. Some web servers can run on almost any operating system while others are platform specific. The general purpose web servers are intended to run on powerful server computers, workstations or personal computers and support a number of advanced features. On the other hand, web servers for embedded systems have limited resources and offer only a set of required features. Requirements of an embedded system web server are:

- *Small RAM and ROM footprint,*
- *Low CPU consumption,*
- *Easy integration with existing application, including static link with the operating system and application,*
- *Serving pages from the RAM if there is no hard drive.*

II. MICROBLAZE SOFT-CORE PROCESSOR

Microblaze is a virtual microprocessor that is built by combining blocks of code called cores inside a Xilinx Field Programmable Gate Array (FPGA). The beauty to this approach is that we only end up with as much microprocessor as we need. It is a 32-bit Harvard Reduced Instruction Set Computer (RISC) architecture optimized for implementation in Xilinx FPGAs with separate 32-bit instruction and data buses running at full speed to execute programs and access data from both on-chip and external memory at the same time.

III. SYSTEM DESIGN & DEVELOPMENT

Two ways that are studied in this project for TCP/IP communication are Socket API and RAW API.

The socket mode provides a simple API that blocks on socket reads and writes until they are complete. However, the socket API requires many pieces to achieve this, chief among them being a simple multithreaded kernel (xilkernel).

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Because this API contains significant overhead for all operations, it is slow.

On the other hand RAW API provides a callback style interface to the application. Applications using the RAW API register callback functions to be called on significant events like accept, read or write. All work is done in the callback functions.

Webserver is developed using LwIP TCP/IP stack in RAW API mode. It implements only a subset of the HTTP 1.1 protocol. Such a web server can be used to control or monitor an embedded platform via a browser. The web server demonstrates the following three features:

- Accessing files residing on a Memory File System via HTTP GET commands.
- Controlling the LED lights on the FPGA board using the HTTP POST command.
- Sending Data to the FPGA board using HTTP POST command and displayed over LCD
- Obtaining status of DIP switches from the FPGA board using the HTTP POST command.
- Interfacing with other processor.

The Xilinx Memory File System (xilmfs) is used to store a set of files in the memory of the FPGA board. These files can then be accessed via a HTTP GET [4] command by pointing a web browser to the IP address of the FPGA board and requesting specific files.

Controlling or monitoring the status of components in the board is done by issuing POST (issued XHR command for every POST Transaction from the client) commands to a set of URLs that map to devices. When the web server receives a POST command to a URL that it recognizes, it calls a specific function to do the work that has been requested. The output of this function is sent back to the web browser in JavaScript Object Notation (JSON) format. The web browser then interprets the data received and updates its display.

There is one main thread in embedded web server which listens on HTTP PORT (PORT 80) for incoming connections. For every incoming connection, a new thread is spawned which processes the request on that connection.

The http thread first reads the request, identifies if it is a GET or a POST operation, and then performs the appropriate operation. For a GET request, the thread looks for a specific file in the memory file system. If this file is present, it is returned to the web browser initiating the request. If it is not available, a HTTP 404 error code is sent back to the browser.

Computer side interface is developed in VB.net with web browser facility. It works under two modes:-

1. Single Device Mode
2. Multi Device Mode

In Single Device Mode user can connect directly with the card and control it via web browser while in Multi Device Mode all the devices can be read or send control signals or data simultaneously.

In TFTP Server GET and PUT command is used to retrieve and store file from/to the FPGA Board (stored in DDR2-SDRAM).

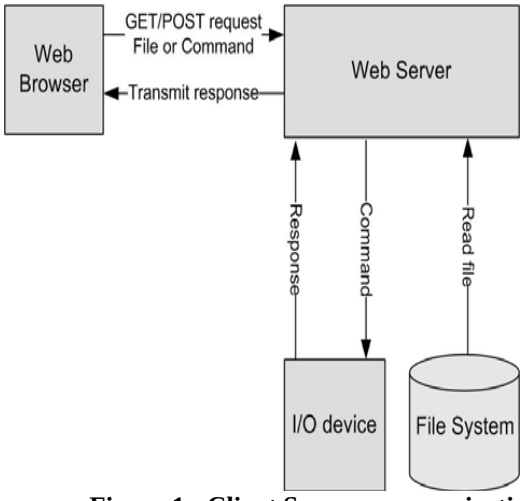

Figure 1 : Client Server communication

Platform flash is used to store the Bootloader while Parallel PROM is used to store images of the file system contains HTML pages, JScript, PDF etc which will be handled by the XilMFS and it also contains Webserver program (written in C) which will be called by the bootloader program. All the stored Application is loaded into the DDR2-SDRAM to start its execution to speed up the process. File system image is loaded into the Parallel PROM at an Offset of 0x00200000 from its Base Address while Webserver code is written at 0x00000000 offset.

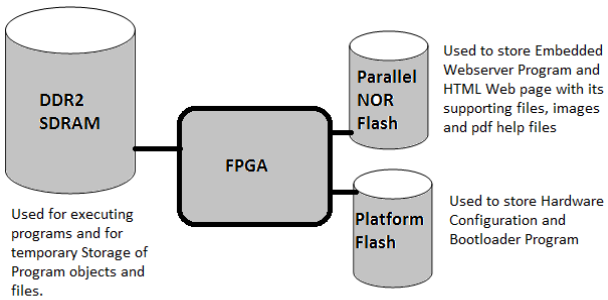

Figure 2 : Memory Interconnection with FPGA

When the system is Power ON then the FPGA configuration takes place and Bootloader Application is initialized into the BRAM which will copy all the S-Records (Application program file) till end from parallel NOR flash to DDR2-SDRAM and then its execution of the program starts at 0x000000 address of the RAM.

In the designed system Barrel shifter is enabled in the Microblaze hardware so as to increase speed. It has increased speed enormously around 58 % increase in throughput rate is noticed as compared when it is using only normal shifter. Also LCD controller is implemented in the hardware so as to reduce load from the processor. Enabling Data and Instruction Cache and increasing TCP window size also affects performance much.

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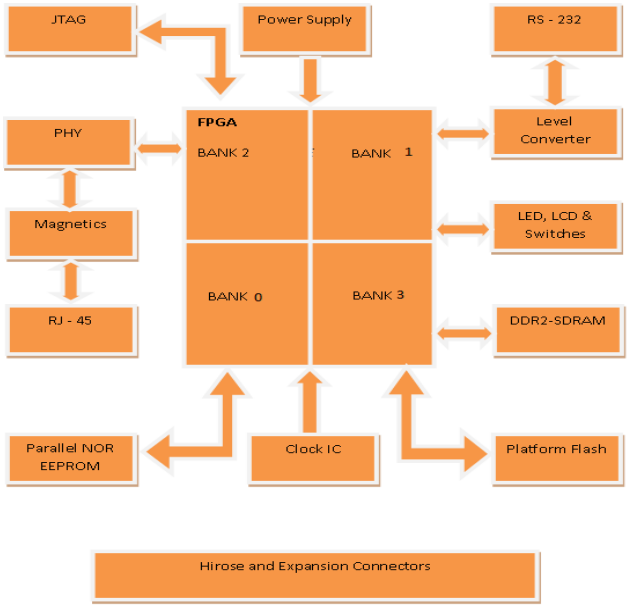

Figure 3 : Block Diagram of Developed Card

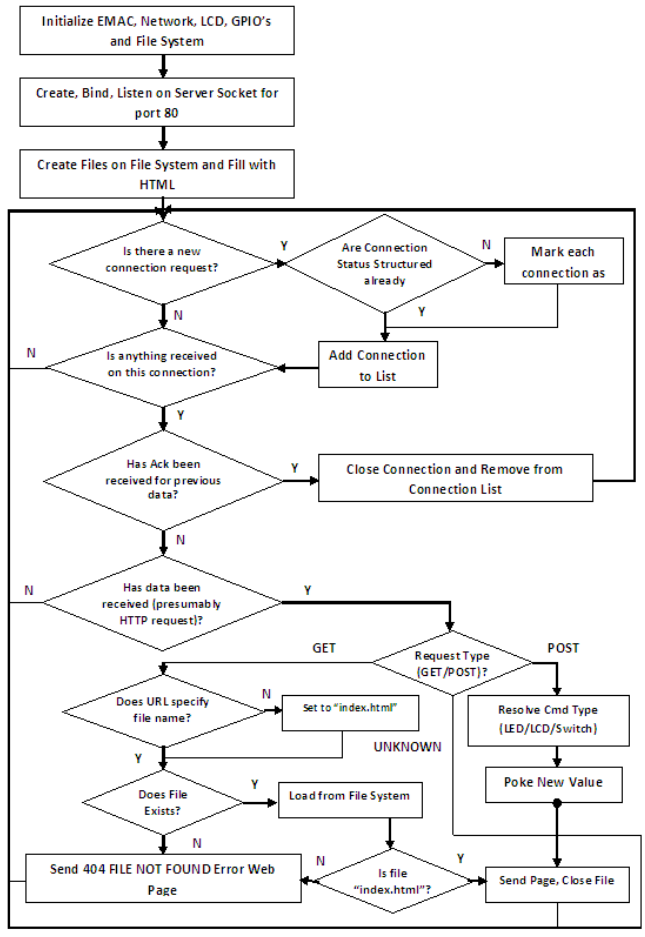

Figure 4 : Webserver Flow Chart

IV. TOOLS USED

- Xilinx ISE Design Suite
- Software Development Kit
- Xilinx Platform Studio
- Altium Designer
- Hyper Terminal

V.TESTING

Initializing Bitstream for hardware Testing

If the entire software application fits on FPGA block RAM blocks, the system can be initialized by updating the hardware bitstream with the block RAM initialization data. This updated bitstream can then be downloaded to the FPGA.

Downloading Design with Bootloader

Program a non-volatile Flash memory with the software and use a bootloader to copy it into RAM memory, and then execute it from there.

After the application has been copied, the bootloader executes it by branching to the entry point of the application. Usually, all interrupts are switched off when the bootloader is executing. The application is responsible for all interrupt handling.

Webserver Test[5]*: -*

Open WireShark, Hyper Terminal and SDK and then download the Webserver code into the FPGA board. Point browser to the IP Address of the Card, it will display the required web page with two Text Boxes and three command buttons. Enter the LED no. in the text box and then press Update LED then the corresponding LED will glow. Similarly if some text is written in the LCD text box and the press Update LCD then it will write over the LCD panel. Next is the Update Switches command button, used to read positions of the switches from the board and displayed in the web browser.

TFTP Test:-

Enter the following command in the command prompt to read file from Webserver.

C:\>tftp -i 192.168.1.10 GET index.html

It will show the following message...

Transfer successful: 3314 bytes in 1 second, 3314 bytes/s

Enter the following command in the command prompt to write file to the Webserver.

C:\>tftp -i 192.168.1.10 PUT test.txt

It will display the following message....

Transfer successful: 24 bytes in 1 second, 24 bytes/s

TCP RX/TX Throughput Test:-

To measure receive throughput, connect to the receive iperf application using the iperf client.

$ iperf -c 192.168.1.10 -i 5 -t 50 -w 8k

To measure the transmit throughput, first start the iperf server on the host, then run the executable on the board. When the executable is running, it tries to connect to a server at host

$ iperf -s -i 5

VI. RESULTS

Table 1 : Device Utilization Summary

	Used Capacity	Whole Capacity	Percentage of Capacity
Slices	5,348	5,888	91%
Lookup Tables	7,672	11,776	65%
Flip Flop	8,690	11,776	73%
IO Signals	135	372	36%
BRAM	16	20	80%

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Table 2 : TCP Receive and Throughput Results

Device	RAW Mode		Socket Mode	
	RX	TX	RX	TX
Spartan3 AN (66.5 MHz CPU Clock)	45.1 Mbps	20.2 Mbps	11 Mbps	10 Mbps

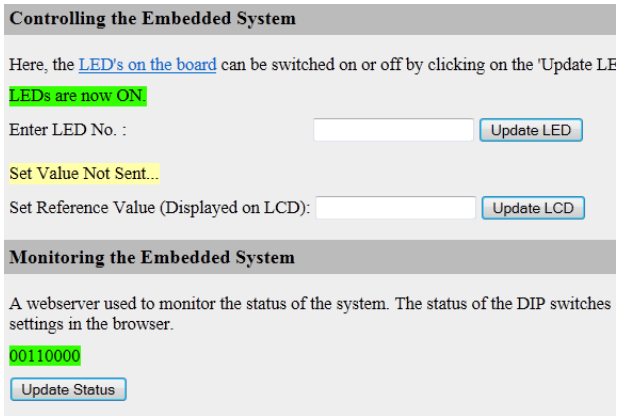

Figure 5 : Magnified view of the web page loaded in Internet Explorer

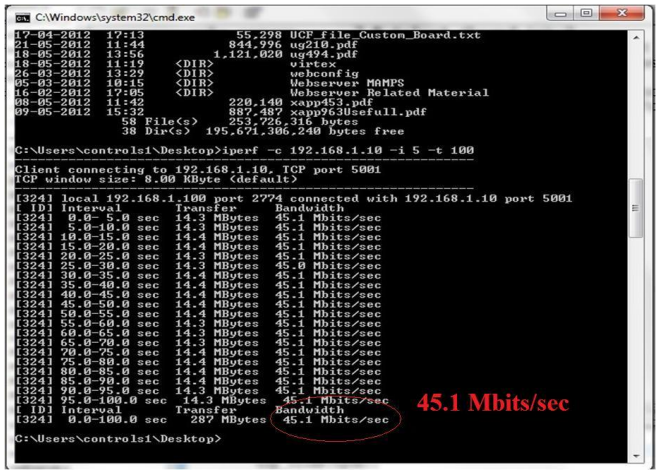

Figure 6 : Test Result showing Maximum Transmission Throughput of Embedded Webserver using iperf command line interface in Xilinx Spartan 3AN kit

Figure 7 : Spartan 3AN Starter Kit connected to a D-Link Switch for testing the logic of developed distributed embedded system

VII. CONCLUSION

FPGA board is designed, developed and schematic has been prepared for webserver and file server with minimal use of hardware and tested in Xilinx Spartan 3AN Board with a throughput of 24.1 Mbps.

VIII. APPLICATION

- It is used as an embedded Webserver and file server.
- FPGA Board can be used for distributed embedded systems.
- This board can be used for providing Ethernet communication to the system in which Ethernet support is not available.

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REFERENCES

[1]. Bryan H. Fletcher, "FPGA Embedded Processor Revealing True System Performance", Embedded Training Program, Embedded Systems Conference and San Francisco, ETP-367, 2005.
[2]. "Getting Started with Embedded System Development using MicroBlaze processor & Spartan-3A FPGAs", www.xilinx.com.
[3]. Franjo Plavec, Blair Fort, Zvonko G. Vranesic, Stephen D. Brown "Experiences with Soft-Core Processor Design",19th IEEE International Parallel and Distributed Processing Symposium (IPDPS'05)
[4]. Petar Borisov Minev (*Technical University of Gabrovo*) and Valentina Stoianova Kukenska (*Technical University of Gabrovo*) "Implementation Of Soft-Core Processors In Fpgas", In "International Scientific Conference" 23 – 24 November 2007, Gabrovo
[5] Stephen MacMahon, Nan Zang, Anirudha Sarangi "LightWeight IP (lwIP) Application Examples", XAPP 1026 (V3.1) , April 21, 2011

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