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Design and Implementation of Wideband Digital Down Converter on FPGA

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Abstract **— In a Communication system, the received signals are of high data rates making it difficult to process the signals to extract information of interest. So to solve this problem DDC makes a better solution. In this paper, an efficient way of designing and implementing a Wideband Digital down Converter has been discussed. It is shown that the signal of interest extracted till now is of narrowband but in this article extraction of wideband signals from the given ADC signal using advanced filtering and decimation techniques has been presented. Filtering is implemented in stages to obtain efficient response. Multiplier-free filter implementation providing decimation rates fron 4 to 4096 has been implemented. Also, the reasons for choosing FPGA over ASSP's to implement DDC are provided. Xilinx ISE 12.3 version software is used for simulating each block of DDC at system level testing and Chip Scope Pro Analyzer tool is used for board level testing. Vitex-5 FPGA with speed -2 is the hardware used for implementing the design.**

Keywords **— Wideband Digital down converter, ADC, Filtering and Decimation techniques, ASSP, FPGA, System level testing, Board level testing.**

I. INTRODUCTION

In the current scenario, Digital Communication is one of the commonly used modes of communication, due to its advantages over Analog Communication. A Digital Communication system has three basic blocks a transmitter, channel and a receiver. The DDC presented in this paper is the key component of Digital Radio Receiver. Digital Radio receivers often have fast ADC converters to digitize the band limited RF or IF signal generating high data rates; but in many cases, the signal of interest represents a small proportion of that bandwidth. A DDC allows the frequency band of interest to be moved down the spectrum so the sample rate can be reduced, filter requirements and further processing on the signal of interest become more easily realizable.

A Digital down Converter converts a digitized real signal centered at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency by using a mixer. Also in addition to down conversion, DDC's typically decimate to a lower sampling rate by using several stages of decimation filters. Before decimation, filtering is performed using linear phase filters to limit the bandwidth to our signal of interest. The decimated signal, with a lower data rate, is easier to process on a low speed DSP processor[1].

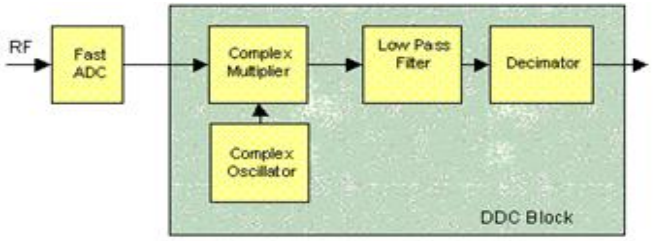


Fig. 1 Theoretical Block diagram of DDC

II. THEORY of DDC SYSTEM

A DDC consists of five basic blocks

i. NCO (numerically controlled oscillator)
ii. Mixer
iii. CIC (Cascaded integrate comb)
iv. CFIR (Compensation FIR) filter
v. PFIR (Programmable FIR) filter

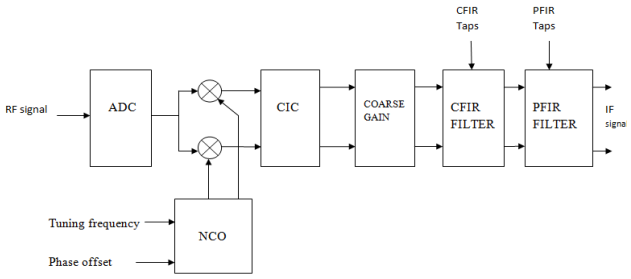


Fig. 2 Practical Implementation of DDC

Implementation of each block of DDC using advanced methods has been discussed in this section.

A.NCO

A numerically controlled oscillator (NCO) is a digital signal generator creating a synchronous (i.e. clocked), discrete-time, discrete-valued representation of a waveform, usually sinusoidal. Numerically Controlled Oscillators (NCO), also called Direct Digital Synthesizers (DDS), offers several advantages over other types of oscillators in terms of accuracy, stability and reliability. NCOs provide a flexible architecture that enables easy programmability such as on-the-fly frequency/phase.

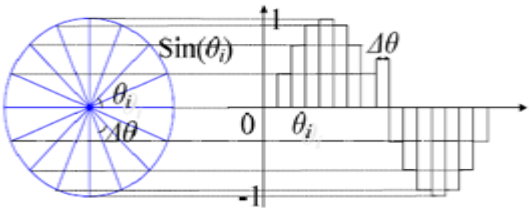


Fig. 3 Principle of NCO

A. An NCO generally consists of two parts:

- A **phase accumulator** (PA), which adds to the value held at its output a frequency control value at each clock sample.
- A **phase-to-amplitude converter** (PAC), which uses the phase accumulator output word (phase word) usually as an address into a waveform look-up table (LUT) to provide a corresponding amplitude sample.

1) Phase Accumulator: The phase accumulator is actually a modulo-*M* counter that increments its stored number by the value of Frequency Control Word (Tuning Frequency) each time it receives a clock pulse.

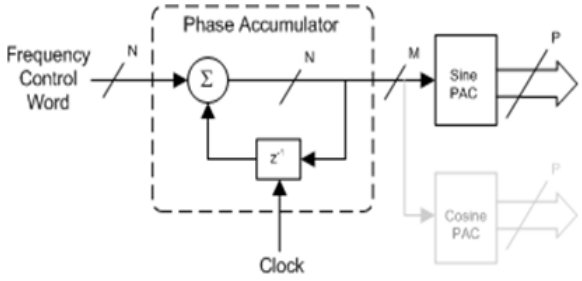


Fig. 4 Numerically Controlled Oscillator

Tuning frequency is obtained by using the below formula.

$$Fout = \Delta f / 2^N . f_{clk}$$

When clocked, the phase accumulator (PA) creates a modulo-2^N sawtooth waveform as shown in the below figure, where N is the number of bits carried in the phase accumulator. N sets the frequency resolution of the Numerically Controlled Oscillator.

2) *Phase-to-amplitude converter:* Each phase value from the PA serves as an address to the LUT which outputs corresponding amplitude value. Here the LUT is a memory that stores the amplitude values of sine wave for each phase value. The N-bit output from PA is truncated to M-bit as the memory space is 2^M only. The output of PAC is a sine wave.

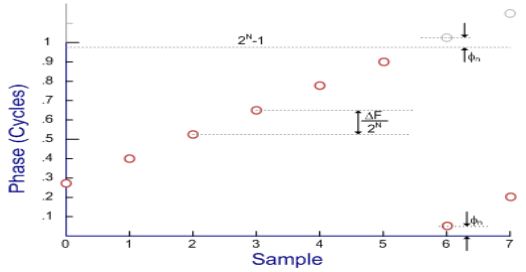


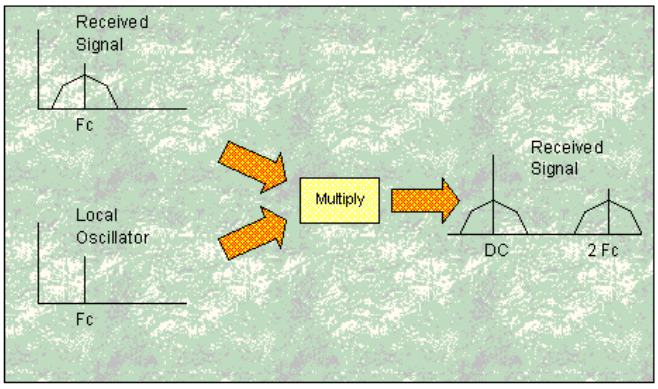
Fig. 5 Phase Accumulator Output

B. The Mixer

A mixer is used to convert the IF signal to baseband signal by multiplying the input signal with complex sinusoidal signal cos (wt)-*j* sin(wt) = e-jwt which is generated by NCO thus giving two signals as output i.e.;

i. In-Phase signal
ii. Quadrature-Phase signal

where these signals are 90 degrees out of phase with each other.



This works on the (simplified) mathematical principle: Frequency(A) * Frequency(B) = Frequency(A-B) + Frequency(A+B)[1].
The further stage is to remove unwanted components.

C. CIC Filter

The cascaded integrator-comb (CIC) filter is a class of hardware-efficient linear phase finite impulse response (FIR) digital filters. The CIC filter is suitable for this high-speed application because of its ability to achieve high decimation factors and other reason is it is implemented using additions and subtractions rather than using multipliers. It decimates by R which is programmable.

The two basic building blocks of a CIC filter are

1) An integrator (decimator): An integrator is simply a single-pole IIR filter with a unity feedback coefficient:
Y [n] = y [n-1] + x[n] (1)
This system is also known as an accumulator[2]. The transfer function for an integrator on the z-plane is

$$H_I(Z) = 1/(1 - Z^{-1})$$

2) Comb Filter (Interpolator): A comb filter running at the slow sampling rate fs/R is described by

$$y[n] = x[n] - x[n - M].$$

A comb filter is a differentiator with a transfer function

$$H_C(Z) = 1 - Z^{-M}$$

In this equation, *M* is the differential delay, and is usually limited to 1 or 2[2].

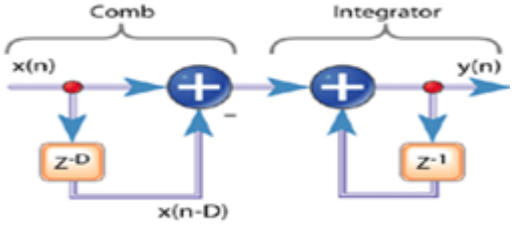


Fig. 6 Integrator and Comb filter

To summarize, a CIC decimator would have N cascaded integrator stages clocked at fs, followed by a rate change by a factor R, followed by N cascaded comb stages running at fs/R[5] .

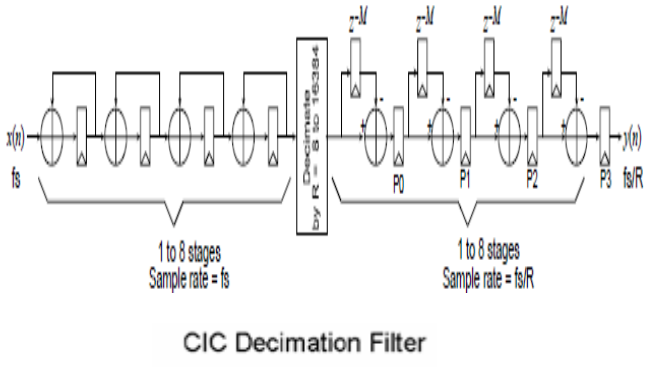


Fig. 7 CIC Filter

Frequency Characteristics:

The transfer function for a CIC filter at fs is

$$H(Z) = H_I(Z)H_C(Z) = \frac{(1- Z^{-RM})^N}{(1- Z^{-1})^N} = \left[\sum_{K=0}^{RM-1} Z^{-K}\right]^N$$

The magnitude response at the output of the filter is as shown below[3] .We can obtain an expression for the CIC filter's frequency response by evaluating $H_{cic}(z)$ transfer function on the *z*-plane's unit circle, by setting $z = e^{j}2\pi f$, yielding:

$$H_{cic}(e^{j2\pi f}) = \frac{1- e^{-j2\pi fD}}{1- e^{-j2\pi f}}$$

$$= \frac{e^{-j2\pi fD/2}(e^{j2\pi fD/2} - e^{-j2\pi fD/2})}{e^{-j2\pi f/2}(e^{j2\pi f/2} - e^{-j2\pi f/2})}$$

Using Euler's identity $2j\sin(\alpha) = e^{j\alpha} - e^{j\alpha}$, we can write:

$$H_{cic}(e^{j2\pi f}) = \frac{e^{-j2\pi fD/2}\,2j\sin(2\pi fD/2)}{e^{-j2\pi f/2}\,2j\sin(2\pi f/2)}$$

$$= e^{-j2\pi f(D-1)/2}\,\frac{\sin(\pi fD)}{\sin(\pi f)}.$$

where here D = M = Differential Delay

It is a sinc function

$$|H(f)| = \left|\frac{\sin \pi Mf}{\sin \frac{\pi f}{R}}\right|^N$$

In the CIC Filter there is a disadvantage i.e.; it exhibits pass band droop. So we use CFIR to compensate this.

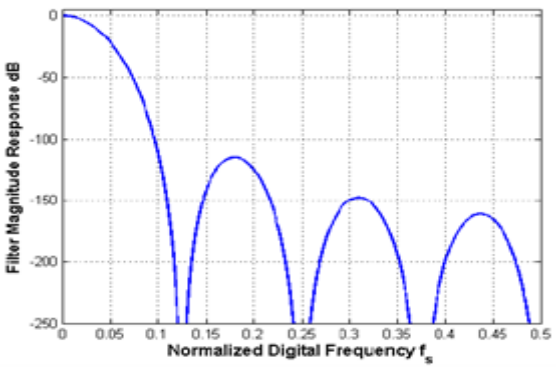


Fig. 8 Magnitude Response of CIC Filter

D. Compensation FIR filter:

The output of the CIC filter has a sinc shape, which is not suitable for most applications. A "clean-up" filter can be applied at the CIC output to correct for the pass band droop, as well as to achieve the desired cut-off frequency and filter shape. This filter typically decimates by a factor of 2 or 4 to minimize the output sample[4]. This filter will operate at low frequency (fS/*R)* to achieve a more efficient hardware solution. Its magnitude response is an inverse-sinc function.

$$G(f) = \left|MR\left(\frac{\sin(\pi f/R)}{\sin(\pi Mf)}\right)\right|^N \approx \left|\frac{\pi Mf}{\sin(\pi Mf)}\right|^N = \left|\sin c^{-1}(Mf)\right|^N$$

As before, the filter order can be limited such that it can be implemented in a single MAC unit, in this case N=62 (63 filter taps).

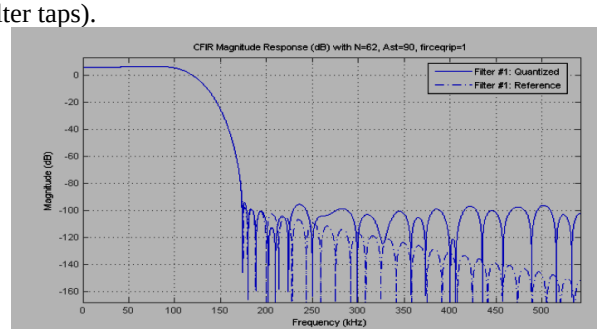


Fig. 9 Magnitude Response of CFIR Filter

III. IMPLEMENTATION on FPGA

An advantage of using an FPGA for the DDC is that we can customize the filter chain to exactly meet our requirements. ASSPs don't offer the design flexibility or integration attainable in an FPGA.

During filter design, a behavioral model of the complete DDC is generated using Xilinx ISE software by writing VHDL code for each individual block and their operation is tested by simulating the design using Modelsim Simulator. Later the design is synthesized and implemented on an FPGA by generating a .bit file of the design and programming, configuring the FPGA with the .bit file. The correct operation of the design in the FPGA is tested using Chip Scope Pro Analyzer tool which uses three main blocks to analyze any part of DDC. These blocks are generated through the IP Core Generator tool in Xilinx ISE. The blocks are:

1) ICON: Integrated controller is use as an interface between the other two blocks and PC, JTAG which is connected to FPGA on which the design is programmed.

2) ILA: Integrated Logic Analyzer is used to control the inputs of any part of DDC thus achieving Controllability of inner circuits.

3) VIO: Virtual input output is used to observe the outputs of any part of DDC thus achieving observability.

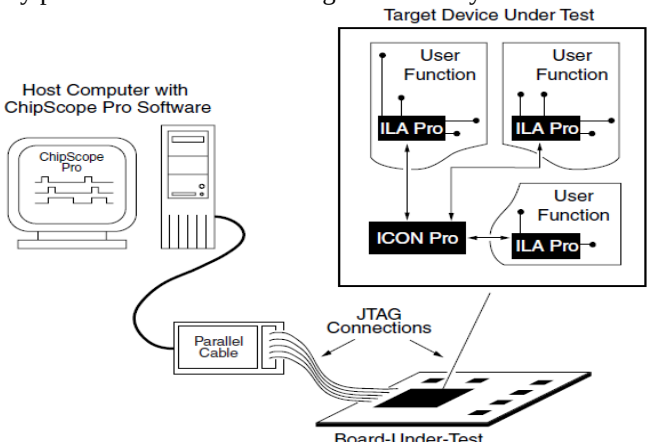


Fig. 10 Chip Scope pro Block Diagram

Thus Board level testing has also been performed.

Why to choose FPGA:

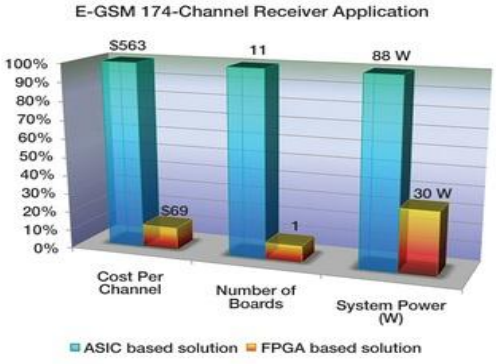


Fig. 11 Comparison of ASIC and FPGA

IV. SIMULATION RESULTS

Thus the results at each block of DDC have been shown. Here the sine wave is generated at 30MHz output frequency, thus the tuning frequency is 30MHz
and clock frequency is 100MHz . The input signal to the mixer is 70MHz. The output of the mixer is in kHz.

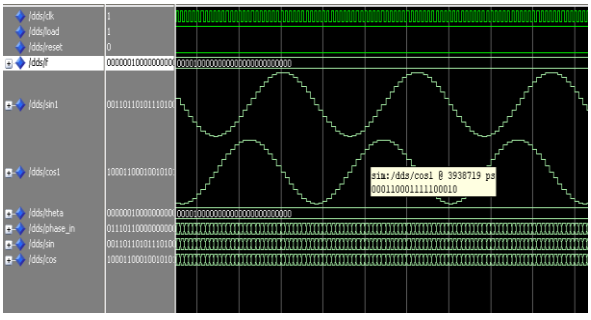


Fig. 12 Output wave generated by NCO

The signal from the mixer is filtered and decimated through CIC and is shown below.

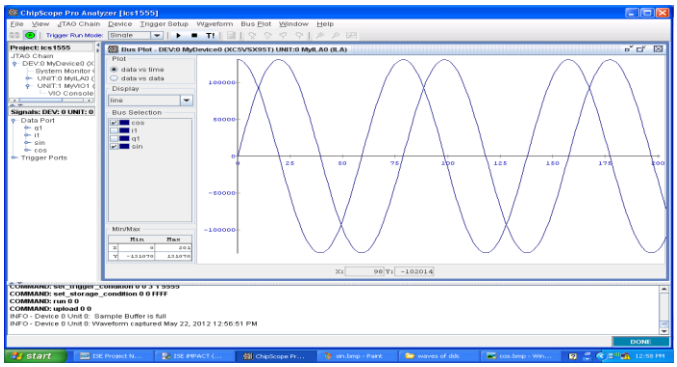


Fig. 13 NCO Output : Result from Chip Scope Pro Analyzer

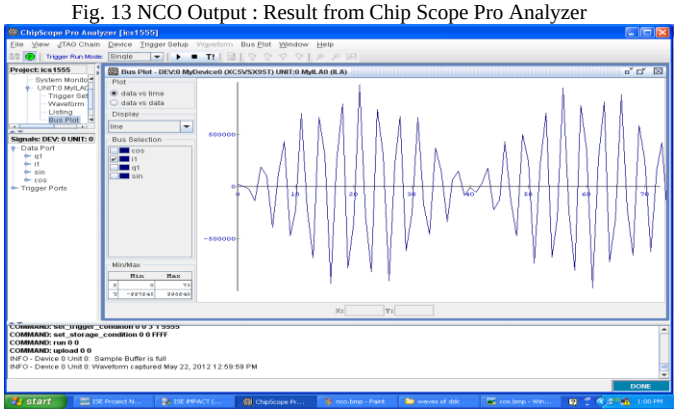


Fig. 14 Mixer(I) signal output from Chip Scope Pro Analyzer

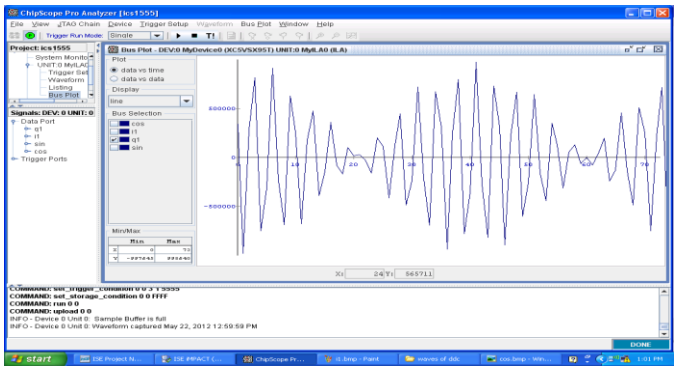


Fig. 15 Mixer(Q) signal output from Chip Scope Pro Analyzer

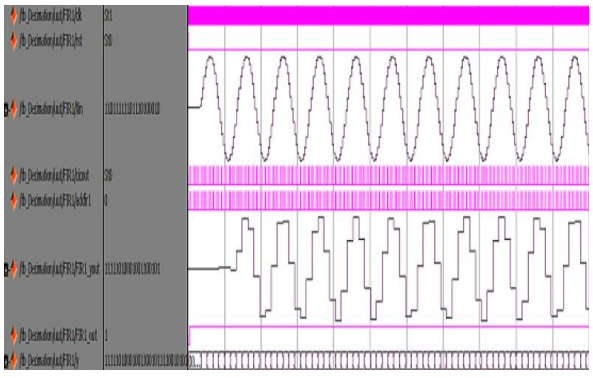


Fig. 16 Output of CIC Filter

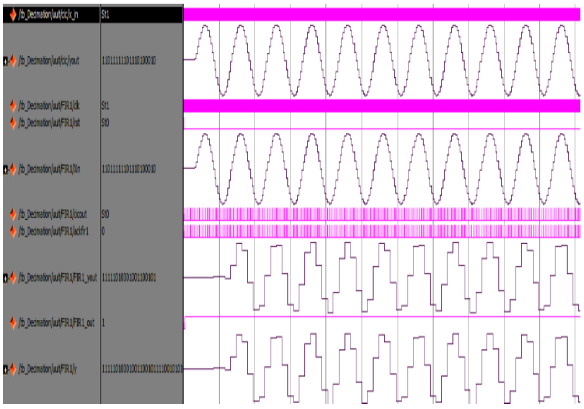


Fig. 17 Output of DDC

Thus the output of DDC which contains signal of interest has been obtained.

CONCLUSION

The components are been designed such that the end users can customize the design according to their requirements by simply modifying certain parameters in each block. Also as FPGA is choosen as the target technology, it results in a design with low power consumption, accurate performance, high integration and customizability. Further if required the components of DDC can be designed to work at higher rates by further improving their architectures .

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