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Design & Implementation of 64 bit ALU for Instruction Set Architecture & Comparison between Speed/Power Consumption on FPGA

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Abstract

In the present paper design of 64 bit ALU is presented. Arithmetic Logical Unit is the part of Microprocessor. All the arithmetic & logical functions are performed inside the ALU. So ALU is the heart of the microprocessor.The speed of the ALU decides the speed of the microprocessor. Now in MOS Technology the power consumption is depend upon then switching frequency of the clock as

$P=CV^2f$

Here P is the power consumption

C is the capacitance of the interconnections

f is the clock frequency of the design

So if the clock frequency is reduced then the power consumption is less but on the other side of the coin the speed (performance) is reduced at a significant amount.So we should choose a architecture so that when no instruction is available to ALU it is transferred in power down mode i.e during the waiting states no power is consumed by the ALU.ALU is the part of the instruction set architecture defined the microarchitecture of the processor. The processor architecture is defined by the instruction set.

Keywords

ALU, ISA , Microprocessor, MOS Technology, Power Consumption, Power Down mode, Speed

Introduction

Processor is the brain of the computer. Now ALU is the heart of the processor. In the designing of superscalar processors Fetch, Decode, Execute & Write back stages are present. Now ALU is the building block of the Execute stage. Now to execute the instruction operation code & the operand (digital data) is required. Now the Opcode is transferred by control unit tell the processor which operation is done at which time. Now the two operands of desired width is transferred by the register file. In this particular paper design of 64 bit ALU is presented which is operated at low power consumption. Low power design is important in hand held devices such as mobile phones in which long backup of the battery are required. In the present design if instruction is not available to ALU then it becomes off i.e no power is consumed. So this is the additional arrangement in the present design.

Architecture Design

First of all the specifications are written first. In the present architecture x & y is the 64 bit input (operands) and z is the 64 bit output. Here clk is the clock signal taken as negative edge triggered for fast triggering. Here the clock contains a period of 100ns i.e 10MHz frequency. control is the control signal generated by the Finite State Machine (FSM) tell the ALU which operation is done. Which operation is done by the ALU is decided by the instruction set of the processor

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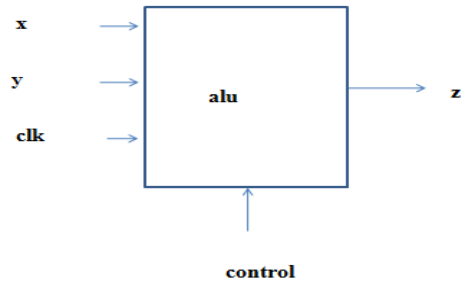


Instruction Set

Instruction Set of the Processor contains 16 different instructions such as arithmetic, logical, shifting operations & data transfer instructions which are given as follows

Instruction	**Opcode**
Add	0000
Sub	0001
Mul	0010
Logical AND	0011
Logical OR	0100
Left Shift	0101
Right Shift	0110
NOT	0111

NAND	1000
NOR	1001
Bitwise AND	1010
Bitwise OR	1011
Bitwise NAND	1100
Bitwise NOR	1101
Move	1110
Compare	1111
Power Down Mode	zzzz

Simulation Result

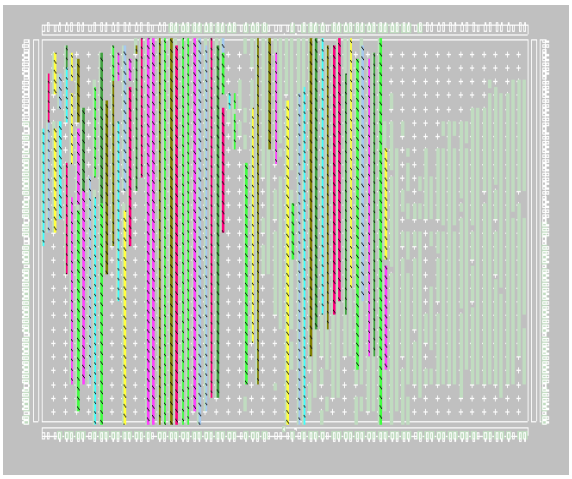
After architecture design the specifications are converted into RTL (Register Transfer Level).RTL is written in Verilog HDL (Hardware Description Language).Now to check the functionality simulation is done in modelsim.Here the clock latency of the clock is 8.The frequency of the clock is 10MHz.

Synthesis Report

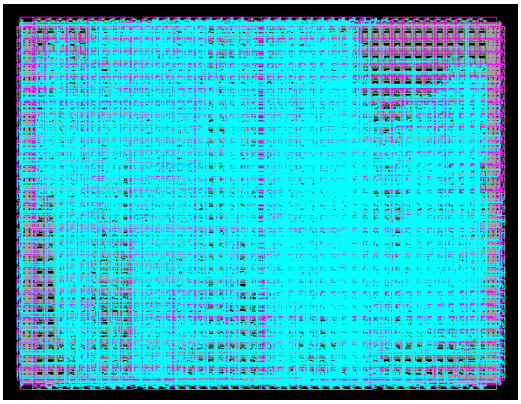
To generate the gate level netlist Xilinx ISE 9.2i is used. So that the design is technology dependent. To generate the netlist Synthesis is done on Spartan2 FPGA.As we see from the table Gate count is 36308.Now the final Chip contains 196 pins. So the final design is implemented on 0.18µm CMOS Technology.

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	3,346	4,704	71%	
Logic Distribution				
Number of occupied Slices	1,696	2,352	72%	
Number of Slices containing only related logic	1,696	1,696	100%	
Number of Slices containing unrelated logic	0	1,696	0%	
Total Number of 4 input LUTs	3,354	4,704	71%	
Number used as logic	3,346			
Number used as a route-thru	8			
Number of bonded IOBs	196	284	69%	
IOB Flip Flops	128			
Number of GCLKs	1	4	25%	
Number of GCLKIOBs	1	4	25%	
Total equivalent gate count for design	36,308			
Additional JTAG gate count for IOBs	9,456			

Chip Floorplan



Chipdesign



Power Report

```
Power summary:                          I(mA)     P(mW)
---------------------------------------------------------------------
Total estimated power consumption:                   7
                                        ---
                      Vccint 1.20V:       0         0
                      Vcco33 3.30V:       2         7
                                        ---
                           Clocks:        0         0
                           Inputs:        0         0
                            Logic:        0         0
                          Outputs:
                             Vcco33       0         0
                          Signals:        0         0
                                        ---
           Quiescent Vcco33  3.30V:       2         7

Thermal summary:
---------------------------------------------------------------------
   Estimated junction temperature:                  25C
                  Ambient temp:  25C
                     Case temp:  25C
                Theta J-A range:   9 -  22C/W
```

Final Result

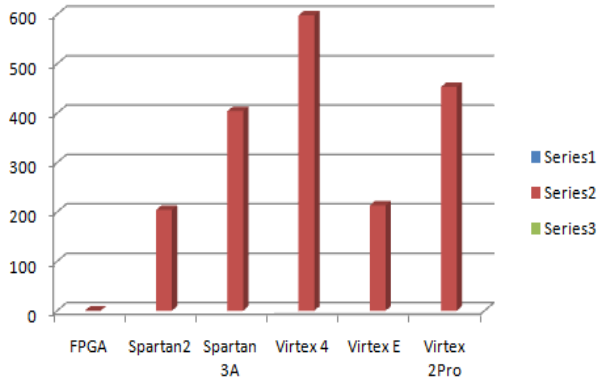
Parameter	**Value**
Clock Latency	8
Net Delay	5.753ns
Gate Delay	6.959ns
LUT	3354
Slices	1696
Setup Time	32.463ns
Hold Time	6.956ns
Fanout	64
Power Consumption	7mW
Speed	203.087MHz

Estimation of Performance Parameters on FPGA

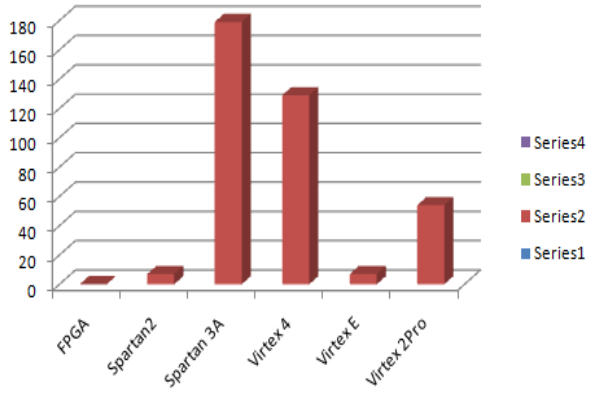
Parameter	***Spartan2***	***Spartan 3A***	***Virtex 4***	***Virtex E***	***Virtex 2Pro***
Net Delay(ns)	5.753	4.891	3.487	5.047	2.962
Gate Delay(ns)	6.959	5.271	3.766	5.967	3.340
LUT	3354	1699	1486	3573	1699
Slices	1696	940	827	1893	924
Setup Time(ns)	32.463	21.488	16.827	22.549	14.368
Hold Time(ns)	6.956	5.271	3.766	5.967	3.340
Fanout	64	64	64	64	64
Power Consumption (mW)	7	179	129	7	54
Speed(MHz)	203.087	403.234	597.086	212.811	452.131

Results

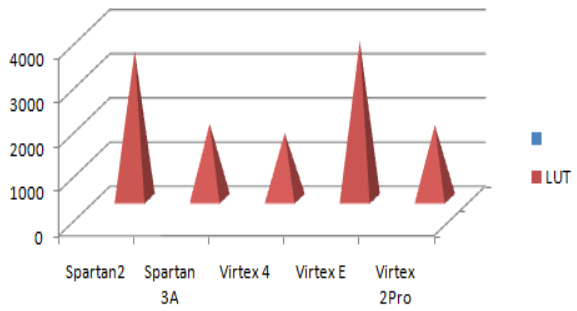
FPGA/Speed



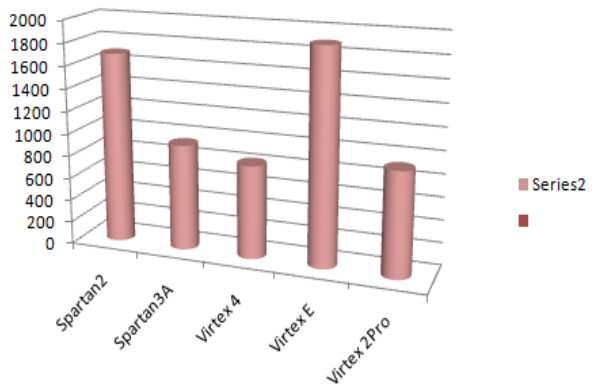
FPGA/Power Consumption



FPGA/LUT



FPGA/Slices



Discussion & Conclusion

The final design is implemented on 0.18µm CMOS Technology with gate count of 36308.Present design is used for low power consumption. In future we can implement the design for low chip area i.e the low fabrication cost. The design can be done for high speed but in that case the power consumption increases. So there is a compromise between the speed & power consumption. The final design supports 203.087 MHz clock frequency when implemented on FPGA. Virtex 4 provides the highest speed & Spartan 2 provides the lowest power consumption. Virtex 4 Provides low chip area (slices are less).Among these architectures Virtex E provides high speed and low power consumption.

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Rajeev Kumar obtained his MSc Electronic Science & M.Tech (Microelectronics & VLSI Design) Degree from Deptt of Electronic Science, Kurukshetra University, Kurukshetra (Haryana).Currently working as Coordinator M.Tech ECE Program in IITT College of Engineering, Punjab. He is the member of R&D in the IITT College. He is also the member of IAENG (International Association of Engineers), Research Gates & Silicon India. He worked in the field of High Speed Processor Architecture, Low Power VLSI Design & Implementation of Hardware for DSP. He is currently involved in Design & Implementation of VLIW Processor for Reconfigurable Architecture. In future he is interested to work in ASIP Design for Low Power, Design of Hardware for Neural Network and Design of DSP Processor for Image Processing. He is keen for Reconfigurable Computing. During M.Tech they are involved in Full Custom design of 0.1µm NMOS inverter. For Synthesis purpose in Verilog HDL based design they used the library of Semi Custom Design (ASIC) & FPGA. He is involved logic verification of gates & architecture in C Language in Linux Operating System. They worked in the area of Microelectronics during MSc Electronic Science (Thin Film Deposition, Photolithography & Wet Etching).

Manpreet Kaur done his B.Tech ECE from Bhutta College of Engineering Ludhiana, Punjab.Pursuing M.Tech ECE form IITT College of Engineering,Punjab.In B.Tech they done their project in Dynamic Host Configuration.Her research interest is DSP, Wireless & Mobile Communication, and Low Power VLSI Design. In future she is interested to work in high performance Reconfigurable Computing.