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ON-CHIP CRYSTAL OSCILLATOR WITH BETTER ESD & LATCH-UP PROTECTION

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Abstract: ***There are no stand alone on-chip crystal oscillators are available for R&D activities and lab evaluation of a new circuit. The ESD Protected ON-CHIP crystal oscillator is simple and robust to use. It protects itself against any sudden transients that might occur during handling. Thus it is useful for reference designs & electronic Research & Development activities. The On-Chip Crystal Oscillator can be designed by using a layout tool MICROWIND 3.1.7 version. Here the simulation is based on the Tanner Tool.***

I. INTRODUCTION:

A Crystal Oscillator is a timing device that consists of a crystal and an oscillator circuit, providing an output waveform at a specific frequency. When a crystal is placed into an amplifier circuit (as shown in Figure1), a small amount of energy is fed back to the crystal, which causes it to vibrate. These vibrations act to stabilize the frequency of the oscillator circuit.

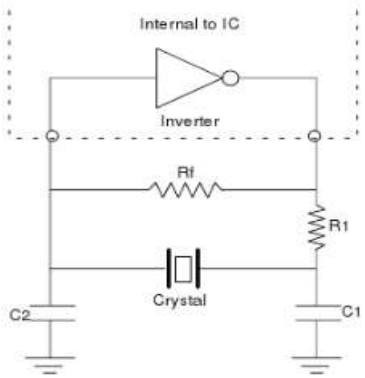


Figure1: Crystal Oscillator Circuit.

Figure1. shows the recommended Crystal Oscillator circuit diagram. In this type of setup the crystal is expected to oscillate in parallel resonant mode. The Inverter which is internal to the chip acts as class AB amplifier and provides approximately 180^0 phase shift from input to the output and the pi network formed by the crystal,R_1,C_1 and C_2 provides additional 180^0 phase shift. So the total phase shift around the loop is 360^0. This satisfies one of the conditions required to sustain oscillation. The other condition, for proper start up and sustaining oscillation is the closed loop gain should be ≥ 1.

The resistor R_f around the inverter provides negative feedback and sets the bias point of the inverter near mid-supply operating the inverter in the high gain linear region. The value of this resistor is high, usually in the range of a 500kilo ohm-2 mega ohm. Some of MXCOM's ICs have this resistor internal, refer to the external component specifications in the data sheet of a particular chip.

Select a crystal with low effective series resistance (ESR), which helps with crystal start-up problems. Lower ESR increases the loop gain. Reduce the stray capacitance on the board layout by shortening the traces. This would help with start up problem and as well as the frequency of oscillation.

The capacitors C_1 & C_2 form the load capacitance for the crystal. The optimum load capacitance(C_L) for a given crystal is specified by the crystal manufacturer. The equation to calculate the values of C_1 and C_2 is

$$C_L=(C_1*C_2)/(C_1+C_2)+C_S$$

Where C_S is the stray capacitance

The ON-CHIP Crystal oscillator with the following aspects :

i. Electro Static Discharge(ESD)
ii. LATCH-UP Protection

I.Electro static discharge (ESD) is a form of electrical over stress caused by static electricity.

The precautions taken for On-Chip crystal oscillator protected from Electro static discharge(ESD) are

i. Proper handling precautions will minimised the risks of electro static discharge.
ii. ESD sensitive components should always be stored in a static shielded packaging.
iii. Humidifiers, ionizers and antistatic mates can minimize the build-up of static charges around workstations and machinery.

These precautions reduce but do not eliminate ESD damage, so manufacturers routinely include special ESD structures on-board integrated circuit. These structures are design to observe and dissipate moderate levels of ESD energy without damage.

II.LATCH-UP Protection can cause physical destruction of an IC due to excessive power dissipation and consecutive overheating.

The LATCH-UP problem can overcome by introducing of guard rings in the layout.

The block diagram of the proposed system is shown below

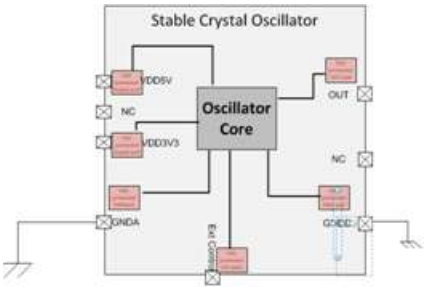


Figure2: On-Chip Crystal Oscillator with ESD protection

Here the Oscillator Core is the Crystal Oscillator to which the ESD protected supply pad, signal pad, ground pad and the input /output pads are externally connected to it.

II.SCHEMATIC DIAGRAM OF THE CRYSTAL OSCILLATOR

The schematic diagram of the proposed crystal oscillator circuit is shown below in the figure

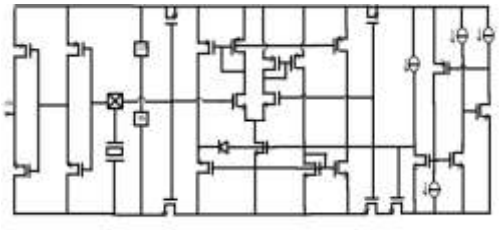


Figure3: Complete Schematic Diagram Of The Crystal Oscillator

III. MICROWIND TOOL:

i. Microwind is a friendly PC tool for designing a circuits at layout level.
ii. The package contains a library of common logic and analog ic's to design.
iii. The tool features various views like 2D cross section, 3D process viewer.

The Complete layout design of the crystal oscillator circuit which is drawn using microwind tool is shown below in the figure4

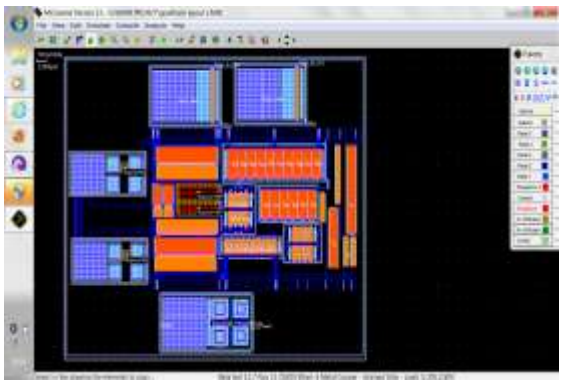


Figure4: Layout Diagram Of The Crystal Oscillator Circuit

ISSUES IN ANALOG LAYOUT:

The layout is the representation of a circuit in the physical domain.

It must contain all the information required to generate the masks for circuit fabrication.

The physical mask layout of any circuit to be manufactured using a particular process must confirm to a set of geometric constraints or rules, which are generally called layout design rules.

These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and poly silicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

a) DESIGN RULES:

The design rules are usually described in two ways:

Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers, or,

Lambda rules, which specify the layout constraints in terms of a single parameter(lambda) and thus allow linear, proportional scaling of all geometrical constraints.

b) Matching of Devices:

Matching is important because most analog circuit designs use a ratio based design techniques (e.g. current mirrors).

Some common techniques that help improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT.

FINGERING:

Analog transistor often having large Width/Length Using identical finger geometries.

Transistors of different widths and lengths match very poorly. Even minimally matched devices must have identical channel lengths Most matched transistors require relatively large widths and are usually divided into sections , or fingers.

Each of these fingers should have the same width and length as all others.

The pattern of the fingering is shown below in the Figure5

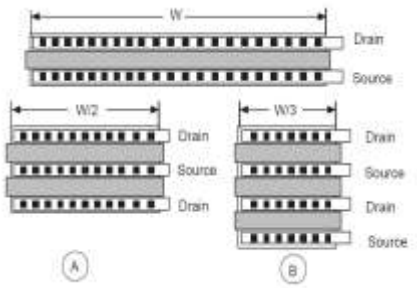


Figure5: Pattern of the Fingering

COMMON CENTROID:

Common-Centroid layout design guidelines:

a. Placement: The geometric center of the devices to match must be very near.

b. Symmetry: The layout of the devices must be evenly distributed in both directions: x and y.

c. Regularity: Partial devices must be distributes uniformly.

d. Dispersion: The layout must be as compact and square as possible.

e. Orientation: The number of partial devices oriented in each direction must be the same for each device to be match.

The diagram for the common centroid technique is shown below:

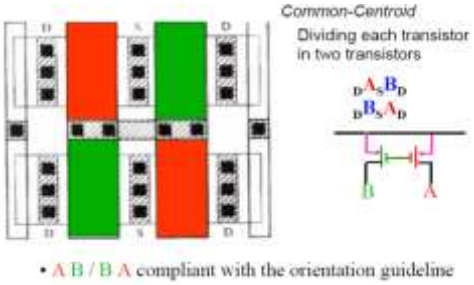


Figure6: Common-Centroid Technique

c) DUMMY RESISTORS

In order to minimize the noise, resistor can be designed

a) with a guard ring

b) inside a well to reduce the coupling to the substrate.

c) The dummy resistor pattern is shown in the following Figure7

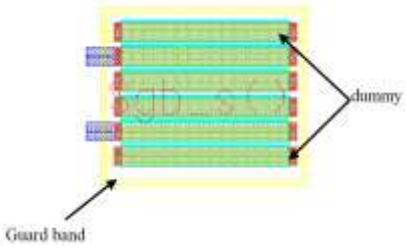


Figure7: Dummy Resistor Pattern

IV. TANNER TOOL:

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow to enter schematic, perform SPICE simulations.

There are 3 tools that are used for this process:

S-edit - a schematic capture tool

T-SPICE – the SPICE simulation engine integrated with S-edit

L-edit - the physical design tool

If any errors or warnings are there then it will be shown at the bottom. After click on the simulator the T-Spice window will appear. If everything is ok, the waveform viewer will also appear.

VIEW THE NET LIST:

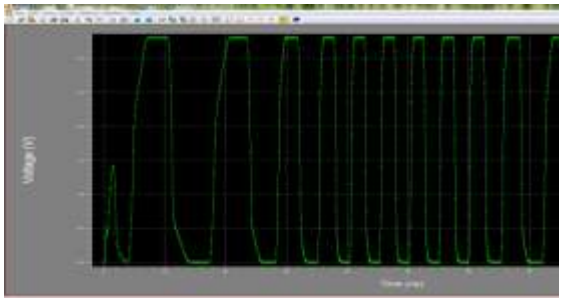
To see the net list in the T-SPICE window, right click on the file at the bottom and select " show net list "

This is a good place to look when you get errors. This is the text based description of what we have entered in S-edit.

Figure8: Netlist window

VI SIMULATION RESULTS

The simulation results of schematic of the crystal oscillator is shown in the below figure9 which is obtained in w-edit window.



CONCLUSION

It can be concluded that this oscillator covers all the aspects like Perfect Matched Layout, Robust ESD Performance on Output Pins, Highly Stable Oscillations, and the on-chip with better ESD & Latch-up Protection.

REFERENCES

1) ESD protected on-Chip Crystal Oscillator, International Journal of Computer Science and Information Technologies,Vol.3(3),2012
2) Design of Low Power CMOS Crystal Oscillator with Tuning Capacitors, Advance online publication.
3) The ART of ANALOG LAYOUT by alan hastings
4) ON-CHIP ESD Protection for Integrated Circuits(an IC design perspective)
5) CMOS Analog Circuit Design, phillip E. Allen, Douglas R. Holberg , second edition.
6) Guide to the Tanner EDA v12.6 design tools2011

Gowthami Kolukuluri received BTech degree in electronics and communication engineering from Jawaharlal Nehru technological University. She is currently pursuing the M.Tech degree in VLSI at M.V.G.R.College of Engineering.

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